

4 x 5 SoM Integration Guide

Table of Content

- 1 [Table of Content](#)
 - 1.1 [Power and Signal Pin Assignment](#)
 - 1.1.1 [How to Use This Guide](#)
 - 1.1.2 [Module Power Connection Table](#)
 - 1.1.3 [Module Pinout Overview](#)
 - 1.1.4 [Carrier Board Power Connection Table](#)
 - 1.1.5 [Carrier Pinout Overview](#)
 - 1.2 [4x5 Module Controller IOs](#)
 - 1.3 [Remove 4x5 module](#)
 - 1.4 [Compatibility Guide](#)
 - 1.4.1 [Ethernet LED'S](#)
 - 1.4.2 [JM2 pins 1, 3 \(TE0720 Bank 34 Voltage\)](#)
 - 1.5 [Carrier Board Checklist](#)
 - 1.5.1 [Schematic Checklist](#)
 - 1.5.2 [PCB Checklist](#)
 - 1.5.3 [Visual Check of Module placement](#)

Power and Signal Pin Assignment

How to Use This Guide

- This guide is split into two tables:
 - **Module Power Connection Table** section shows the power source of the different FPGA banks and components of the different module boards as well as the power and group location on the B2B connectors of the module site.
 - **Carrier Board Power Connection Table** section shows the power source of the B2B connectors with pins, schematic names and available options of the different carrier boards as well as the power location on the B2B connectors of the carrier site.
 - The PCBs have fixed and variable user supplied I/O voltage pins. Variable power supply pins are colored in four groups (VCCIOA, VCCIOB, VCCIOC and VCCIOD).
1. Find your module model on the **Module Power Connection Table** and check the power supply of the different FPGA banks.
 2. If the power supply is variable(colored), go to the **Carrier Board Power Connection Table** and see how it's connected on your carrier board. Often the power source can be selected by jumper, resistor or variable used from other connector pin of the carrier board. So use the schematic name or the component designator from the table to search for the available options in the PCB schematics or TRM.
 3. Additional Master Pinout Viewer/XDC-Generator is available on [Trenz Electronic Download - Pinout](#)

Module Power Connection Table

Group	1				2				3				4				5				6				7				8	9	special
Module Model	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage			
TE0710	B15	48	HR	VC CIOA	-	-	-	-	-	-	-	-	B34	50	HR	VC CIOD	B16	6	HR	3.3 V	B14	8	HR	3.3 V	2x 100Mb it ETH						
TE0711	B15	48	HR	VC CIOA	B34	36	HR	VC CIOB	B14	18	HR	3.3 V	B35	50	HR	VC CIOD	B16	6	HR	1.8 V	B14	8	HR	3.3 V	B34	8	HR	VC CIOB	B34(4)	USB	
TE0712	B16	48	HR	VC CIOA	B13	20	HR	VC CIOB	B14	18	HR	3.3 V	B15	50	HR	VC CIOD	B13	6	HR	VC CIOB	B14	8	HR	3.3 V	1x 100Mb it ETH / B13	4	HR	VC CIOB		B14	4x GTP on G2
TE0713																															4x GTP on G2
TE0715 with Z-7015 Z-7012S	B13	48	HR	VC CIOA	B34	16	HR	VC CIOC	B34	18	HR	VC CIOC	B35	50	HR	VC CIOD	B5 01	6	MIO	1.8 V	B500	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTP on G2

TE0715 with Z-7030	B13	48	HR	VC CIOA	B34	16	HP	VC CIOC	B34	18	HP	VC CIOC	B35	50	HP	VC CIOD	B5 01	6	MIO	1.8 V	B500	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTP on G2
TE0720	B35	48	HR	VC CIOA	B34	36	HR	VC CIOB	B33	18	HR	VC CIOC	B13	50	HR	VC CIOD	B5 01	6	MIO	1.8 V	B500	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	
TE0820*	B66	48	HP	VC CIOA	B65	16	HP	VC CIOC	B65	18	HP	VC CIOC	B64	50	HP	VC CIOD	B5 01	6	MIO	3.3 V	B5 01	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTR on G2
TE0821*	B26	48	HD	VC CIOA	B65	16	HP	VC CIOC	B65	18	HP	VC CIOC	B24	48	HD	VC CIOD	B5 01	6	MIO	3.3 V	B5 01	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTR on G2
TE0823*	B66	48	HP	VC CIOA	B65	16	HP	VC CIOC	B65	18	HP	VC CIOC	B64	50	HP	VC CIOD	B5 01	6	MIO	3.3 V	B5 01	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTR on G2
TE0741	B13	48	HR	VC CIOA	B16	16	HR	VC CIOB	B15	18	HR	VC CIOC	B12	50	HR	VC CIOD	1x GTX	1 Lane			B14	8	HR	3.3 V	2x GTX	2 Lan es		1x GTX		4x GTX on G2	
TE0742*																															
TE0841	B64	48	HR	VC CIOA	B66	16	HP	VC CIOB	B68	18	HP	VC CIOC	B67	50	HP	VC CIOD	1x GTH	1 Lane			B65	8	HR	3.3 V	2x GTH	2 Lan es		1x GTH		4x GTH on G2	
TE0842*																															

I/O resource comparison for all 4x5 modules. There are maximum 4 user supplied I/O voltages (VCCIOA, VCCIOB, VCCIOC and VCCIOD).

*Attention: Maximum supply voltage for HP banks is 1.8V.
Module B2B FPGA-Banks and Voltages

Module Pinout Overview

		JM1					
Direction	Name	Pin	Pin	Name	Direction		
in	PWR_1	1	2	GND			
in	PWR_1	3	4	GROUP7_ETH MDIO0	MST TX	io/no/tx	
in	PWR_1	5	6	GROUP7_ETH MDIO0	MST TX	io/no/tx	
in	NOSEQ	7	8	GND			
in	VCCIOA	9	10	GROUP7_ETH MDIO1	MST RX	io/no/tx	
in	VCCIOA	11	12	GROUP7_ETH MDIO1	MST RX	io/no/tx	
in	PWR_1	13	14	ETH_VIO			
in	PWR_1	15	16	GROUP7_ETH MDIO2	MST TX	io/no/tx	
io/no/tx/out	GROUP3 MIO	SD D3	MST TX	17	18	GROUP7_ETH MDIO2	io/no/tx
io/no/tx/out	GROUP3 MIO	SD D2	MST TX	19	20	GND	
io/no/tx	GROUP3 MIO	SD D1	GND	21	22	GROUP7_ETH MDIO3	MST RX
io/no/tx	GROUP3 MIO	SD D0	GND	23	24	GROUP7_ETH MDIO3	MST RX
io/no/tx/in	GROUP3 MIO	SD CMD	MST RX	25	26	GND	
io/no/tx/in	GROUP3 MIO	SD CLK	MST RX	27	28	SC_EN1	in
				29	30	SC_PG00D	in
				31	32	SC_BOOTMODE	in
io	GROUP1	33	34	GND			
io	GROUP1	35	36	GROUP3		io	
io	GROUP1	37	38	GROUP3		io	
out	PWR_VIO	39	40	GROUP1		io	
io	GROUP1	41	42	GROUP1		io	
io	GROUP1	43	44	GND			
io	GROUP1	45	46	GROUP3		io	
io	GROUP1	47	48	GROUP3		io	
io	GROUP1	49	50	GROUP3		io	
io	GROUP1	51	52	GROUP3		io	
io	GND	53	54	GND			
io	GROUP1	55	56	GROUP1		io	
io	GROUP1	57	58	GROUP1		io	
io	GROUP1	59	60	GROUP1		io	
io	GROUP1	61	62	GROUP1		io	
io	GND	63	64	GND			
io	GROUP1	65	66	GROUP1		io	
io	GROUP1	67	68	GROUP1		io	
io	GROUP1	69	70	GROUP1		io	
io	GROUP1	71	72	GROUP1		io	
io	GROUP1	73	74	GND			
io	GROUP1	75	76	GROUP1		io	
io	GROUP1	77	78	GROUP1		io	
in	PWR_VIO	79	80	GROUP1		io	
io	GROUP1	81	82	GROUP1		io	
io	GROUP1	83	84	GND			
io/no/tx	GROUP3 MIO	UART TX		85	86	GROUP1	io
io/no	GROUP3 MIO			87	88	GROUP1	io
in	FIADJEL	89	90	GND			
io/no	GROUP3 MIO			91	92	GROUP3 MIO	UART RX
io/no	GROUP3 MIO			93	94	GROUP1	io
io/no	GROUP3 MIO			95	96	GROUP1	io
io/no	GROUP3 MIO			97	98	GROUP1	io
io/no	GROUP3 MIO			99	100	GROUP1	io

Positions are displayed as Top View

Legend
Power-VCC
GROUP1
GROUP2
GROUP3
GROUP4
GROUP5
GROUP6
GROUP7
Special
VCCIOA
VCCIOB
VCCIOD

Direction	Name	JM2	Pin	Name	Direction
in	VCCIOB	1	2	PWR_1	in
in	VCCIOB	3	4	PWR_1	in
in	VCCIOB	5	6	PWR_1	in
in	VCCIOB	7	8	PWR_1	in
in	VCCIOB	9	10	PWR_VIO	out
io	GROUP3	11	12	PWR_VIO	out
io	GROUP3	13	14	GROUP3	io
io	GROUP3	15	16	GROUP3	io
io	GROUP3	17	18	SC_WST	in
io	PWR_VIO	19	20	GND	
io	GROUP3	21	22	GROUP3	io
io	GROUP3	23	24	GROUP3	io
io	GROUP3	25	26	GROUP3	io
io	GROUP3	27	28	GROUP3	io
io	GND	29	30	GND	
io	GROUP3	31	32	GROUP4	io
io	GROUP3	33	34	GROUP4	io
io	GROUP3	35	36	GROUP4	io
io	GROUP3	37	38	GROUP4	io
io	GND	39	40	GND	
io	GROUP4	41	42	GROUP4	io
io	GROUP4	43	44	GROUP4	io
io	GROUP4	45	46	GROUP4	io
io	GROUP4	47	48	GROUP4	io
io	GROUP4	49	50	GND	
io	GROUP4	51	52	GROUP4	io
io	GROUP4	53	54	GROUP4	io
io	GROUP4	55	56	GROUP4	io
io	GROUP4	57	58	GROUP4	io
io	GND	59	60	GND	
io	GROUP4	61	62	GROUP4	io
io	GROUP4	63	64	GROUP4	io
io	GROUP4	65	66	GROUP4	io
io	GROUP4	67	68	GROUP4	io
io	GND	69	70	GND	
io	GROUP4	71	72	GROUP4	io
io	GROUP4	73	74	GROUP4	io
io	GROUP4	75	76	GROUP4	io
io	GROUP4	77	78	GROUP4	io
io	GND	79	80	GND	
io	GROUP4	81	82	GROUP4	io
io	GROUP4	83	84	GROUP4	io
io	GROUP4	85	86	GROUP4	io
io	GROUP4	87	88	GROUP4	io
io	GROUP4	89	90	GND	
io	PWR_VIO	91	92	GROUP4	io
in	TMS	93	94	GROUP4	io
in	TDO	95	96	GROUP4	io
out	TDO	97	98	GROUP4	io
in	TCK	99	100	GROUP4	io

Module basic power and group pin assignment, recommended to verify with Schematics

Carrier Board Power Connection Table

IO Voltage		B2B Connector		Carrier Boards													
Name	Direction*	JB1	JB2	TE0701		TE0703 Rev01 - Rev04		TE0703 Rev 05		TE0705		TE0706		TEBA0841		TEBA0841 REV01	
		Pin	Pin	Schematic Name	Value, Option, Comp.	Schematic Name	Value, Option, Comp.	Schematic Name	Value,Option, Comp.	Schematic Name	Value, Option, Comp.	Schematic Name	Value,Option, Comp.	Schematic Name	Value,Option, Comp.	Schematic Name	Value,Option, Comp.
PWR_1	out	2,4,6	1,3,5,7	5V0	5V	3.3V	3.3V	3.3V	3.3V	5V0	5V	3.3V	3.3V	3.3V	use ext. 3.3V power supply	3.3V	use ext. 3.3V power supply
VCCIOA	out	10,12		VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO35	R23M3. 3VOUT J1B-B1	VCCIOA	J5M3. 3VOUT, M1. 8VOUT R23M3. 3VOUT J1-B1	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO35	R20->M3. 3VOUT/J6B-B32	VCCIOA	J26 M1.8VOUT, 2.5V, 3.3V_OUT J20-6,J20-45	VCCIOA	J26 M1.8VOUT, 2.5V, 3.3V_OUT J20-6,J20-45

VCCIOD	out		8,10	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO13	R26M3. 3VOUT J2B-B1	VCCIOD	J10M3. 3VOUT, M1. 8VOUT R26M3. 3VOUT J2B-B1	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO13	R22->M3. 3VOUT/J6B- B1	VCCIOD	J27 M1.8VOUT, 2.5V, 3.3V_OUT J17-6,J17-45	VCCIOD	J27 M1.8VOUT, 2.5V, 3.3V_OUT J17-6,J17-45
PWR_2	out	14,16		3V3IN	3.3V	3.3V	3.3V	3.3V	3.3V	3V3IN	3.3V	3.3V	3.3V	3.3V	use ext. 3.3V power supply	3.3V	use ext. 3.3V power supply
VCCIOB	out		2,4	no name / VIOTA	FMC_VA DJ 2V5 3.3VOUT	VCCIO34	J5M3. 3VOUT J1B-B32	VCCIOB	J8M3.3VOUT, M1.8VOUT J2B-B32	VIOTB	FMC_VA DJ 2V5 3.3VOUT	1.8V	1.8V	VCCIOB	J5 M1.8VOUT, 2.5V, 3.3V_OUT	VCCIOB	NC
VCCIOC	out		6	no name / VIOTA	FMC_VA DJ 2V5 3.3VOUT	VCCIO33	R25M3. 3VOUT J2B-B32	VCCIOC	J9M3. 3VOUT, M1. 8VOUT R25M3. 3VOUT J2B-B32	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO33	R21->M3. 3VOUT	VCCIOC	J6 M1.8VOUT, 2.5V, 3.3V_OUT	VCCIOC	NC
PWR_M1	in		9,11	3.3 VOUT	3.3V	3.3 VOUT	3.3V	M3. 3VOUT	3.3V	3.3 VOUT	3.3V	M3. 3VOUT	3.3V	3.3 V_OUT	3.3V	3.3 V_OUT	3.3V
PWR_M2	in	40		VIOB	1.8V	M1. 8VOUT	1.8V	M1. 8VOUT	1.8V	VIOB	1.8V	M1. 8VOUT	1.8V	M1. 8VOUT	1.8V	M1. 8VOUT	1.8V
PWR_M3	in		20	NC		NC		NC		NC		NC			NC		NC
PWR_VBAT	out	80		VBAT	B1	VBAT	J7	VBAT	J7	NC		VBAT	J9	VBAT	NC	VBAT	NC
PWR_JTAG	in		92	VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG	NC

Power comparison of all 4x5 carrier boards. ***Power direction based on carrier boards view.** There are 4 variable user supplied I/O voltages (VCCIOA, VCCIOB, VCCIOC and VCCIOD). PWR_1 and PWR_2 are fixed from carrier boards. PWR_M1 and PWR_M2 normally use default value from module. NC=Not Connected

Attention: On some carrier boards the user supplied I/O voltages are connected together (red colored schematic names).

Power Pin Connection on different Carrierboards

Carrier Pinout Overview

Positions are displayed
as
Top View

JB1					
Direction	Name	Pin	Pin	Name	Direction
out	PWR_1	2	1	GND	
out	PWR_1	4	3	ID	
out	PWR_1	6	5	ID	
io	NOSQL	8	7	GND	
out	VCCIOA	10	9	ID	
out	VCCIOA	12	11	ID	
out	PWR_2	14	13	ETH_VCC	
out	PWR_2	16	15	ID	
	ID	18	17	ID	
	ID	20	19	GND	
	ID	22	21	ID	
	ID	24	23	ID	
	ID	26	25	GND	
	ID	28	27	SC_EN1	out
	GND	30	29	SC_PGOOD	io
	ID	32	31	SC_BOOTMODE	out
	ID	34	33	GND	
	ID	36	35	ID	
	ID	38	37	ID	
in	PWR_M1	40	39	ID	
	ID	42	41	ID	
	ID	44	43	GND	
	ID	46	45	ID	
	ID	48	47	ID	
	ID	50	49	ID	
	ID	52	51	ID	
	GND	54	53	GND	
	ID	56	55	ID	
	ID	58	57	ID	
	ID	60	59	ID	
	ID	62	61	ID	
	GND	64	63	GND	
	ID	66	65	ID	
	ID	68	67	ID	
	ID	70	69	ID	
	ID	72	71	ID	
	GND	74	73	GND	
	ID	76	75	ID	
	ID	78	77	ID	
out	PWR_VCC1	80	79	ID	
	ID	82	81	ID	
	ID	84	83	GND	
in	IO/UART TX	86	85	ID	
	ID	88	87	ID	
out	JTAGSEL	90	89	GND	
	ID	92	91	IO/UART RX	out
	ID	94	93	ID	
	ID	96	95	ID	
	ID	98	97	ID	
	ID	100	99	ID	

JB2					
Direction	Name	Pin	Pin	Name	Direction
out	VCCIOB	2	1	PWR_1	out
out	VCCIOB	4	3	PWR_1	out
out	VCCIOB	6	5	PWR_1	out
out	VCCIOB	8	7	PWR_1	out
out	VCCIOB	10	9	PWR_M1	in
	ID	12	11	PWR_M1	in
	ID	14	13	ID	
	ID	16	15	ID	
	ID	18	17	SC_nRST	out
	PWR_M1n	20	19	GND	
	ID	22	21	ID	
	ID	24	23	ID	
	ID	26	25	ID	
	ID	28	27	ID	
	NC/GND	30	29	GND	
	ID	32	31	ID	
	ID	34	33	ID	
	ID	36	35	ID	
	ID	38	37	ID	
	GND	40	39	GND	
	ID	42	41	ID	
	ID	44	43	ID	
	ID	46	45	ID	
	ID	48	47	ID	
	GND	50	49	GND	
	ID	52	51	ID	
	ID	54	53	ID	
	ID	56	55	ID	
	ID	58	57	ID	
	GND	60	59	GND	
	ID	62	61	ID	
	ID	64	63	ID	
	ID	66	65	ID	
	ID	68	67	ID	
	GND	70	69	GND	
	ID	72	71	ID	
	ID	74	73	ID	
	ID	76	75	ID	
	ID	78	77	ID	
	GND	80	79	GND	
	ID	82	81	ID	
	ID	84	83	ID	
	ID	86	85	ID	
	ID	88	87	ID	
	ID	90	89	GND	
in	PWR_ITAG	92	91	ID	
out	TMS	94	93	ID	
out	TDI	96	95	ID	
	TDO	98	97	ID	
out	TCK	100	99	ID	

Positions are displayed
as
Top View

Legend	
	Power-VCC
	Power-GND
	Special
	IO / Special
	VCCIOA
	VCCIOB
	VCCIOB

Carrierboard basic power and group pin assignment (Top View), recommended to verify with Schematics

4x5 Module Controller IOs

Name	Module B2B Pin	Carrier B2B Pin	Direction (Module view)	Description	Recommendation
JTAGSEL	JM1-89	JB1-90	in	JTAG Chain multiplexer. Low FPGA, High CPLD. For module with CPLD only.	Connect Pulldown on carrier. DIP switch possible.
SC_EN1	JM1-28	JB1-27	in	Module power. Set high to enable module power. Note: Power management depends on module. Sometimes this is a only used as Power ON Reset like SC_nRST	Connect Pullup on carrier. DIP switch possible
SC_NO SEQ	JM1-7	JB1-8	in / inout	Module Power management. Set high to disable CPLD power management. Note: Power management depends on module and not all modules support extended power management with CPLD.	Connect Pullup or force to GND over zero ohm resistor on carrier. DIP switch possible.
SC_PG OOD	JM1-30	JB1-29	out / inout	Power Good signal. Is Low, if SC_EN1 is set to zero or if power is not ready, otherwise high impedance output. Note: Power management depends on module. On newer Firmware SC_PGOOD will be used as Additionally Boot Mode Pin.	Connect Pullup on carrier. Do not use this signal to enable FPGA Bank voltages. It's only for monitoring. To Enable FPGA Banks, use 3.3V(PWR_M1) or 1.8V(PWR_M2) module output.

SC_BO OTMODE	JM1-32	JB1-31	in	Boot Mode selection Pin for Zynq module only. Default low for primary SD boot and high for primary QSPI boot. Note: Depends also on module CPLD firmware	Connect Pullup on carrier. DIP switch possible.
SC_nRST	JM2-18	JB2-17	in	Low active module reset. Pin force Power one reset on FPGA /SoC. Note: Depending from module CPLD or voltage supervisor is used.	Connect Pullup on carrier. DIP switch possible.

- Controller IOs are 3.3V IOs

 It's planned to use SC_PGOOD also as additional Boot Mode Pin (Pin is bidirectional, pull up or force to zero), to additionally set JTAG only boot mode (to avoid programming problems with some vivado versions, see: [AR#00002 - QSPI Programming issues](#)). Current state of CPLD Redesigns: [AVN-20220506 4 x 5 modules controller IOs redefinition and CPLD updates](#)

4x5 Module Controller IOs

Remove 4x5 module

[4 x 5 SoMs Handling and Usage Precautions](#)

Compatibility Guide

Ethernet LED'S

TE07xx 4x5 modules do not have dedicated pins for the Ethernet PHY LED's, also there are no fix pins on the baseboards for the PHY LED's or any other LED's.

If Ethernet JACKs on Baseboard have LED's then those should be connected to some free PL I/O pins, and then routed in the FPGA logic from the PHY to the I/O Pin in the B2B Connector.

Recommended connections would be to use JM2.89 and JM2.100 for the PHY LED's, those positions support baseboard ETH LED's for TE0701 and TE0703 and TE0706.

JM2 pins 1, 3 (TE0720 Bank 34 Voltage)

- To be compatible with TE0720 JM2 pins 1,3 must be connected to some valid VCCIO voltage.
- When JM2 pins 1, 3 are not powered TE0720 would not boot, and may not be recognized in JTAG chain as well.
- When those pins are not used on the module (TE0710) then to be compatible with TE0720:
- Solution A: connect to 3.3V out from the module, option compatible to all modules except those with HP banks
- Solution B: connect to 1.8V out from the module, option compatible with all modules.

Carrier Board Checklist

Schematic Checklist

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1	Are B2B pin numbers on the connectors mirrored compared to the module pin numbers?	As B2B connectors are "unisex" type they do mirror pin numbers when connecting. That is pin1 connects to pin2, and pin2 to pin1, etc.
2	Are B2B connectors named JB1, JB2, JB3?	This is not a hard requirement, but it helps to use the same identifiers.
3	Are all GND pins connected to a common ground net?	
4	Are all VIN pins connected together?	
5	Is JB2 pin 92 pin used as VREF for the JTAG interface?	for future compatibility only, currently all modules have 3.3V JTAG
6	For 7 Series Zynq module only: Are external circuits/buffers connecting to MIO bank 1 pins powered from JB1 pin 40?	JB1 pins 18, 20, 22, 24, 26, 28 use voltage at pin 40 as VCCIO. Currently it is 1.8V for 4x5 Zynq Modules. Note: Different Power supply on TE0820(3.3V MIO Bank) and normal FPGA modules(check schematics)

PCB Checklist

1	Are mounting holes placed properly?	Four Mounting holes should always be used. They are required for mounting screws and for module extraction. The mounting holes will also help in dissipating some heat from the module to the carrier board PCB. Four holes with a 3.2mm diameter should be placed exactly at the corners of a 34mm by 44mm rectangle.
2	Are B2B headers properly placed?	B2B headers must be placed and aligned very precisely or the module will not align correctly (in the worst case module insertion could destroy the connectors or the PCB). The B2B headers should be locked on the PCB, and it is recommended that the position and placement be checked against placement dimensions before submitting the PCB files.
3	Are B2B headers rotated properly?	As B2B header pin numbers differ from module to the carrier (swap of odd and even numbers), it is recommended that the rotation is checked in the PCB design.
4	Height clearance below module	Components can be placed below the module but height clearance rules must be obeyed.
5	Power dissipation of components below module	It is not recommended to place any components with high power dissipation below the module, as there will be almost no airflow below the module.

Visual Check of Module placement

It is highly recommended to use the Base board Template designs as a starting point for new PCB designs. If that is not possible, then adding linear dimensions in the design helps to check that all connectors and mounting holes are properly placed.



This placement is same for all 4x5 Modules!

Connector numbers as on base! (pin JB1.1 on base would mate to pin JM1.2 on module).