

4 x 5 SoM Integration Guide

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Power and Signal Pin Assignment

How to Use This Guide

- This guide is split into two tables:
 - Module Power Connection Table** section shows the power source of the different FPGA banks and components of the different module boards as well as the power and group location on the B2B connectors of the module site.
 - Carrier Board Power Connection Table** section shows the power source of the B2B connectors with pins, schematic names and available options of the different carrier boards as well as the power location on the B2B connectors of the carrier site.
 - The PCBs have fixed and variable user supplied I/O voltage pins. Variable power supply pins are colored in four groups (VCCIOA, VCCIOB, VCCIOC and VCCIOD).
- Find your module model on the **Module Power Connection Table** and check the power supply of the different FPGA banks.
 - If the power supply is variable(colored), go to the **Carrier Board Power Connection Table** and see how it's connected on your carrier board. Often the power source can be selected by jumper, resistor or variable used from other connector pin of the carrier board. So use the schematic name or the component designator from the table to search for the available options in the PCB schematics or TRM.
 - Additional Master Pinout Viewer/XDC-Generator is available on [Trenz Electronic Download - Pinout](#)

Module Power Connection Table

Group	1				2				3				4				5				6				7				8	9	special
Module Model	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage			
TE0710	B15	48	HR	VC CIOA	-	-	-	-	-	-	-	-	B34	50	HR	VC CIOD	B16	6	HR	3.3 V	B14	8	HR	3.3 V	2x 100Mb it ETH						
TE0711	B15	48	HR	VC CIOA	B34	36	HR	VC CIOB	B14	18	HR	3.3 V	B35	50	HR	VC CIOD	B16	6	HR	1.8 V	B14	8	HR	3.3 V	B34	8	HR	VC CIOB	B34(4)	USB	
TE0712	B16	48	HR	VC CIOA	B13	20	HR	VC CIOB	B14	18	HR	3.3 V	B15	50	HR	VC CIOD	B13	6	HR	VC CIOB	B14	8	HR	3.3 V	1x 100Mb it ETH / B13	4	HR	VC CIOB		B14	4x GTP on G2
TE0713																															4x GTP on G2
TE0715 with Z-7015 Z-7012S	B13	48	HR	VC CIOA	B34	16	HR	VC CIOC	B34	18	HR	VC CIOC	B35	50	HR	VC CIOD	B5 01	6	MIO	1.8 V	B500	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTP on G2

TE0715 with Z-7030	B13	48	HR	VC CIOA	B34	16	HP	VC CIOC	B34	18	HP	VC CIOC	B35	50	HP	VC CIOD	B5 01	6	MIO	1.8 V	B500	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTP on G2
TE0720	B35	48	HR	VC CIOA	B34	36	HR	VC CIOB	B33	18	HR	VC CIOC	B13	50	HR	VC CIOD	B5 01	6	MIO	1.8 V	B500	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	
TE0820*	B66	48	HP	VC CIOA	B65	16	HP	VC CIOC	B65	18	HP	VC CIOC	B64	50	HP	VC CIOD	B5 01	6	MIO	3.3 V	B5 01	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTR on G2
TE0821*	B26	48	HD	VC CIOA	B65	16	HP	VC CIOC	B65	18	HP	VC CIOC	B24	48	HD	VC CIOD	B5 01	6	MIO	3.3 V	B5 01	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTR on G2
TE0823*	B66	48	HP	VC CIOA	B65	16	HP	VC CIOC	B65	18	HP	VC CIOC	B64	50	HP	VC CIOD	B5 01	6	MIO	3.3 V	B5 01	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTR on G2
TE0741	B13	48	HR	VC CIOA	B16	16	HR	VC CIOB	B15	18	HR	VC CIOC	B12	50	HR	VC CIOD	1x GTX	1 Lane			B14	8	HR	3.3 V	2x GTX	2 Lan es		1x GTX		4x GTX on G2	
TE0742*																															
TE0841	B64	48	HR	VC CIOA	B66	16	HP	VC CIOB	B68	18	HP	VC CIOC	B67	50	HP	VC CIOD	1x GTH	1 Lane			B65	8	HR	3.3 V	2x GTH	2 Lan es		1x GTH		4x GTH on G2	
TE0842*																															

I/O resource comparison for all 4x5 modules. There are maximum 4 user supplied I/O voltages (VCCIOA, VCCIOB, VCCIOC and VCCIOD).

*Attention: Maximum supply voltage for HP banks is 1.8V.
Module B2B FPGA-Banks and Voltages

Module Pinout Overview

JMS									
Direction	Name	Pin	Name	Pin	Direction	Name	Pin	Name	Direction
io/tx/tx	MST TX	1	ETH SMI	GROUP1	1	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	2	ETH SMI	GROUP1	2	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	3	ETH SMI	GROUP1	3	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	4	ETH SMI	GROUP1	4	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	5	ETH SMI	GROUP1	5	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	6	ETH SMI	GROUP1	6	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	7	ETH SMI	GROUP1	7	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	8	ETH SMI	GROUP1	8	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	9	ETH SMI	GROUP1	9	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	10	ETH SMI	GROUP1	10	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	11	ETH SMI	GROUP1	11	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	12	ETH SMI	GROUP1	12	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	13	ETH SMI	GROUP1	13	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	14	ETH SMI	GROUP1	14	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	15	ETH SMI	GROUP1	15	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	16	ETH SMI	GROUP1	16	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	17	ETH SMI	GROUP1	17	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	18	ETH SMI	GROUP1	18	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	19	ETH SMI	GROUP1	19	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	20	ETH SMI	GROUP1	20	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	21	ETH SMI	GROUP1	21	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	22	ETH SMI	GROUP1	22	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	23	ETH SMI	GROUP1	23	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	24	ETH SMI	GROUP1	24	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	25	ETH SMI	GROUP1	25	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	26	ETH SMI	GROUP1	26	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	27	ETH SMI	GROUP1	27	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	28	ETH SMI	GROUP1	28	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	29	ETH SMI	GROUP1	29	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	30	ETH SMI	GROUP1	30	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	31	ETH SMI	GROUP1	31	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	32	ETH SMI	GROUP1	32	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	33	ETH SMI	GROUP1	33	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	34	ETH SMI	GROUP1	34	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	35	ETH SMI	GROUP1	35	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	36	ETH SMI	GROUP1	36	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	37	ETH SMI	GROUP1	37	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	38	ETH SMI	GROUP1	38	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	39	ETH SMI	GROUP1	39	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	40	ETH SMI	GROUP1	40	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	41	ETH SMI	GROUP1	41	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	42	ETH SMI	GROUP1	42	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	43	ETH SMI	GROUP1	43	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	44	ETH SMI	GROUP1	44	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	45	ETH SMI	GROUP1	45	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	46	ETH SMI	GROUP1	46	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	47	ETH SMI	GROUP1	47	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	48	ETH SMI	GROUP1	48	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	49	ETH SMI	GROUP1	49	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	50	ETH SMI	GROUP1	50	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	51	ETH SMI	GROUP1	51	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	52	ETH SMI	GROUP1	52	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	53	ETH SMI	GROUP1	53	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	54	ETH SMI	GROUP1	54	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	55	ETH SMI	GROUP1	55	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	56	ETH SMI	GROUP1	56	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	57	ETH SMI	GROUP1	57	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	58	ETH SMI	GROUP1	58	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	59	ETH SMI	GROUP1	59	MST RX	ETH SMI	GROUP1	io/tx/tx
io/tx/tx	MST TX	60	ETH SMI	GROUP1	60	MST RX	ETH SMI	GROUP1	io/tx/tx

JMS									
Direction	Name	Pin	Name	Pin	Direction	Name	Pin	Name	Direction
in	PWR_1	1	GND	2	in	PWR_1	3	GND	4
in	PWR_1	3	GROUP1	ETH MDIO0	MST TX	io/tx/tx	5	GROUP1	ETH MDIO0
in	PWR_1	5	GROUP1	ETH MDIO0	MST TX	io/tx/tx	6	GROUP1	ETH MDIO0
in	NOSEQ	7	GND	8	in	NOSEQ	9	GND	10
in	VCCIOA	11	GROUP1	ETH MDIO1	MST RX	io/tx/tx	12	GROUP1	ETH MDIO1
in	VCCIOA	13	GROUP1	ETH MDIO1	MST RX	io/tx/tx	14	GROUP1	ETH MDIO1
in	PWR_1	15	GROUP1	ETH MDIO2	MST TX	io/tx/tx	16	GROUP1	ETH MDIO2
in	PWR_1	17	GROUP1	ETH MDIO2	MST TX	io/tx/tx	18	GROUP1	ETH MDIO2
io/tx/tx	GROUP1	MDIO	SD D3	MST TX	19	20	GROUP1	ETH MDIO3	MST TX
io/tx/tx	GROUP1	MDIO	SD D2	MST TX	21	22	GROUP1	ETH MDIO3	MST TX
io/tx/tx	GROUP1	MDIO	SD D1	GND	23	24	GROUP1	ETH MDIO3	MST RX
io/tx/tx	GROUP1	MDIO	SD D0	GND	25	26	GROUP1	ETH MDIO3	MST RX
io/tx/tx	GROUP1	MDIO	SD CMD	MST RX	27	28	GROUP1	ETH MDIO3	MST RX
io/tx/tx	GROUP1	MDIO	SD CLK	MST RX	29	30	GROUP1	ETH MDIO3	MST RX
in	GROUP1	31	32	SC BOOTMODE	in	GROUP1	33	34	SC BOOTMODE
in	GROUP1	35	36	GROUP1	io	GROUP1	37	38	GROUP1
in	GROUP1	39	40	GROUP1	io	GROUP1	41	42	GROUP1
in	GROUP1	43	44	GROUP1	io	GROUP1	45	46	GROUP1
in	GROUP1	47	48	GROUP1	io	GROUP1	49	50	GROUP1
in	GROUP1	51	52	GROUP1	io	GROUP1	53	54	GROUP1
in	GROUP1	55	56	GROUP1	io	GROUP1	57	58	GROUP1
in	GROUP1	59	60	GROUP1	io	GROUP1	61	62	GROUP1
in	GROUP1	63	64	GROUP1	io	GROUP1	65	66	GROUP1
in	GROUP1	67	68	GROUP1	io	GROUP1	69	70	GROUP1
in	GROUP1	71	72	GROUP1	io	GROUP1	73	74	GROUP1
in	GROUP1	75	76	GROUP1	io	GROUP1	77	78	GROUP1
in	GROUP1	79	80	GROUP1	io	GROUP1	81	82	GROUP1
in	GROUP1	83	84	GROUP1	io	GROUP1	85	86	GROUP1
io/tx/tx	GROUP1	MDIO	MDIO	MDIO	io	GROUP1	87	88	GROUP1
io/tx/tx	GROUP1	MDIO	MDIO	MDIO	io	GROUP1	89	90	GROUP1
io/tx/tx	GROUP1	MDIO	MDIO	MDIO	io	GROUP1	91	92	GROUP1
io/tx/tx	GROUP1	MDIO	MDIO	MDIO	io	GROUP1	93	94	GROUP1
io/tx/tx	GROUP1	MDIO	MDIO	MDIO	io	GROUP1	95	96	GROUP1
io/tx/tx	GROUP1	MDIO	MDIO	MDIO	io	GROUP1	97	98	GROUP1
io/tx/tx	GROUP1	MDIO	MDIO	MDIO	io	GROUP1	99	100	GROUP1

Positions are displayed as Top View

Legend	
Power-VCC	GROUP1
Power-GND	GROUP2
Special	GROUP3
VCCIOA	GROUP4
VCCIOB	GROUP5
VCCIOD	GROUP6

JMS									
Direction	Name	Pin	Name	Pin	Direction	Name	Pin	Name	Direction
in	VCCIOB	1	PWR_1	2	in	VCCIOB	3	PWR_1	4
in	VCCIOB	5	PWR_1	6	in	VCCIOB	7	PWR_1	8
in	VCCIOB	9	PWR_1	10	in	VCCIOB	11	PWR_1	12
in	VCCIOB	13	PWR_1	14	in	VCCIOB	15	PWR_1	16
in	VCCIOB	17	PWR_1	18	in	VCCIOB	19	PWR_1	20
in	VCCIOB	21	PWR_1	22	in	VCCIOB	23	PWR_1	24
in	VCCIOB	25	PWR_1	26	in	VCCIOB	27	PWR_1	28
in	VCCIOB	29	PWR_1	30	in	VCCIOB	31	PWR_1	32
in	VCCIOB	33	PWR_1	34	in	VCCIOB	35	PWR_1	36
in	VCCIOB	37	PWR_1	38	in	VCCIOB	39	PWR_1	40
in	VCCIOB	41	PWR_1	42	in	VCCIOB	43	PWR_1	44
in	VCCIOB	45	PWR_1	46	in	VCCIOB	47	PWR_1	48
in	VCCIOB	49	PWR_1	50	in	VCCIOB	51	PWR_1	52
in	VCCIOB	53	PWR_1	54	in	VCCIOB	55	PWR_1	56
in	VCCIOB	57	PWR_1	58	in	VCCIOB	59	PWR_1	60
in	VCCIOB	61	PWR_1	62	in	VCCIOB	63	PWR_1	64
in	VCCIOB	65	PWR_1	66	in	VCCIOB	67	PWR_1	68
in	VCCIOB	69	PWR_1	70	in	VCCIOB	71	PWR_1	72
in	VCCIOB	73	PWR_1	74	in	VCCIOB	75	PWR_1	76
in	VCCIOB	77	PWR_1	78	in	VCCIOB	79	PWR_1	80
in	VCCIOB	81	PWR_1	82	in	VCCIOB	83	PWR_1	84
in	VCCIOB	85	PWR_1	86	in	VCCIOB	87	PWR_1	88
in	VCCIOB	89	PWR_1	90	in	VCCIOB	91	PWR_1	92
in	VCCIOB	93	PWR_1	94	in	VCCIOB	95	PWR_1	96
in	VCCIOB	97	PWR_1	98	in	VCCIOB	99	PWR_1	100

Module basic power and group pin assignment, recommended to verify with Schematics

Carrier Board Power Connection Table

IO Voltage		B2B Connector		Carrier Boards													
Name	Direction*	JB1	JB2	TE0701		TE0703 Rev01 - Rev04		TE0703 Rev 05		TE0705		TE0706		TEBA0841		TEBA0841 REV01	
		Pin	Pin	Schematic Name	Value, Option, Comp.	Schematic Name	Value, Option, Comp.	Schematic Name	Value,Option, Comp.	Schematic Name	Value, Option, Comp.	Schematic Name	Value,Option, Comp.	Schematic Name	Value,Option, Comp.	Schematic Name	Value,Option, Comp.
PWR_1	out	2,4,6	1,3,5,7	5V0	5V	3.3V	3.3V	3.3V	3.3V	5V0	5V	3.3V	3.3V	3.3V	use ext. 3.3V power supply	3.3V	use ext. 3.3V power supply
VCCI OA	out	10,12		VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO35	R23M3. 3VOUT J1B-B1	VCCIOA	J5M3. 3VOUT, M1. 8VOUT R23M3. 3VOUT J1-B1	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO35	R20->M3. 3VOUT/J6B-B32	VCCIOA	J26 M1.8VOUT, 2.5V, 3.3V_OUT J20-6,J20-45	VCCIOA	J26 M1.8VOUT, 2.5V, 3.3V_OUT J20-6,J20-45

VCCIOD	out		8,10	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO13	R26M3. 3VOUT J2B-B1	VCCIOD	J10M3. 3VOUT, M1. 8VOUT R26M3. 3VOUT J2B-B1	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO13	R22->M3. 3VOUT/J6B- B1	VCCIOD	J27 M1.8VOUT, 2.5V, 3.3V_OUT J17-6,J17-45	VCCIOD	J27 M1.8VOUT, 2.5V, 3.3V_OUT J17-6,J17-45
PWR_2	out	14,16		3V3IN	3.3V	3.3V	3.3V	3.3V	3.3V	3V3IN	3.3V	3.3V	3.3V	3.3V	use ext. 3.3V power supply	3.3V	use ext. 3.3V power supply
VCCIOB	out		2,4	no name / VIOTA	FMC_VA DJ 2V5 3.3VOUT	VCCIO34	J5M3. 3VOUT J1B-B32	VCCIOB	J8M3.3VOUT, M1.8VOUT J2B-B32	VIOTB	FMC_VA DJ 2V5 3.3VOUT	1.8V	1.8V	VCCIOB	J5 M1.8VOUT, 2.5V, 3.3V_OUT	VCCIOB	NC
VCCIOC	out		6	no name / VIOTA	FMC_VA DJ 2V5 3.3VOUT	VCCIO33	R25M3. 3VOUT J2B-B32	VCCIOC	J9M3. 3VOUT, M1. 8VOUT R25M3. 3VOUT J2B-B32	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO33	R21->M3. 3VOUT	VCCIOC	J6 M1.8VOUT, 2.5V, 3.3V_OUT	VCCIOC	NC
PWR_M1	in		9,11	3.3 VOUT	3.3V	3.3 VOUT	3.3V	M3. 3VOUT	3.3V	3.3 VOUT	3.3V	M3. 3VOUT	3.3V	3.3 V_OUT	3.3V	3.3 V_OUT	3.3V
PWR_M2	in	40		VIOB	1.8V	M1. 8VOUT	1.8V	M1. 8VOUT	1.8V	VIOB	1.8V	M1. 8VOUT	1.8V	M1. 8VOUT	1.8V	M1. 8VOUT	1.8V
PWR_M3	in		20	NC		NC		NC		NC		NC			NC		NC
PWR_VBAT	out	80		VBAT	B1	VBAT	J7	VBAT	J7	NC		VBAT	J9	VBAT	NC	VBAT	NC
PWR_JTAG	in		92	VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG	NC

Power comparison of all 4x5 carrier boards. ***Power direction based on carrier boards view.** There are 4 variable user supplied I/O voltages (VCCIOA, VCCIOB, VCCIOC and VCCIOD). PWR_1 and PWR_2 are fixed from carrier boards. PWR_M1 and PWR_M2 normally use default value from module. NC=Not Connected

Attention: On some carrier boards the user supplied I/O voltages are connected together (red colored schematic names).

Power Pin Connection on different Carrierboards

Carrier Pinout Overview

J1					J2				
Direction	Name	Pin	Pin	Direction	Direction	Name	Pin	Pin	Direction
out	PWR_1	2	1	IO	out	PWR_1	2	1	IO
out	PWR_1	4	4	IO	out	PWR_1	4	4	IO
out	PWR_1	6	5	IO	out	PWR_1	6	5	IO
to	NOISEL	8	7	IO	to	NOISEL	8	7	IO
out	PWR_2	10	9	IO	out	PWR_2	10	9	IO
out	VCCIOA	12	11	IO	out	VCCIOA	12	11	IO
out	PWR_3	14	13	IO	out	PWR_3	14	13	IO
out	PWR_3	15	15	IO	out	PWR_3	15	15	IO
		18	17	IO			18	17	IO
		20	19	IO			20	19	IO
		22	21	IO			22	21	IO
		24	23	IO			24	23	IO
		26	25	IO			26	25	IO
		28	27	IO			28	27	IO
		30	29	IO			30	29	IO
		32	31	IO			32	31	IO
		34	33	IO			34	33	IO
		36	35	IO			36	35	IO
		38	37	IO			38	37	IO
in	PWR_M1	40	39	IO	in	PWR_M1	40	39	IO
		42	41	IO			42	41	IO
		44	43	IO			44	43	IO
		46	45	IO			46	45	IO
		48	47	IO			48	47	IO
		50	49	IO			50	49	IO
		52	51	IO			52	51	IO
		54	53	IO			54	53	IO
		56	55	IO			56	55	IO
		58	57	IO			58	57	IO
		60	59	IO			60	59	IO
		62	61	IO			62	61	IO
		64	63	IO			64	63	IO
		66	65	IO			66	65	IO
		68	67	IO			68	67	IO
		70	69	IO			70	69	IO
		72	71	IO			72	71	IO
		74	73	IO			74	73	IO
		76	75	IO			76	75	IO
		78	77	IO			78	77	IO
out	PWR_M2	80	79	IO	out	PWR_M2	80	79	IO
		82	81	IO			82	81	IO
		84	83	IO			84	83	IO
in	IO/UART TX	86	85	IO	in	IO/UART TX	86	85	IO
		88	87	IO			88	87	IO
out	ITAGSEL	90	89	IO	out	ITAGSEL	90	89	IO
		92	91	IO			92	91	IO
		94	93	IO			94	93	IO
		96	95	IO			96	95	IO
		98	97	IO			98	97	IO
		100	99	IO			100	99	IO

Legend

Power VCC

Power GND

Special

IO / Special

VCCIOA

VCCIOB

VCCIOD

Positions are displayed as Top View

J3					J4				
Direction	Name	Pin	Pin	Direction	Direction	Name	Pin	Pin	Direction
out	VCCIOD	2	1	IO	out	PWR_1	2	1	IO
out	VCCIOD	4	4	IO	out	PWR_1	4	4	IO
out	VCCIOD	6	5	IO	out	PWR_1	6	5	IO
out	VCCIOD	8	7	IO	out	PWR_1	8	7	IO
out	VCCIOD	10	9	IO	in	PWR_M1	10	9	IO
		12	11	IO			12	11	IO
		14	13	IO			14	13	IO
		15	15	IO			15	15	IO
		18	17	IO			18	17	IO
		20	19	IO			20	19	IO
		22	21	IO			22	21	IO
		24	23	IO			24	23	IO
		26	25	IO			26	25	IO
		28	27	IO			28	27	IO
		30	29	IO			30	29	IO
		32	31	IO			32	31	IO
		34	33	IO			34	33	IO
		36	35	IO			36	35	IO
		38	37	IO			38	37	IO
		40	39	IO			40	39	IO
		42	41	IO			42	41	IO
		44	43	IO			44	43	IO
		46	45	IO			46	45	IO
		48	47	IO			48	47	IO
		50	49	IO			50	49	IO
		52	51	IO			52	51	IO
		54	53	IO			54	53	IO
		56	55	IO			56	55	IO
		58	57	IO			58	57	IO
		60	59	IO			60	59	IO
		62	61	IO			62	61	IO
		64	63	IO			64	63	IO
		66	65	IO			66	65	IO
		68	67	IO			68	67	IO
		70	69	IO			70	69	IO
		72	71	IO			72	71	IO
		74	73	IO			74	73	IO
		76	75	IO			76	75	IO
		78	77	IO			78	77	IO
		80	79	IO			80	79	IO
		82	81	IO			82	81	IO
		84	83	IO			84	83	IO
		86	85	IO			86	85	IO
		88	87	IO			88	87	IO
		90	89	IO			90	89	IO
		92	91	IO			92	91	IO
		94	93	IO			94	93	IO
		96	95	IO			96	95	IO
		98	97	IO			98	97	IO
		100	99	IO			100	99	IO

Carrierboard basic power and group pin assignment (Top View), recommended to verify with Schematics

4x5 Module Controller IOs

Name	Module B2B Pin	Carrier B2B Pin	Direction (Module view)	Description	Recommendation
JTAGSEL	JM1-89	JB1-90	in	JTAG Chain multiplexer. Low FPGA, High CPLD. For module with CPLD only.	Connect Pulldown on carrier. DIP switch possible.
SC_EN1	JM1-28	JB1-27	in	Module power. Set high to enable module power. Note: Power management depends on module. Sometimes this is a only used as Power ON Reset like SC_nRST	Connect Pullup on carrier. DIP switch possible
SC_NO SEQ	JM1-7	JB1-8	in / inout	Module Power management. Set high to disable CPLD power management. Note: Power management depends on module and not all modules support extended power management with CPLD.	Connect Pullup or force to GND over zero ohm resistor on carrier. DIP switch possible.
SC_PG OOD	JM1-30	JB1-29	out / inout	Power Good signal. Is Low, if SC_EN1 is set to zero or if power is not ready, otherwise high impedance output. Note: Power management depends on module. On newer Firmware SC_PGOOD will be used as Additionally Boot Mode Pin.	Connect Pullup on carrier. Do not use this signal to enable FPGA Bank voltages. It's only for monitoring. To Enable FPGA Banks, use 3.3V(PWR_M1) or 1.8V(PWR_M2) module output.

SC_BO OTMODE	JM1-32	JB1-31	in	Boot Mode selection Pin for Zynq module only. Default low for primary SD boot and high for primary QSPI boot. Note: Depends also on module CPLD firmware	Connect Pullup on carrier. DIP switch possible.
SC_nRST	JM2-18	JB2-17	in	Low active module reset. Pin force Power one reset on FPGA /SoC. Note: Depending from module CPLD or voltage supervisor is used.	Connect Pullup on carrier. DIP switch possible.

- Controller IOs are 3.3V IOs

 It's planned to use SC_PGOOD also as additional Boot Mode Pin (Pin is bidirectional, pull up or force to zero), to additionally set JTAG only boot mode (to avoid programming problems with some vivado versions, see: [AR#00002 - QSPI Programming issues](#)). Current state of CPLD Redesigns: [AVN-20220506 4 x 5 modules controller IOs redefinition and CPLD updates](#)

4x5 Module Controller IOs

Remove 4x5 module

[4 x 5 SoMs Handling and Usage Precautions](#)

Compatibility Guide

Ethernet LED'S

TE07xx 4x5 modules do not have dedicated pins for the Ethernet PHY LED's, also there are no fix pins on the baseboards for the PHY LED's or any other LED's.

If Ethernet JACKs on Baseboard have LED's then those should be connected to some free PL I/O pins, and then routed in the FPGA logic from the PHY to the I/O Pin in the B2B Connector.

Recommended connections would be to use JM2.89 and JM2.100 for the PHY LED's, those positions support baseboard ETH LED's for TE0701 and TE0703 and TE0706.

JM2 pins 1, 3 (TE0720 Bank 34 Voltage)

- To be compatible with TE0720 JM2 pins 1,3 must be connected to some valid VCCIO voltage.
- When JM2 pins 1, 3 are not powered TE0720 would not boot, and may not be recognized in JTAG chain as well.
- When those pins are not used on the module (TE0710) then to be compatible with TE0720:
- Solution A: connect to 3.3V out from the module, option compatible to all modules except those with HP banks
- Solution B: connect to 1.8V out from the module, option compatible with all modules.

Carrier Board Checklist

Schematic Checklist

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1	Are B2B pin numbers on the connectors mirrored compared to the module pin numbers?	As B2B connectors are "unisex" type they do mirror pin numbers when connecting. That is pin1 connects to pin2, and pin2 to pin1, etc.
2	Are B2B connectors named JB1, JB2, JB3?	This is not a hard requirement, but it helps to use the same identifiers.
3	Are all GND pins connected to a common ground net?	
4	Are all VIN pins connected together?	
5	Is JB2 pin 92 pin used as VREF for the JTAG interface?	for future compatibility only, currently all modules have 3.3V JTAG
6	For 7 Series Zynq module only: Are external circuits/buffers connecting to MIO bank 1 pins powered from JB1 pin 40?	JB1 pins 18, 20, 22, 24, 26, 28 use voltage at pin 40 as VCCIO. Currently it is 1.8V for 4x5 Zynq Modules. Note: Different Power supply on TE0820(3.3V MIO Bank) and normal FPGA modules(check schematics)

PCB Checklist

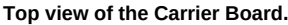
1	Are mounting holes placed properly?	Four Mounting holes should always be used. They are required for mounting screws and for module extraction. The mounting holes will also help in dissipating some heat from the module to the carrier board PCB. Four holes with a 3.2mm diameter should be placed exactly at the corners of a 34mm by 44mm rectangle.
2	Are B2B headers properly placed?	B2B headers must be placed and aligned very precisely or the module will not align correctly (in the worst case module insertion could destroy the connectors or the PCB). The B2B headers should be locked on the PCB, and it is recommended that the position and placement be checked against placement dimensions before submitting the PCB files.
3	Are B2B headers rotated properly?	As B2B header pin numbers differ from module to the carrier (swap of odd and even numbers), it is recommended that the rotation is checked in the PCB design.
4	Height clearance below module	Components can be placed below the module but height clearance rules must be obeyed.
5	Power dissipation of components below module	It is not recommended to place any components with high power dissipation below the module, as there will be almost no airflow below the module.

Visual Check of Module placement

It is highly recommended to use the Base board Template designs as a starting point for new PCB designs. If that is not possible, then adding linear dimensions in the design helps to check that all connectors and mounting holes are properly placed.



This placement is same for all 4x5 Modules!



Connector numbers as on base! (pin JB1.1 on base would mate to pin JM1.2 on module).