TE0701 CPLD

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Overview

CPLD Device with designator U14: LCMX02-1200HC

Feature Summary

- Power Management
  - VADJ Configuration via DIP-Switch or I2C
- Reset Management
- Boot Mode Controller
- FPGA UART routing
- RGPIO Interface to FPGA

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Description
ACBUS4		96	FTDI / currently_not_used
ACBUS5		88	FTDI / currently_not_used
ADBUS4	out	98	constant 0 / currently_not_used
ADBUS7	in	97	/ currently_not_used
BDBUS0	in	87	UART TX from FTDI
BDBUS1	out	86	UART RX to FTDI
C_TCK	out	81	JTAG FTDI
C_TDI	out	84	JTAG FTDI
C_TDO	in	83	JTAG FTDI
C_TMS	out	85	JTAG FTDI
CM0	in	99	DIP Switch S3-M1
CM1	in	1	DIP Switch S3-M2
CM2	in	51	REV06+ only: DIP Switch S4-4 / RGPIO Bus (powered by VIOTB (FMC VADJ))
EN_FMC	out	31	VADJ and 3V3V_FMC Power on
EN1	out	24	Power Enable Pin for Module CPLD
FMC_PRSNT	in	28	FMC Card present pin (zero if not present)
FMC_SCL	out	10	FMC I2C
FMC_SDA	inout	8	FMC I2C
FMC_TCK	out	4	JTAG FMC / currently_not_used
FMC_TDI	out	12	JTAG FMC / currently_not_used
FMC_TDO	in	9	JTAG FMC / currently_not_used
FMC_TMS	out	7	JTAG FMC / currently_not_used
HDMI_SCL	inout	47	HDMI / used also for I2C FMC control
HDMI_SDA	inout	45	HDMI / used also for I2C FMC control
HDMI_SPDIF	out	15	HDMI / currently_not_used
HDMI_SPDIFOUT	in	14	HDMI / currently_not_used
JTAGEN	--	82	Enable JTAG access to carrier CPLD for Firmware update (zero: JTAG routed to module, one: CPLD access) Set DIP Switch S3-JTAGEN to ON, for module access.
M_TCK	in	91	JTAG Module
M_TDI	in	94	JTAG Module
M_TDO	out	95	JTAG Module
M_TMS	in	90	JTAG Module
MIO10	inout	29	MIO
MIO11	inout	19	MIO
MIO12	inout	36	MIO

MIO13	inout	30	MIO
MIO14	inout	37	MIO / Module UART0.RX << BDBUS0
MIO15	in	18	MIO / Module UART0.TX >> BDBUS1
MODE	out	27	Boot Mode for Zynq Devices (Flash or SD)
NOSEQ	inout	21	No Sequence, connected to Module CPLD / currently_not_used
PG_C2M	out	20	Power Good for FMC
PGOOD	inout	25	connected to Module CPLD / currently_not_used
PHY_LED1	out	42	PHY LED
PHY_LED2	out	43	PHY LED
POK_FMC	in	32	FMC Power good from FMC VADJ DCDC
PX6	inout	49	PMOD J2
PX7	inout	48	PMOD J2
RESIN	out	13	Module Reset
REVISION_DETECION	in	57	REV06+ only: Detection / currently_not_used
S1	in	3	User Pushbutton
S2	in	2	User Pushbutton / global Reset
SD_DETECT	in	40	SD Detection
SD_WP	in	41	SD
SEL_SD	out	39	SD Selection, MMC SD Slot or PMOD J2
ULED1	out	78	LED D1
ULED2	out	77	LED D2
ULED3	out	76	LED D3
ULED4	out	16	LED D4
ULED5	out	69	LED D5, powered by VIOTB (FMC VADJ)
ULED6	out	68	LED D6, powered by VIOTB (FMC VADJ)
ULED7	out	65	LED D7, powered by VIOTB (FMC VADJ)
ULED8	out	64	LED D8, powered by VIOTB (FMC VADJ)
USB_OC	in	17	USB Over Current
VID0	out	34	VADJ Voltage selection (EN5335QI)
VID1	out	35	VADJ Voltage selection (EN5335QI)
VID2	out	38	VADJ Voltage selection (EN5335QI)
X6	in	60	Module IO (powered by VIOTB (FMC VADJ))
Y0	in	75	I2C SCL (powered by VIOTB (FMC VADJ))
Y1	out	66	I2C SDA_OUT (powered by VIOTB (FMC VADJ))
Y2	in	67	RGPIO CLK (powered by VIOTB (FMC VADJ))
Y3	out	70	RGPIO TX (powered by VIOTB (FMC VADJ))
Y4	in	74	RGPIO RX (powered by VIOTB (FMC VADJ))
Y5	in	71	I2C SDA_IN (powered by VIOTB (FMC VADJ))
Y6	in	63	Module IO (powered by VIOTB (FMC VADJ))

Functional Description

JTAG

JTAGEN set carrier board CPLD into the chain for firmware update. In normal mode JTAG is routed directly to Module. Set S3-ENJTAG to OFF to get access to carrier CPLD.

FMC JTAG is currently not enabled.

Power

EN1 is set to logical one .

EN_FMC is set to logical one or is controlled by I2C on I2C Mode.

PG_C2M is set to logical one or is controlled by I2C on I2C Mode.

VADJ

VADJ on PCB REV06+ S4 Control

This mode is only available on PCB Revision 06 or higher.

S4 control will be enabled on power on sequence or reset (S2-Button), if one of the three S4-DIP switches is set to one.

In this Mode I2C-controll is not selectable and S3-M1 and S3-M2 are available as User-DIP-Switch.

S4-3(VID2)	S4-2(VID1)	S4-1(VID0)	Description
ON	ON	ON	VADJ: 3.3V
ON	ON	OFF	VADJ: 2.5V
ON	OFF	ON	VADJ: 1.8V
ON	OFF	OFF	VADJ: 1.5V
OFF	ON	ON	VADJ: 1.25V
OFF	ON	OFF	VADJ: 1.2V
OFF	OFF	ON	VADJ: 0.8V (Do not use, not supported as IO standard)
OFF	OFF	OFF	used to set VADJ control to REV05- or I2C control after power up sequence

VADJ on PCB REV05- S3 Control

S4 control will be disabled on power on sequence or reset (S2-Button), if all of the three S4-DIP switches is set to OFF or older PCB revision is used.

Do not set S4-Switches to ON, if REV05- or I2C control is enabled.

S3-M1	S3-M2	Description
OFF	OFF	VADJ: 1.8V
OFF	ON	VADJ: 2.5V
ON	OFF	VADJ: 3.3V
On	ON	I2C controlled

VADJ on I2C Control

Disable S4 Control (see VADJ on PCB REV05- S3 Control) and set S3-M1 and S3-M2 to on. I2C VADJ Control use TE0701 HDMI I2C Bus (HDMI_SCL and HDMI_SDA) connected to module FPGA PL side. I2C-GPIO controller device address is 0x22. Transmitted data will be converted to a 8-bit GPIO bus.

Bit	Access	Default	Description
7	R/W	0	FMC - Enable
6	R/W	0	VID2
5	R/W	0	VID1
4	R/W	0	VID0
3	R/W	0	PG_C2M - Enable
2	R	x	POK_FMC (EN5335QI Power OK)
1	R	x	one: I2C Mode, zero: DIP Mode,
0	R	x	VID Mode (zero: S4-DIP-controlled, one: REV05-/I2C controlled)

VID2	VID1	VID0	Description
0	0	0	VADJ: 3.3V
0	0	1	VADJ: 2.5V
0	1	0	VADJ: 1.8V
0	1	1	VADJ: 1.5V
1	0	0	VADJ: 1.25V
1	0	1	VADJ: 1.2V
1	1	0	VADJ: 0.8V
1	1	1	reserved

To read I2C with petalinux use i2cget -y 0 0x22.

- -y: do not confirm input
- 0: I2CBUS, use bus number, which is connected to TE0701 HDMI I2C Bus (HDMI_SCL and HDMI_SDA)
- 0x22 I2C GPIO controller on TE0701 CPLD

To write I2C with petalinux use i2cset -y 0 0x22 0x80

- -y: do not confirm input
- 0: I2CBUS, use bus number, which is connected to TE0701 HDMI I2C Bus (HDMI_SCL and HDMI_SDA)
- 0x22 I2C GPIO controller on TE0701 CPLD
- 0x80: Enable FMC Power with VAD 3.3V, see I2C control table.

Reset

RESIN (negative Reset) to module, can be set by S2 button.

Boot Mode

Boot mode is set to SD-Boot, when SD-Card is detected.

FMC I2C

"3 wire split i2c" to to normal I2C:

```
FMC_SDA       <= '0' when Y5='0' else 'Z';
FMC_SCL       <= Y0 and PON;
Y1            <= FMC_SDA;
```

RGPIO

RGPIO Master is a 32Bit Remote GPIO Interface to talk with FPGA over 3 lanes.

RGPIO Pin to FPGA	Value
0	MIO10
1	MIO11
2	MIO12
3	MIO13
4	MIO14
5	MIO15
6	PX6
7	PX7
8	S1
9	CM0
10	CM1
11	CM2
12	SD_WP
13	SD_DETECT
14	USB_OC
15	POK_FMC
16	FMC_PRSNT
17	PGOOD
18	NOSEQ
19	unused
20	X6
21	Y6
22-23	unused
24-27	reserved
28-31	Interface detection

RGPIO Pin from FPAG	Value
0-7	LED 1-8
8-9	PHY_LED 1/2
10-23	unused
24-27	reserved
28-31	Interface detection

LED

LED	Description
ULED1	VADJ selection when RGPIO Bus is not active else RGPIO Bus Pin 0 VADJ selection: blink when VCCIO(VIOTB/VADJ) is disabled else on when VADJ on PCB REV05- or I2C Control or off when VADJ on PCB REV06+ S4 Control
ULED2	I2C control mode when RGPIO Bus is not active else RGPIO Bus Pin 1
ULED3	UART to Module activity when RGPIO Bus is not active else RGPIO Bus Pin 2
ULED4	UART to FTDI activity when RGPIO Bus is not active else RGPIO Bus Pin 3
ULED5	BOOTMODE (on Flash, off SD) when RGPIO Bus is not active else RGPIO Bus Pin 4
ULED6	CM2 when RGPIO Bus is not active else RGPIO Bus Pin 5
ULED7	X6 when RGPIO Bus is not active else RGPIO Bus Pin 6
ULED8	Y6 when RGPIO Bus is not active else RGPIO Bus Pin 7

PHY LED	Description
PHY_LED1	Y2 when RGPIO Bus is not active else RGPIO Bus Pin 8
PHY_LED2	Y4 when RGPIO Bus is not active else RGPIO Bus Pin 9

UART

To	From	Description
MIO14	BDBUS0	Module UART0.RX
BDBUS1	MIO15	Module UART0.TX

Appx. A: Change History

Revision Changes

Older Revisions to REV05

- Power Management

    - three VADJ Control Modi (REV06+ S4 Control, REV05- S3 Control and I2C Control)
- Reset Management
    - only little changes
- RGPIO Interface to FPGA
    - RGPIO support
- LED
    - new Order and accessible by RGPIO

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
	Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] Unknown macro: 'metadata'	REV05	REV03,REV04, REV05,REV6	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which metho	Add FMC I2C description

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

d to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class

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2017-08-14	v.27	REV05	REV03,REV04, REV05,REV6	John Hartfiel	Description correction on port table
2017-06-08	v.26	REV05	REV03,REV04, REV05,REV6	John Hartfiel	document style update.
2016-11-29	v.24	REV05	REV03,REV04, REV05,REV6	John Hartfiel	Revision 05 finished
2016-04-11	v.1	---			Initial release

Error rendering macro 'page-info'

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	All			**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy2	

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