

# MPSoC Debug

## Zynq MPSoC Debug Troubleshooting

#	Problem	Possible reason(s)	Fix(es) or workaround
1	Debug freezes on DDR4 init	DDR4 init can be done only once, if the PS DDR4 was initialized then any attempt of double init, by FSBL c code or psu_init.tcl will freeze	Power cycle or hardware reset is required to clear DDR4 registers
2	Debug freezes on SERDES init	On TE0808 Si5345 is not initialized after power-up by default, and if the FSBL was generated from Vivado project that enables any PS GT, then FSBL or psu_init.tcl would freeze	Programming the Si5345 OTP, disabling all PS GT in Vivado, starting an FSBL that does init Si5345 then debugging without power cycle, using Silabs desktop programmer to init Si5345.
3	JTAG Target not detected by SDK /Debugger	On Zynq MPSoC JTAG is disabled by default after each power cycle or main reset and only enabled if bootrom does it under software control. If FSBL is not found or the FSBL found detects some error condition, then JTAG may be left disabled, and further debugging is not possible.	Select JTAG bootmode. Use known good FSBL that releases JTAG for debug process.
4	SDK FSBL Debugger show only Assembler Code, instead of C Code	Build and BSP settings are not correct	<p>Change Settings</p> <p>For fsbl:</p> <ul style="list-style-type: none"><li>• right click on fsbl, select C/C++ Build settings</li><li>• Select ARM A53 gcc compiler-&gt;Miscellaneous</li><li>• remove "-Os -fno-float-objects" from 'other flags'</li></ul> <p>For fsbl_bsp</p> <ul style="list-style-type: none"><li>• right click on fsbl_bsp and select Board Support Package Settings</li><li>• Select overview-&gt;standalone</li><li>• change zynqmp_fsbl_bsp value from 'true' to 'false'</li></ul> <p>See: <a href="https://forums.xilinx.com/t5/Embedded-Development-Tools/Debug-FSBL-with-SDK-on-ZynqMP-ES2/td-p/773403">https://forums.xilinx.com/t5/Embedded-Development-Tools/Debug-FSBL-with-SDK-on-ZynqMP-ES2/td-p/773403</a></p> <p>Debugging Menu has changed with Vitis. Here some additional notes: <a href="https://www.centennialsoftwaresolutions.com/post/fsbl-creation-and-source-debug-in-xilinx-vitis-2019-2">https://www.centennialsoftwaresolutions.com/post/fsbl-creation-and-source-debug-in-xilinx-vitis-2019-2</a> FSBL is too big for OCM in case it's not optimised, so debugging with SDK is not so easy</p>
5			FSBL debug flags: <a href="https://www.xilinx.com/support/documentation/user_guides/ug1137-zynq-ultrascale-mpsoc-swdev.pdf">https://www.xilinx.com/support/documentation/user_guides/ug1137-zynq-ultrascale-mpsoc-swdev.pdf</a>

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