TEBF0808 Master CPLD

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Overview

Firmware for PCB-Master CPLD with designator U17. First CPLD Device in Chain: LCMX02-1200HC

Feature Summary

- FMC VADJ Power
- JTAG / FMC JTAG / PJTAG
- RESET/Enable Management
- LED
- RGPIO
- SD
- CAN
- USB
- DisplayPort

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Schematic /Souce Code Name	Direction	Pin	Description	PCB REV2 Exception
C_T1		24	/ currently_not_used	NC
C_T2		26	/ currently_not_used	NC
C_T3		25	/ currently_not_used	NC
C_TCK	in	131	JTAG J28 (XMOD2) / FMC JTAG	
C_TDI	in	136	JTAG J28 (XMOD2) / FMC JTAG	
C_TDO	out	137	JTAG J28 (XMOD2) / FMC JTAG	
C_TMS	in	130	JTAG J28 (XMOD2) / FMC JTAG	
CAN_FAULT	in	106	CAN	
CAN_RX	in	107	CAN	
CAN_S	out	105	CAN	
CAN_TX	out	104	CAN	
CLK_125MHZ / PHY_CLK	in	70	/ currently_not_used	
CON_NTRST		117	/ currently_not_used	
CON_RTCK / JTAG_RTCK	out	125	JTAG, Connector J30	
CON_SRST / JTAG_SRST	in	127	JTAG, Connector J30	
CON_TCK / JTAG_TCK	in	122	JTAG, Connector J30 / PJTAG0	
CON_TDI / JTAG_TDI	in	119	JTAG, Connector J30 / PJTAG0	
CON_TDO / JTAG_TDO	out	126	JTAG, Connector J30 / PJTAG0	
CON_TMS / JTAG_TMS	in	121	JTAG, Connector J30 / PJTAG0	
DIR_T1		23	/ currently_not_used	NC
DIR_T2		28	/ currently_not_used	NC
DIR_T3		27	/ currently_not_used	NC
DP_AUX_DE / DP_DE	out	92	Display Port	
DP_AUX_RX / DP_RX	in	91	Display Port	
DP_AUX_TX / DP_TX	out	93	Display Port	
DP_EN	out	77	Display Port	
DP_TX_HPD /DP_HDP	in	94	Display Port	
ETH_RST	out	62	Ethernet	
EX_IO1		112	PMOD / currently_not_used	
EX_IO2		113	PMOD / currently_not_used	
EX_IO3		114	PMOD / currently_not_used	
EX_IO4		115	PMOD / currently_not_used	
F2_EN		19	FAN J35 / currently_not_used	NC
F2PWM		20	FAN J35 / currently_not_used	NC

F2SENSE		21	FAN J35 / currently_not_used	NC
FMC_CLK_DIR	in	73	FMC	
FMC_TCK	out	95	FMC	
FMC_TDI	out	96	FMC	
FMC_TDO	in	97	FMC	
FMC_TMS	out	98	FMC	
FMC_VID0	out	139	FMC VADJ Power Selection	
FMC_VID1	out	140	FMC VADJ Power Selection	
FMC_VID2	out	141	FMC VADJ Power Selection	
GND		84	REV03 unconnected / currently_not_used	USB_TRST, other USB HUB
HDIO_SC10 / SC10	inout	60	FPGA / DP_RX or 'Z'	
HDIO_SC11 / SC11	in	59	FPGA / DP_DE	
HDIO_SC12 / SC12	out	58	FPGA / DP_HPD	
HDIO_SC13 / SC13	out	57	FPGA / RGPIO TX	
HDIO_SC14 / SC14	in	56	FPGA / RGPIO RX	
HDIO_SC15 / SC15	in	55	FPGA / RGPIO CLK	
HDIO_SC16 / SC16	in	54	FPGA / CAN_S	
HDIO_SC17 / SC17	in	52	FPGA / XMOD LED	
HDIO_SC18 / SC18	in	68	FPGA / CAN_TX	
HDIO_SC19 / SC19	out	69	FPGA / CAN_RX	
I2C_RST	out	61	I2C	
JTAGENB		120	external Pin for CPLD Firmware Update	
LED_1A / JLED1	out	109	USB3.0 LED Jellow	
LED_2A / JLED2A	out	111	USB3.0 LED Green/Orange	
LED_2B / JLED2B	out	110	USB3.0 LED Green/Orange	
MIO26	in	41	MIO / PJTAG	
MIO27	in	40	MIO / PJTAG	
MIO28	in	39	MIO / PJTAG	
MIO29	in	38	MIO / PJTAG	
OCLK_EN / OSC_EN	out	74	Programmable Oscillator U45	
PHY_CONFIG	out	65	ETH PHY	
PHY_LED0	in	67	ETH PHY	
PHY_LED1	in	86	ETH PHY	
PHY_LED2	in	85	ETH PHY	
SC_CLK0 / CLK0	in	76	/ currently_not_used	SC_CLK_P
SC_CLK1 / CLK1	in	75	/ currently_not_used	SC_CLK_N
SC_IO0 / X0	in	50	Master-Slave SC-Communication / Power Reset	
SC_IO1 / X1	in	49	Master-Slave SC-Communication / Power Reset	
SC_IO2 / X2	in	48	Master-Slave SC-Communication / currently_not_used	
SC_IO3 / X3	in	47	Master-Slave SC-Communication / currently_not_used	

SC_IO4 / X4	out	45	Master-Slave SC-Communication / SD WP to Slave CPLD	
SC_IO5 / X5	out	44	Master-Slave SC-Communication / currently_not_used	
SC_IO6 / X6	out	43	Master-Slave SC-Communication / Sanity check to other CPLD (FMC VADJ Enable)	
SC_IO7 / X7	out	42	Master-Slave SC-Communication / Sanity check to other CPLD (FMC VADJ Enable)	
SC_IO8		22	Master-Slave SC-Communication / currently_not_used	NC
SC_SCL / SCL	in	14	I2C Mux U27 / currently_not_used	
SC_SDA / SDA	in	13	I2C Mux U27 / currently_not_used	
SC2_SW3 / SW3	in	6	DIP-Switch S5-3	
SC2_SW4 / SW4	in	5	DIP-Switch S5-4	
SD_WP	in	100	MMC SD	
SFP_LED1 / SFP_LED0	out	81	SFP	
SFP_LED2 / SFP_LED1	out	82	SFP	
SFP_LED3 / SFP_LED2	out	78	SFP	
SFP_LED4 / SFP_LED3	out	83	SFP	
SFP1_LOS		32	SFP / currently_not_used	NC, controlled by FPGA
SFP1_TX_DIS	out	33	SFP	NC, controlled by FPGA
SFP2_LOS		35	SFP / currently_not_used	NC, controlled by FPGA
SFP2_TX_DIS	out	34	SFP	NC, controlled by FPGA
STAT_LED0 / LED0		99	LED D4 Green	
STAT_LED1 / LED1		128	LED D1 Red	
USB0_RST / USB_RST	out	71	USB (U9) PHY Reset	USB PHY and HUB Reset
USBH_LED_G3		11	USB Hub (U4) / currently_not_used	NC, other USB HUB
USBH_LED_G4		12	USB Hub (U4) / currently_not_used	NC, other USB HUB
USBH_LED_SS1		9	USB Hub (U4) / currently_not_used	NC, other USB HUB
USBH_LED_SS2 / dummy	out	133	USB Hub (U4) Dummy Signal / currently_not_used	NC, other USB HUB
USBH_LED_SS3		132	USB Hub (U4) / currently_not_used	NC, other USB HUB
USBH_LED_SS4		138	USB Hub (U4) / currently_not_used	NC, other USB HUB
USBH_MODE0	out	142	USB Hub (U4)	NC, other USB HUB
USBH_MODE1	out	143	USB Hub (U4)	NC, other USB HUB
USBH_RST	out	10	USB Hub (U4)	NC, other USB HUB
XMOD1_A		3	J28 (XMOD 2) / currently_not_used	
XMOD1_B		2	J28 (XMOD 2) / currently_not_used	
XMOD1_E /XMOD_E	out	4	J28 (XMOD 2 LED)	
XMOD1_G / XMOD_G	in	1	J28 (XMOD 2 Button)	

Functional Description

JTAG

JTAGENB set carrier board CPLD into the chain for firmware update. For Update set DIP S4-3 to ON.

FMC JTAG is connected to XMOD2 JTAG. Set DIP S4-3 to OFF for FMC access.

PJTAG (MIO29..26) is connected to JTAF Pinheader J30.

Power

FMC VADJ is 1.8V if S5-4 is ON else 1.2V.

Reset

Main Reset is send by Slave CPLD via X0, X1 Pins.

USB PHY hold ~0,6s after Main Reset or XMOD_G Reset or inv.RGPIO Bus Pin 0 (if active).

USB HUB hold ~0,25s after Main Reset or XMOD_G Reset or inv. RGPIO Bus Pin 0 (if active). Long delay is a BUGFIX: is currently need to start Linux before Reset is disabled.

I2C Reset is Main Reset or inv. RGPIO Bus Pin 2 (if active).

ETH Reset is Main Reset or inv. RGPIO Bus Pin 3 (if active).

Enable

FMC VADJ Enable is set from Slave CPLD via Saity Check (X6, X7).

SFP1 and SFP2 are always enabled.

Oscillator U45 is enabled

USB

USB Hub Device Operation Mode (USBH_MODEx Pins) are set to internal ROM configuration. Can be controlled by RGPIO Bus Pin 4 and 5.

ETH

PHY Address is 1.

Display Port

SC10 is controlled by DP_RX when SC11 is zero else high impedance state. DP_TX controlled by SC10 and DP_DE controlled by SC11.SC12 is controlled by DP_HPD.

CAN

CAN_TX soured by SC18.

SC19 sourced by CAN_RX.

CAN_S sourced by S16.

SD

SD WP is forwarded to Slave CPLD.

RGPIO

RGPIO Pin to FPGA	Value
0	SW3
1	SW4
2	SD_WP
3	XMOD_G
4	'0'
5	'0'
6	'0'
7	'0'
8	CAN_FAULT
9	PHY_LED0
10	PHY_LED1
11	PHY_LED2
12	FMC_TDO
13	FMC_CLKDIR
14	JTAG_TRST
15	JTAG_SRST
16	'0'
17	'0'
18	'0'
19	DP_HPD
20	SDA
21	SCL
22-23	unused zero
24-27	reserved
28-31	Interface detection

RGPIO Pin from FPGA	Value
0	not USB_RST
1	not USBH_RST
2	not I2C_RST
3	not ETH_RST
4	not USBH_MODE0
5	not USBH_MODE1
6	LED0

7	LED1
8	SFP_LED0
9	SFP_LED1
10	SFP_LED2
11	SFP_LED3
12	JLED1
13	JLED2A
14	JLED2B
15-23	unused
24-27	reserved
28-31	Interface detection

LED

Name	Description
LED0 D4 Green	RGPIO (6) when active else USB HUB RSTN
LED1 D1 Red	RGPIO (7) when active else Main Reset from Slave CPLD
SFP_LED0 Red	RGPIO (8) when active else blinking when PCB power is on and reset Button is pressed else off
SFP_LED1 Green	RGPIO (9) when active else blinking when PCB power is on and reset Button is pressed else off
SFP_LED2 Red	RGPIO (10) when active else blinking when PCB power is on and reset Button is pressed else off
SFP_LED3 Green	RGPIO (11) when active else blinking when PCB power is on and reset Button is pressed else off
JLED1 Yellow	RGPIO (12) when active else blinking when PCB power is on and reset Button is pressed else not PHY_LED0 when X1 is zero else off
JLED2A Green	RGPIO (13) when active else blinking when PCB power is on and reset Button is pressed else not PHY_LED1 when X1 is zero else on
JLED2B Orange	RGPIO (14) when active else blinking when PCB power is on and reset Button is pressed else off
XMOD_E Red	Blinking when Main Power Reset else SC17

*Blinking: ~1,5Hz

Appx. A: Change History

Revision Changes

CPLD REV05 to REV06

- BUGFIX: renamed SC19 to SC17
- Connect FMC JTAG to XMOD2 JTAG

- Connect PJTAG0 (MIO29..26) to JTAG Pin Header J30
- Connect CAN to PL
- RGPIO Pin changes

CPLD REV04 to REV05

- SD WP
- XMOD LED access over PL

Older Revision (PCB REV03) to CPLD REV04

- Fix USB HUB Mode default state over RGPIO
- Invert JLED2B over RGPIO

Older Revision (PCB REV02) to CPLD REV04

- Add all functionality from older Revision (PCB REV03)

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
	Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] Unknown macro: 'metadata'	REV06	(REV02 Special Firmware!), REV03,REV04	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevel	• small Update Pinout Table

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

Permission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceU

				ser, class java. lang. String, class com. atlassi an. conflue nce. core. Conten tEntity Object] [interfa ce com. atlassi an. user. User, class java. lang. String, class com. atlassi an. conflue nce. core. Conten tEntity Object]	

2017-10-18	v.25	REV06	(REV02 Special Firmware!), REV03,REV04	John Hartfiel	• Revision 06 finished
2017-06-20	v.23	REV05	(REV02 Special Firmware!), REV03,REV04	John Hartfiel	• Document Bugfix, XMOD LED is connected to SC17
2017-06-12	v.22	REV05	(REV02 Special Firmware!), REV03,REV04	John Hartfiel	• Port description update
2017-06-09	v.21	REV05	(REV02 Special Firmware!), REV03,REV04	John Hartfiel	• Revision 05 finished
2017-06-08	v.17	REV04	(REV02 Special Firmware!), REV03,REV04	John Hartfiel	• document style update
2017-03-10	v.15	REV04	(REV02 Special Firmware!), REV03,REV04	John Hartfiel	• Revision 04 finished
2016-12-14	v.1	---		**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasConten	• Initial release

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	All			**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.	

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Appx. B: Legal Notices

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