TE0710 TRM

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Overview

Trenz Electronic TE0710 is an industrial-grade FPGA module integrating a Xilinx Artix-7 FPGA, two 10/100 Mbit Ethernet PHYs, 512 MByte DDR3 SDRAM, 32 MByte Quad SPI Flash memory for configuration and operation and powerful switching-mode power supplies for all on-board voltages. Numerous configurable I/Os are provided via rugged high-speed strips. All this on a tiny footprint, smaller than a credit card size at very competitive price. All Trenz Electronic SoMs in 4 x 5 cm form factor are mechanically compatible.

Key Features

- Industrial-grade Xilinx Artix-7 FPGA (15T to 100T) , supported by the free Xilinx Vivado WebPACK development tool
- Rugged for shock and high vibration
- 512 MByte DDR3 SDRAM
- Dual 10/100 Mbit Ethernet PHY
    - MAC Address EEPROM
- 32 MByte QSPI Flash memory (with XiP support)
- 100 MHz MEMS oscillator
- Plug-on module with 2 × 100-pin high-speed hermaphroditic strips
- 112 FPGA I/Os (51 differential pairs) are available via board-to-board connectors
- On-board high-efficiency DC-DC converters
    - 4.0 A x 1.0 V power rail
    - 1.0 A x 1.8 V power rail
    - 1.0 A x 1.5 V power rail
- System management and power sequencing
- eFUSE bit-stream encryption
- AES bit-stream encryption
- User LED
- Evenly-spread supply pins for good signal integrity

NB! Assembly options for cost or performance optimization are available upon request.

Block Diagram

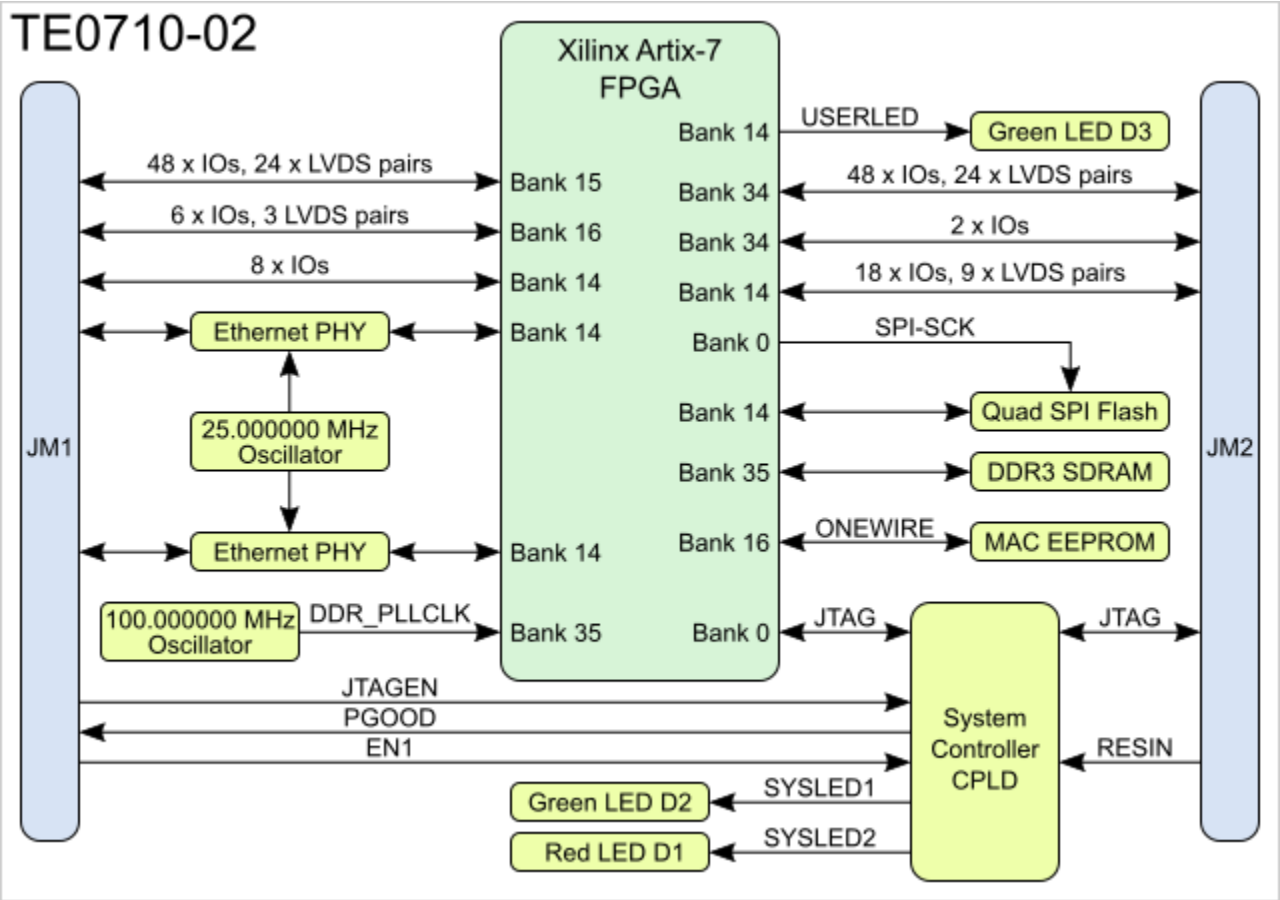


Figure 1: TE0710-02 block diagram.

Main Components

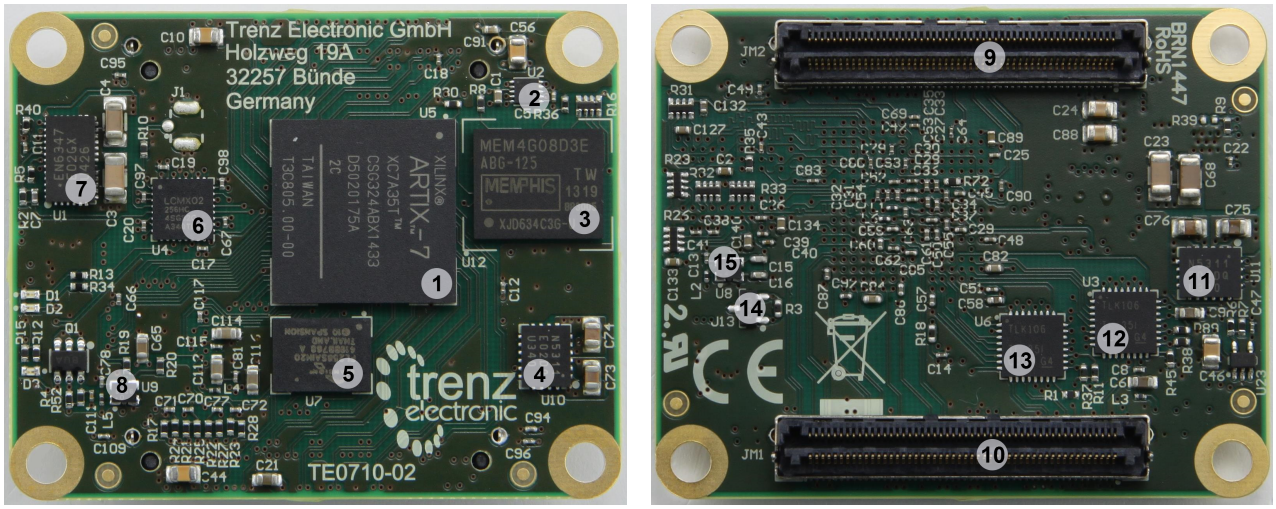


Figure 2: TE0710-02 PCB.

1. Xilinx Artix-7 FPGA , U5
2. Voltage regulator for DDR3 SDRAM (Texas Instruments TPS51206), U2
3. 512 MByte DDR3 SDRAM (Memphis MEM4G08D3EABG), U12
4. 1A PowerSoC DC-DC converter for 1.5V (Altera EN5311QI), U10
5. 32 MByte Quad SPI Flash memory (Cypress S25FL256S), U7
6. System Controller CPLD (Lattice Semiconductor LCMXO2-256HC), U4
7. 4A PowerSoC DC-DC converter for 1.0V (Altera EN6347QI), U1
8. Programmable oscillator @25.000000 MHz for Ethernet reference clock (SiTime SiT8008), U9
9. B2B connector (0,40 mm Razor Beam™ High Speed Hermaphroditic Strip LSHM-150), JM2
10. B2B connector (0,40 mm Razor Beam™ High Speed Hermaphroditic Strip LSHM-150), JM1
11. 1A PowerSoC DC-DC converter for 1.5V for 1.8V (Altera EN5311QI), U11
12. 10/100 Mbps Ethernet PHY (Texas Instruments TLK106), U3
13. 10/100 Mbps Ethernet PHY (Texas Instruments TLK106), U6
14. 2 Kbit serial EEPROM with UNI/O serial interface (Microchip 11AA02E48T-I/TT), U13
15. Programmable oscillator @100.000000 MHz for reference clock (SiTime SiT8008), U8

Initial Delivery State

Storage Component	Content	Notes
SPI Flash OTP Area	Empty, not programmed	Except serial number programmed by flash vendor.
SPI Flash Quad Enable bit	Programmed	-
SPI Flash main arraay	Empty	-
eFUSE USER	Not programmed	-
eFUSE Security	Not programmed	-

Table 1: TE0710-02 module initial delivery state.

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

FPGAs I/O banks, voltages and B2B connections:

Bank	Type	B2B Connector	I/O Signal Count	Voltage	Notes
14	HR	JM1	8 I/O pins	3.3V	HR banks support voltages from 1.2V to 3.3V. See Xilinx Artix-7 datasheet (DS181) for voltage ranges.
15	HR	JM1	48 I/O pins 24 LVDS pairs	User	Same as above.
16	HR	JM1	6 I/O pins 3 LVDS pairs	3.3V	Same as above.
34	HR	JM2	50 I/O pins 24 LVDS pairs	User	Same as above.

Table 2: FPGA I/O banks.

Please refer to Pin-out tables page for more information.

JTAG Interface

JTAG access to the Xilinx Artix-7 and System Controller CPLD is provided through B2B connector JM2.

JTAG Signal	B2B Pin
TMS	JM2-93
TDI	JM2-95
TDO	JM2-97
TCK	JM2-99

Table 3: JTAG interface connector.

> ⚠ JTAGEN pin on B2B connector JM1 is used to control which physical device is accessible via JTAG interface. If this pin is set to low or left open, JTAG interface is enabled for Xilinx Artix-7 FPGA, if set to high, JTAG interface for System Controller CPLD will be enabled.
>
> The use of Xilinx legacy development tools (ISE, iMPACT) is not recommended. iMPACT does not recognize any Xilinx Artix-7 below A100T model.

System Controller I/O Pins

Special purpose pins are connected to the System Controller CPLD which have following default function:

Pin Name	Mode	Function	Default Configuration	B2B Pin
PGOOD	Output	Power Good	Active high when all on-module power supplies are operating properly.	JM1-30
RESIN	Input	Reset	Active low, drive low to keep system in reset state (FPGA pin PROG_B will be driven by CPLD).	JM2-18
EN1	Input	Reset	Same as RESIN, can be left unconnected.	JM1-28

JTAGEN	Input	JTAG Select	Low for normal operation, high (3.3V) to enable JTAG for System Controller CPLD.	JM1-89
MODE	-	-	Not used by default, leave open.	JM1-32
NOSEQ	-	-	Not used by default, leave open.	JM1-7

Table 4: Special purpose pins description of the System Controller CPLD.

On-board LEDs

There are three LEDs available on TE0710-02 SoM. Two are status LEDs, and one can be freely used by user design. The user LED is routed to the FPGA as 'USERLED'.

When the FPGA is not configured the status LEDs will flash continuously. Once the FPGA configuration has completed, the status LEDs can be used by the user FPGA design.

LED	Color	Connected to	Description and Notes
D1	Red	SYSLED2	System Controller status LED, connected to CPLD.
D2	Green	SYSLED1	System Controller status LED, connected to CPLD.
D3	Red	USERLED	User LED, active LOW, connected to FPGA pin L15.

Table 5: On-board LEDs.

Clocking

The TE0710-02 SoM is equipped with two MEMS oscillators to provide clock signals for two on-board Ethernet PHYs and DDR3 SDRAM.

Clock	Frequency	IC	Connected to	Notes
Ethernet reference	25 MHz	U9, SiT8008AI-73-XXS-25.000000E	ICs U3, U6 TLK106RHB	Clock signal shared by both Ethernet PHYs.
DDR3 SDRAM reference	100 MHz	U8, SiT8008AI-73-XXS-100.000000E	FPGA bank 35, pin F4	Differential clock signal for DDR3 SDRAM IC, U12.

Table 6: Clocks overview.

On-board Peripherals

32 MByte Quad SPI Flash Memory

An SPI flash memory S25FL256S (U7) is provided for FPGA configuration file storage. After configuration completes the remaining free memory can be used for application data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.

> ⚠ SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash during power-on. By default this bit is set to high at the manufacturing plant.

System Controller CPLD

System Controller CPLD (Lattice MachXO2-256HC, U4) is used to control FPGA configuration process. The FPGA is held in reset (by driving the PROG_B signal low) until all power supplies have stabilized.

By driving signal RESIN to low you can reset the FPGA. This signal can be driven from the user's baseboard PCB via the B2B connector JM2 pin 18.

Input EN1 is also gated to FPGA reset, should be open or pulled up for normal operation. By driving EN1 low, on-board DC-DC converters are not turned off.

User can create their own System Controller design using Lattice Diamond software. Once created it can be programmed into CPLD via JTAG interface.

DDR3 SDRAM

The TE0710-02 SoM has one 512 MByte volatile DDR3 SDRAM IC (U12) for storing user code and data.

- Part number: MEM4G08D3EABG-125 (Memphis)
- Supply voltage: 1.5V
- Organization: 64M words x 8 bits x 8 banks
- Memory speed limited by Xilinx Artix-7 speed grade and MIG

Configuration of the DDR3 memory controller in the FPGA should be done using the MIG tool in the Xilinx Vivado Design Suite IP catalog.

Ethernet PHYs

The TE0710-02 is equipped with two Texas Instruments TLK106 10/100 Mbit Ethernet PHYs (U3 and U6). The I/O voltage is fixed at 3.3V. The reference clock input for both PHYs is supplied by on-board 25 MHz oscillator (U9). Both Ethernet PHYs are connected to FPGA bank 14 using MII interface.

Note: Pin ETH2_INT (power down or interrupt, default function is power down) is connected to FPGA bank 16 (pin D10).

MAC Address EEPROM

TE0710-02 module is equipped with 2 Kbit serial Electrically Erasable PROM (EEPROM, U14). It provides pre-programmed 48-bit Extended Unique Identifier (EUI-48™) to identify network hardware MAC address which is write-protected to ensure tamper-proof designs. This EEPROM can be accessed by UNI/O® serial interface bus using Manchester encoding techniques. The clock and data are combined into a single, serial bit stream (SCIO), where the clock signal is extracted by the receiver to correctly decode the timing and value of each bit. The bus is controlled by a master device (Xilinx Artix-7) which determines the clock period, controls the bus access and initiates all operations, while the EEPROM works as a slave. Refer to Microchip's 11AA02E48 datasheet for more information.

Power and Power-On Sequence

Power Supply

Power supply with minimum current capability of 2A for system startup is recommended.

Power Input Pin	Voltage Range	Current
VIN	3.3V to 5.5V	Typical 200mA, depends on customer design and setup.
3.3VIN	3.3V	Typical 50mA, depends on customer design and setup.

Table 7: Typical power consumption during normal operation.

VIN and 3.3VIN can be connected to the same power source (3.3 V).

Lowest power consumption is achieved when powering the module from single 3.3V power supply. When using split 3.3V/5V supplies the power consumption (and heat dissipation) will rise, this is due to the DC-DC converter efficiency (it decreases when VIN/VOUT ratio rises).

Power-On Sequence

For highest efficiency of on-board DC-DC regulators, it is recommended to use same 3.3V power source for both VIN and 3.3VIN power rails. Although VIN and 3.3VIN can be powered up in any order, it is recommended to power them up simultaneously.

It is important that all baseboard I/Os are 3-stated at power-on until System Controller sets PGOOD signal high (B2B connector JM1, pin 30), or 3.3V is present on B2B connector JM2 pins 10,12 or 91, meaning that all on-module voltages have become stable and module is properly powered up.

See Xilinx datasheet DS181 (for Artix7) for additional information. User should also check related baseboard documentation when choosing baseboard design for TE0710-02 module.

A 3.3V supply is also needed and must be supplied from the user's PCB. An output 3.3V supply is available on some of the board connector pins (see section 'Power Rails'). The input 3.3VIN will be switched to the internal 3.3V voltage level after the FPGA 1.0V supply is stable. Than 3.3V supply will be available on the B2B connector pins.

The regulators can be powered from the 3.3V supply or a 5V supply if preferred. The options for powering the board are as follows:

- Apply 5V to pins VIN and 3.3V to pins 3.3VIN on the board connector
- Apply 3.3V to pins VIN and 3.3VIN on the board connectors.

Power Rails and Bank Voltages

Voltages on B2B-Connectors	B2B JM1-Pin	B2B JM2-Pin	Direction	Note
VIN	1, 3, 5	2, 4, 6, 8	Input	Supply voltage
3.3VIN	13, 15	-	Input	Supply voltage
VCCIO15	9, 11	-	Input	High range bank voltage
VCCIO34	-	7, 9	Input	High range bank voltage
3.3V	-	10, 12	Output	Internal 3.3V voltage level
JTAG VREF	-	91	Output	JTAG reference voltage (3.3V).
1.8V	39	-	Output	Internal 1.8V voltage level
1.5V	-	19	Output	Internal 1.5V voltage level

Table 8: Power rails on B2B connectors.

FPGA Bank	Schematics Name	Voltage	Range
0 Config	3.3V	3.3V	-
14	3.3V	3.3V	-
15	VCCIO15	User	HR: 1.2V to 3.3V
16	3.3V	3.3V	-
34	VCCIO34	User	HR: 1.2V to 3.3V
35	1.5V	1.5V	-

Table 9: FPGA bank voltages.

See Xilinx Artix-7 datasheet DS181 for allowed voltage ranges.

Board to Board Connectors

These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three Samtec Razor Beam LSHM connectors on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

Connectors.

The module can be manufactured using other connectors upon request.

Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

Speed rating.

Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

Manufacturer Documentation

File	Modified
PDF File hsc-report_lshm-lshm-05mm_web.pdf High speed test report	07 04, 2016 by Thorsten Trenz

PDF File lshm_dv.pdf LSHM catalog page	07 04, 2016 by Thorsten Trenz
PDF File LSHM-1XX-XX.X-X-DV-A-X-X-TR-FOOTPRINT(1).pdf Recommended layout and stencil drawing	07 04, 2016 by Thorsten Trenz
PDF File LSHM-1XX-XX.X-XX-DV-A-X-X-TR-MKT.pdf Technical drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189016-01.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189016-02.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189017-01.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189017-02.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File TC0923--2523_report_Rev_2_qua.pdf Design qualification test report	07 04, 2016 by Thorsten Trenz
PDF File tc0929--2611_qua(1).pdf Shock and vibration report	07 04, 2016 by Thorsten Trenz

Download All

Variants Currently In Production

Module Variant	FPGA	FPGA Junction Temperature	Operating Temperature Range
TE0710-02-35-2IF	XC7A35T-2CSG324I	-40°C to 100°C	Industrial grade
TE0710-02-100-2IF	XC7A100T-2CSG324I	-40°C to 100°C	Industrial grade
TE0710-02-35-2CF	XC7A35T-2CSG324C	0°C to 85°C	Commercial grade
TE0710-02-100-2CF	XC7A100T-2CSG324C	0°C to 85°C	Commercial grade

Table 10: Differences between TE0710-02 variants.

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VIN supply voltage	-0.3	7.0	V	EN6347QI, EN5311QI datasheet
3.3VIN supply voltage	-0.1	3.6	V	-
HR I/O banks supply voltage (VCCO)	-0.5	3.6	V	Xilinx datasheet DS181
HR I/O banks input voltage	-0.4	VCCO + 0.55	V	Xilinx datasheet DS181
Voltage on module JTAG pins	-0.5	VCCO_0 + 0.45	V	VCCO_0 is 3.3V nominal
Storage temperature	-55	+100	°C	-

Table 11: Absolute maximum ratings.

Recommended Operating Conditions

Parameter	Min	Max	Units	Notes
VIN supply voltage	2.4	5.5	V	EN5311QI data sheet
3.3VIN supply voltage	3.135	3.465	V	3,3V ± 5%
HR I/O banks supply voltage (VCCO)	1.14	3.465	V	Xilinx datasheet DS181
HR I/O banks input voltage	-0.20	VCCO + 0.2	V	Xilinx datasheet DS181
Voltage on JTAG pins	3.135	3.465	V	3,3V ± 5%

Table 12: Recommended operating conditions.

Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial: -40°C to +85°C.

Operating temperature range depends also on customer design and cooling solution. Please contact Trenz Electronic for options.

> ⚠ Please check Xilinx datasheet DS181 for complete list of absolute maximum and recommended operating ratings.

Physical Dimensions

- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8mm
- PCB thickness: 1.4mm+/-10%
- Highest part on PCB: approx. 2.5mm. Please download the step model for exact numbers.

All dimensions are shown in millimeters.

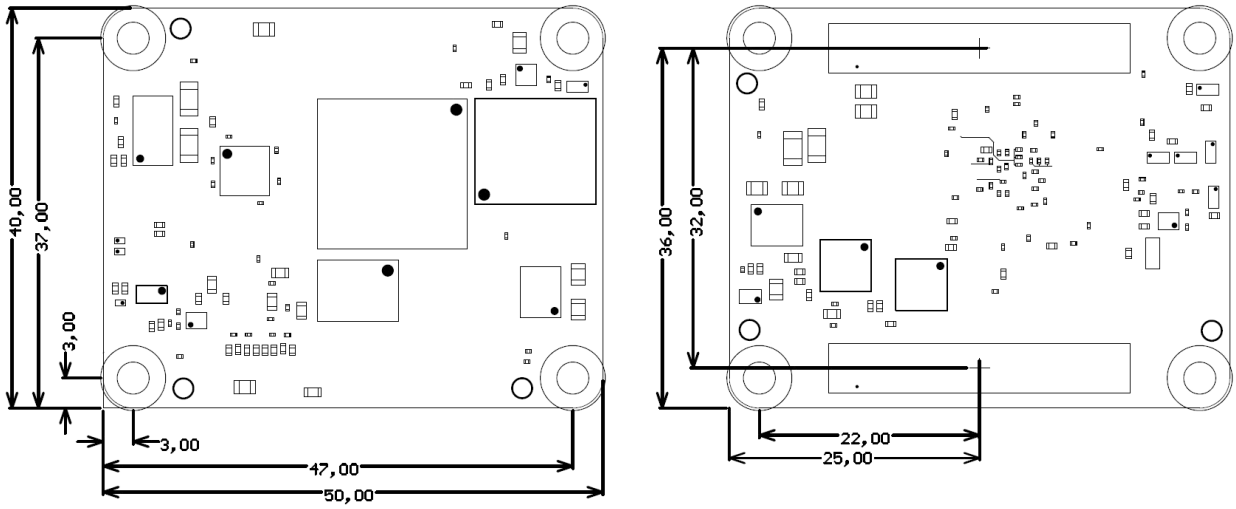


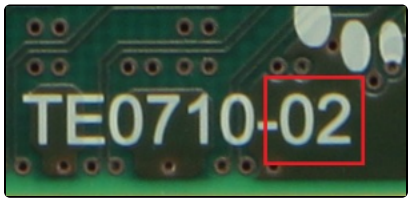
Figure 3: Physical dimensions of the TE0710-02 SoM.

Revision History

Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
2014-03-07	02	Current hardware version		TE0710-02
	01	First production release		

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.



Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• correction pcb thickness • change history style
2018-04-20	v.9	John Hartfiel	• Update power rail section
2017-11-10	v.5	John Hartfiel	• Replace B2B connector section
2017-01-26	v.4	Jan Kumann	• New block diagram.
2017-01-24	v.3	Jan Kumann	• SC I/O pins section improved.

2017-01-01	v.2	Jan Kumann	• TRM revision.
2015-01-23	v.1	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• Initial version.

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Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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REACH, RoHS and WEEE

REACH

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WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]