TE0723 TRM

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Overview

The Trenz Electronic TE0723 is a Arduino compatible Zynq board with numerous on-board peripherals based on the Xilinx Zynq XC7Z010 SoC.

Key Features

- Xilinx Zynq XC7Z010 SoC
- Dual ARM Cortex A9
- 512 MByte DDR3L SDRAM

- 16 MByte quad SPI Flash memory
- Hi-speed USB2.0 ULPI transceiver
- 23 FPGA I/O's available on board-to-board connectors
- Micro SD Card socket with card detect signal
- Micro USB OTG
- On-board USB JTAG and UART
- RGB LED (connected to PL I/O)
- "Done" LED (inverted polarity)
- CERN Open Hardware Licence 1.2

Additional assembly options are available for cost or performance optimization upon request.

Block Diagram

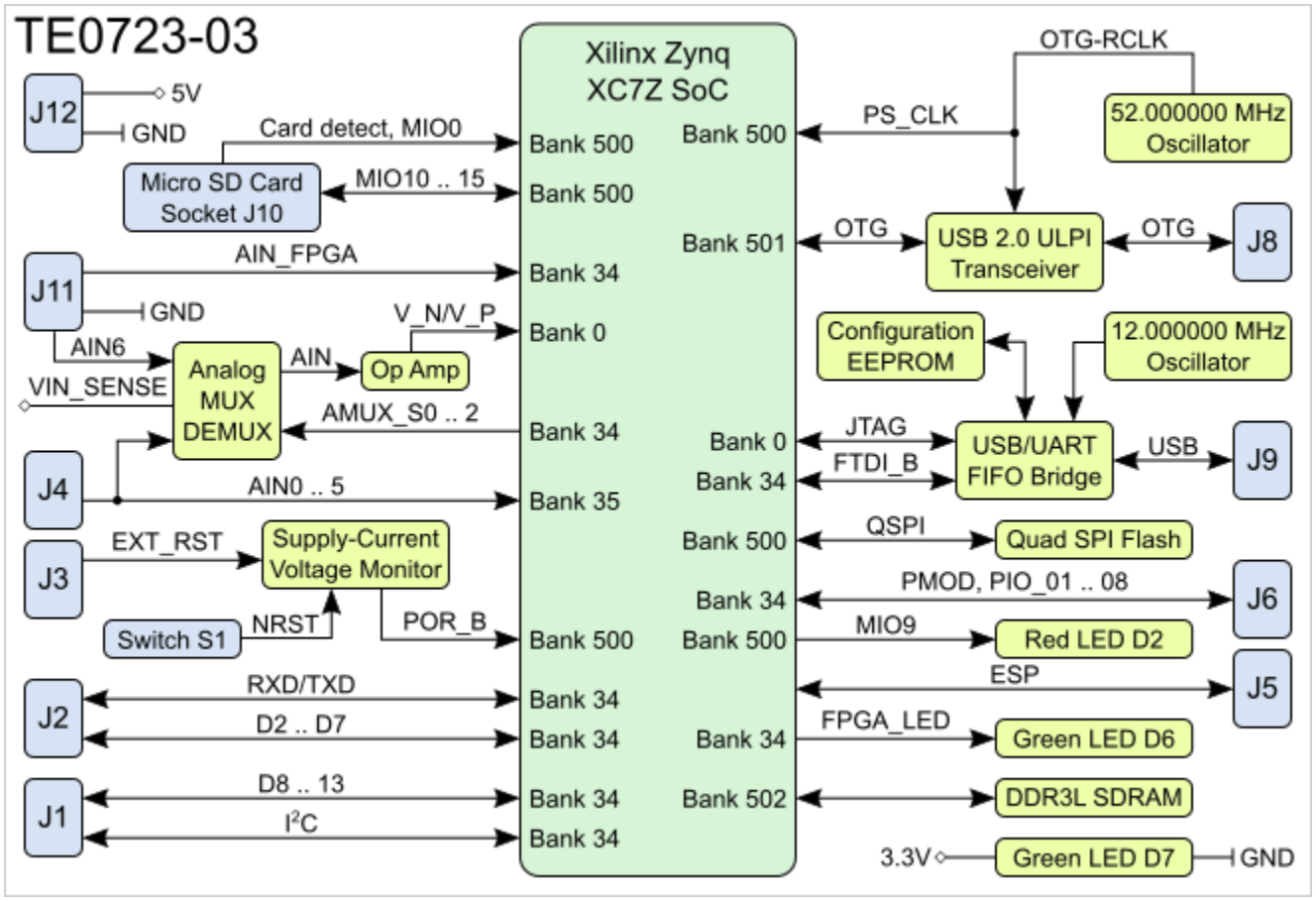

Figure 1: TE0723 block diagram

Main Components

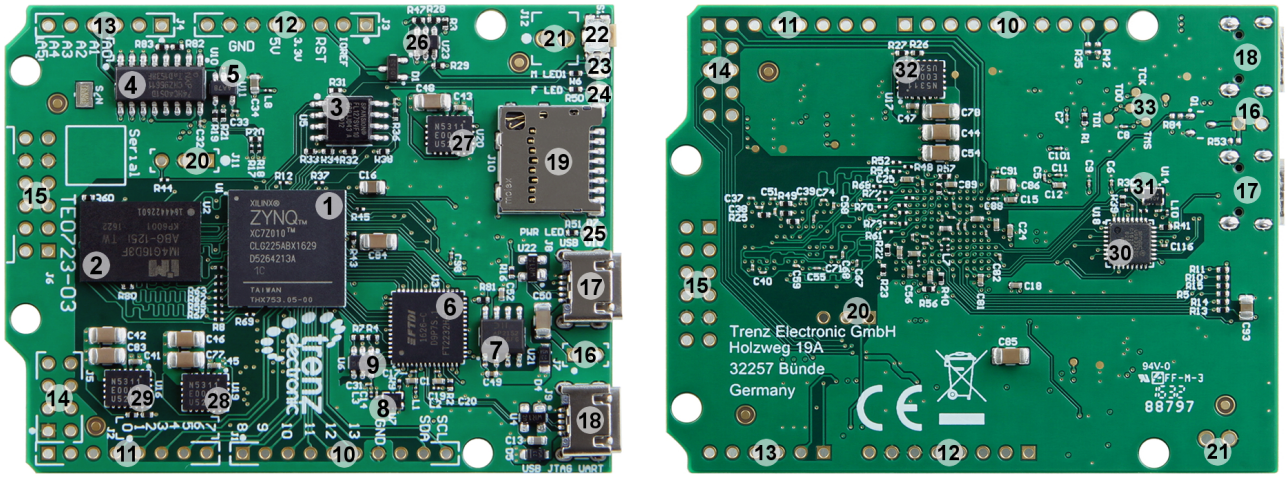

Figure 2: Main components of the TE0723 module

1. Xilinx Zynq XC7Z010 SoC, U1
2. 4 Gbit DDR3L 256M x 16 SDRAM, U2
3. 16 MByte quad SPI Flash memory, U5
4. High-speed CMOS logic analog multiplexer/demultiplexer, U10
5. 1 MHz low-power operational amplifier, U11
6. Dual high-speed USB to multipurpose UART/FIFO, U3
7. 0.5A dual-channel current-limited power switch, U21
8. Low-power programmable oscillator @ 12.000000 MHz, U7
9. 2-Kbit Microwire compatible serial EEPROM, U6
10. 10-pin header, J1
11. 8-pin header, J2
12. 10-pin header, J3
13. Analog input header, J4
14. 2 x 4-pin header, J5
15. PMod 2x6 interface header, J6
16. USB host mode jumper, J7
17. Micro USB 2.0 Type-B receptacle, J8
18. Micro USB 2.0 Type-B receptacle, J9
19. Micro SD card connector with detect signal, J10
20. Analog input select jumper, J11
21. 5V supply power input, J12
22. Reset switch, S1
23. Red LED, D2
24. Green LED, D6
25. Green LED, D7
26. Ultra-low supply-current voltage monitor, U23
27. 1A PowerSoC DC-DC converter (3.3 V), U20
28. 1A PowerSoC DC-DC converter (1.8 V, U19
29. 1A PowerSoC DC-DC converter (1.35 V), U16
30. Hi-speed USB 2.0 ULPI transceiver, U18
31. Low-power programmable oscillator @ 52.000000 MHz, U14
32. 1A PowerSoC DC-DC converter (1.0 V), U17
33. JTAG interface testpoints, TP1-TP4

Initial Delivery State

Storage device name	IC	Content	Notes
Quad SPI Flash	U5	Empty	-
Configuration EEPROM	U6	Pre-Programmed	Xilinx License

Table 1: Initial delivery state of programmable devices on the module

Boot Process

The 7 boot mode strapping pins (MIO2 ... MIO8) of the Xiliny Zynq Z-7010 device are hardware programmed on the board. They are evaluated by the Zynq device soon after the 'POR_B'.signal is deasserted to begin the boot process (see section "Boot Mode Pin Settings" of Xilinx manual UG585).

The TE0723 Zynq board is hardware programmed to boot initially from the on-board QSPI Flash memory U5. The JTAG interface of the module is provided for storing the data to the QSPI Flash memory through the Zynq device.

Signals, Interfaces and Pins

I/O Signals on Connectors

Overview of the Zynq SoC PS/PL banks I/O signals connected to the external connectors:

Bank	Type	Connector	I/O Signal Count	Voltage	Notes
34	HR	J1	8	3.3V	Signal Schematic names: 'SCL', 'SDA', 'D8' ... 'D13'.
34	HR	J2	8	3.3V	Signal Schematic names: 'RXD', 'TXD', 'D2' ... 'D7'.
34	HR	J6	8	3.3V	Signal Schematic names: 'PIO01' ... 'PIO08'.
34	HR	J11	1	3.3V	Signal Schematic name: 'AIN_FPGA'.
35	HR	J4	6	3.3V	Signal Schematic names: 'AIN0' ... 'AIN5', usable as differential analog inputs or regular digital I /O's.
35	HR	J5	1	3.3V	Connector dedicated to ESP8266 module.
500	MIO	J10	7	3.3V	SDIO interface to SD Card socket.
501	MIO	J5	4	3.3V	Connector dedicated to ESP8266 module.

Table 2: Overview of the Zynq SoC's PS/PL banks I/O signals

Zynq SoC I/O Banks

Bank	Type	VCCIO	I/O Signal Count	Available on Connectors	Notes
34	HR	3.3V	44	25	8 user I/O's on Pmod connector J6, female pin header J1 and J2 each. 1 I/O on pin header J11.
35	HR	3.3V	8	7	6 user I/O's on female pin header J4, 1 user I/O on female pin header J5.
500	PS MIO	3.3V	15	-	6 MIO pins used for QSPI flash memory interface, 7 MIO pins used for SD Card interface, 1 MIO pin connected to red LED D2, 1 MIO pin as reset pin routed to USB PHY U18, 'POR_B'-signal is connected to voltage monitor circuit 23.
501	PS MIO	3.3V	16	4	12 MIO pins used for USB ULPI interface, 4 MIO pins used for ESP8266 interface header J5.
0	Config	3.3V	4	-	4 I/O's are dedicated to JTAG interface.

Table 3: General overview of Zynq SoC PL/PS I/O bank

USB2 to JTAG/UART Adapter

The TE0723 board is equipped with the FTDI FT2232H USB2 to JTAG/UART adapter controller connected to micro-USB2 connector J9 to provide JTAG and UART access to the Xilinx Zynq XC7Z010 SoC. There is also a 256-byte configuration EEPROM U6 wired to the FT2232H chip via Microwire bus which holds pre-programmed license code to support Xilinx programming tools.

> Do not access the FT2232H EEPROM using FTDI programming tools, doing so will erase normally invisible user EEPROM content and invalidate stored Xilinx JTAG license. Without this license the on-board JTAG will not be accessible any more with any Xilinx tools. Software tools from FTDI website do not warn or ask for confirmation before erasing user EEPROM content.

Channel A of the FTDI IC is configured as JTAG interface (MPSSE) connected to the JTAG interface of the Zynq SoC on configuration bank 0:

Zynq SoC U1	Signal Schematic Name	FT2232H IC U3 Pin
Pin G9	TCK	12
Pin L7	TDI	13
Pin L8	TDO	14
Pin L9	TMS	15

Table 4: JTAG interface signals

14 additional bus lines of Channel B of the FTDI IC are routed to Zynq SoC PL bank 34 and are available to the user. The FTDI chip which converts signals from USB2 to a variety of standard serial and parallel interfaces like UART and user GPIO's in FIFO mode. Refer to the FTDI data sheet to get information about the capacity of the FT2232H IC.

Zynq SoC U1	Signal Schematic Name	FT2232H IC U3 Pin
Bank 34, pin H13	BDBUS0	32
Bank 34, pin H14	BDBUS1	33
Bank 34, pin J15	BDBUS2	34
Bank 34, pin J14	BDBUS3	35
Bank 34, pin K15	BDBUS4	37
Bank 34, pin L15	BDBUS5	38
Bank 34, pin L14	BDBUS6	39
Bank 34, pin M15	BDBUS7	40
Bank 34, pin M14	BCBUS0	42
Bank 34, pin N14	BCBUS1	46
Bank 34, pin P15	BCBUS2	47
Bank 34, pin N13	BCBUS3	48
Bank 34, pin R15	BCBUS4	49
Bank 34, pin P14	BCBUS7	53

Table 5: FTDI FT2232H bus line signals

Quad SPI Interface

Quad SPI Flash memory (U5) is connected to the Zynq PS QSPI0 interface via PS MIO bank 500, pins MIO1 ... MIO6.

Zynq SoC U1 Pin	Signal Schematic Name	Flash memory U5 Pin
Bank 500, pin MIO1	SPI0_CS	1
Bank 500, pin MIO2	SPI0_DQ0/MIO2	5
Bank 500, pin MIO3	SPI0_DQ1/MIO3	2
Bank 500, pin MIO4	SPI0_DQ2/MIO4	3
Bank 500, pin MIO5	SPI0_DQ3/MIO5	7
Bank 500, pin MIO6	SPI0_SCK	6

Table 6: Quad SPI interface signals

SD Card Interface

TE0723 module has on-board 3.3V SD Card socket (J10) with card detect switch wired to the SoC PS MIO bank 500.

Zynq SoC U1 Pin	Signal Schematic Name	Connected to
Bank 500, pin MIO0	Card detect switch	J10-9
Bank 500, pin MIO10	DAT0	J10-7
Bank 500, pin MIO11	CMD	J10-3
Bank 500, pin MIO12	CLK	J10-5
Bank 500, pin MIO13	DAT1	J10-8
Bank 500, pin MIO14	DAT3	J10-1
Bank 500, pin MIO15	CD/DAT3	J10-2

Table 7: SD Card socket signals

USB2 Interface

High-speed USB2 interface is provided by USB3320 from Microchip (U18). The USB2 PHY is connected via ULPI interface to the Zynq SoC PS USB0, bank 501 and pins MIO28 ... MIO39.

The USB2 interface is accessible through the micro-USB2 B connector J8 and enables device, host or OTG modes. For host mode, the on-board USB2 interface provides the USB-VBUS supply voltage with nominal 4.75V to 5.25V on micro-USB2 connector pin J8-1. To configure host mode on this interface, the board has to be supplied with 5V through pin header J12 or with the USB-VBUS supply voltage of micro-USB2 connector J9, which is connected to the FTDI FT2232H chip.

The USB-VBUS supply voltage enabling the host mode on USB2 interface J8 is switched by the on-board power distribution switch AP2152SG-13 from Dio des Incorporated. The voltage is switched on with the signal 'VBUS_V_EN' which is controlled by the USB2 PHY U18. If the output load exceeds the current-limit threshold, the AP2152SG-13 limits the output current and pulls the over-current low-active logic output signal 'USB_OC' low, which is routed to the Zynq PL bank 35, pin F15.

An extra 100µF decoupling capacitor (in addition to 4.7µF) can be activated on-board to stabilize the USB-VBUS host supply voltage furthermore. This can be done by fitting and closing jumper J7, fitting 0-Ohm-resistor R53 or MOSFET transistor Q1. The transistor Q1 allows to enable and disable this 100µF ex tra capacitor by the signal 'HOST_MODE_EN' routed to the Zynq PL bank 34, pin L13.

Following table shows the signal assignment of the USB PHY U18 with the Zynq PS MIO bank 501:

Zynq SoC U1 Pin	Signal Schematic Name	USB2 PHY U18 Pin
Bank 501, pin MIO28	OTG-DATA4	7
Bank 501, pin MIO29	OTG-DIR	31
Bank 501, pin MIO30	OTG-STP	29
Bank 501, pin MIO31	OTG-NXT	2
Bank 501, pin MIO32	OTG-DATA0	3
Bank 501, pin MIO33	OTG-DATA1	4
Bank 501, pin MIO34	OTG-DATA2	5
Bank 501, pin MIO35	OTG-DATA3	6
Bank 501, pin MIO36	OTG-CLK	1
Bank 501, pin MIO37	OTG-DATA5	9
Bank 501, pin MIO38	OTG-DATA6	10
Bank 501, pin MIO39	OTG-DATA7	13

Table 8: USB interface signals

ESP8266 Wi-Fi Interface

Interface for the ESP8266 Wi-Fi module is provided through connector J5.

Zynq SoC U1 Pin	Signal Schematic Name	Connected to
Bank 501, pin MIO48	ESP_TXD	J5-2
Bank 501, pin MIO49	ESP_RXD	J5-7
Bank 501, pin MIO52	MOD_RST	J5-6
Bank 501, pin MIO53	ESP_GPIO0	J5-3
Bank 35, pin G15	ESP_GPIO2	J5-5

Table 9: ESP8266 Wi-Fi module interface

I²C Interface

I^{2}C interface pins SCL and SDA from the Zynq SoC PL bank 34 are connected to the connector J1. There are no on-board I²C slave devices. The two I²C bus lines 'SDA' and 'SCL' can be optionally pulled up to 3.3V on-board by fitting the 0-Ohm-resistors R35 ('SDA') and R42 ('SCL').

Zynq SoC U1 Pin	Signal Schematic Name	Connected to
R13	SDA	J1-9
P13	SCL	J1-10

Table 10: Zynq SoC I^{2}C interface

Analog Input Interface

The TE0723 board provides up to 7 muxed analog input pins to the XADC unit of the Zynq device. 6 pins are exposed to female pin header J4, 1 to male pin header J11. The pins are muxed by the TI High Speed CMOS 8-Channel Analog Multiplexer CD74HC4051 (U10). There is between the analog output of the multiplexer IC and the differential analog input of the Zynq device an operational amplifier (U11) configured in voltage-follower circuit transforming the single analog output signal of the multiplexer IC to the differential analog signal, which is connected to the differential XADC input pins of the Zynq device, pin G7, H7.

The analog input channels can be selected by the pins 'AMUX_SO', 'AMUX_S1' and 'AMUX_S2', which are connected to the Zynq PL bank 34, pin G12, H12, G11:

Analog Input Channel	[AMUX_S2:AMUX_S1:AMUX_S0]	Connector pin	Note
AIN0	000	J4-1	-
AIN1	001	J4-2	-
AIN2	010	J4-3	-
AIN3	011	J4-4	-
AIN4	100	J4-5	-
AIN5	101	J4-6	-
AIN6	110	J11-1	-
VIN_SENSE	111	-	half divided 5V input supply voltage

Table 11: Selecting multiplexer analog input channels

Another feature of the analog interface capacities of the XADC units of the Zynq device are the Auxiliary Analog Inputs of the Zynq device's PL bank 35 (see Xilinx document UG480, section 'Auxiliary Analog Inputs'). With 6 pins of female pin header J4 3 analog differential pairs can be created:

Analog differential Input Pin Pair	Connector pin	Signal Schematic Name	Note
IO_L1P_T0_AD0P_35, pin F12 IO_L1N_T0_AD0N_35, pin E13	J4-3 J4-1	AIN2 AIN0	I/O's also usable in digital mode
IO_L2P_T0_AD8P_35, pin F11 IO_L2N_T0_AD8N_35, pin E12	J4-4 J4-2	AIN3 AIN1	I/O's also usable in digital mode
IO_L3P_T0_DQS_AD1P_35, pin F13 IO_L3N_T0_DQS_AD1N_35, pin F14	J4-6 J4-5	AIN5 AIN4	I/O's also usable in digital mode

Table 12: Auxiliary Analog Inputs of the Zynq device

Note: These 6 auxiliary analog inputs pins are analog inputs are shared with PL bank pins and can be used as regular digital I/O's.

On-board Peripherals

DDR Memory

TE0723 module has up to 512-MBytes of DDR3L SDRAM arranged into 32-bit wide memory bus providing total of 1 GBytes of on-board RAM. Different memory sizes are available optionally.

Quad SPI Flash Memory

On-board quad SPI Flash memory S25FL127S (U5) is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application storage. All four SPI data lines are connected to the Zynq SoC's PS, allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the bus width and clock frequency used.

FTDI FT2232H IC

The FTDI chip U3 converts signals from USB2.0 to a variety of standard serial and parallel interfaces. Refer to the FTDI data sheet to get information about the capacity of the FT2232H chip.
FTDI FT2232H chip is used in MPPSE mode for JTAG, 14 I/O's of Channel B are routed to PL bank 34 of the Zynq SoC and are usable for example as UART interface.

The configuration of FTDI FT2232H chip is stored with Xllinx License on EEPROM U6. Please note the warning in section "USB2 to JTAG/UART Adapter" to not overwrite or delete the Xilinx License on the EEPROM U6.

Microwire Serial EEPROM

There is a 2-Kbit (128 x 16-bit organization) Microwire compatible serial EEPROM 93AA56B (U6) connected to the FTDI FT2232H dual high-speed USB2 to multipurpose UART/FIFO (U3). This external EEPROM allows each of the FTDI FT2232H chip's channels to be independently configured as a serial UART (RS232 mode), parallel FIFO (245) mode or fast serial (optical isolation). The external EEPROM can also be used to customize the USB VID, PID, serial number, product description strings and power descriptor value of the FT2232H for OEM applications. Other parameters controlled by the EEPROM include remote wake up, soft pull down on power-off and I/O pin drive strength.

High-speed USB2 ULPI PHY

Hi-speed USB2 ULPI PHY (U18) is provided with USB3320 from Microchip. The ULPI interface is connected to the Zynq SoC's PS USB0 via MIO28..39, bank 501 (see also section). The I/O voltage is fixed at 3.3V and PHY reference clock input is supplied from the on-board 52.000000 MHz oscillator (U14).

Oscillators

The module has following reference clock signals provided by on-board oscillators:

Source	Signal	Frequency	Destination	Pin Name	Notes
U14	PS_CLK	52.000000 MHz	U1	PS_CLK_500	Zynq SoC PS subsystem main clock.
U14	OTG-RCLK	52.000000 MHz	U18	REFCLK	USB3320C PHY reference clock.
U7	OSCI	12.000000 MHz	U3	OSCI	FT2232H oscillator input.

Table 13: Reference clock signals

On-board LEDs

There are three LEDs on-board TE0723:

LED	Color	Connected to	Description and Notes
D2	Red	Zynq PS bank 500, pin MIO9	User LED.
D6	Green	Zynq PL bank 34, pin G14	User LED.
D7	Green	3.3V	Indicating 3.3V voltage level.

Table 14: On-board LEDs

Push Buttons

The TE0723 board is equipped with one push buttons S1:

Button	Signal Schematic Name	Connected to	Notes
S1	NRST	Voltage Monitor Circuit, U23	Triggers system reset.

Table 15: Push buttons of the module

Power and Power-On Sequence

To power-up a module, power supply with minimum current capability of 1A is recommended.

Power Supply

5V power can be supplied by the external power supply through connector J12 or via USB connection to the host system through USB connector J8 or J9. Minimum current capability of 1A for external power supply is recommended.

Following diagram shows the dependencies of the power supply:

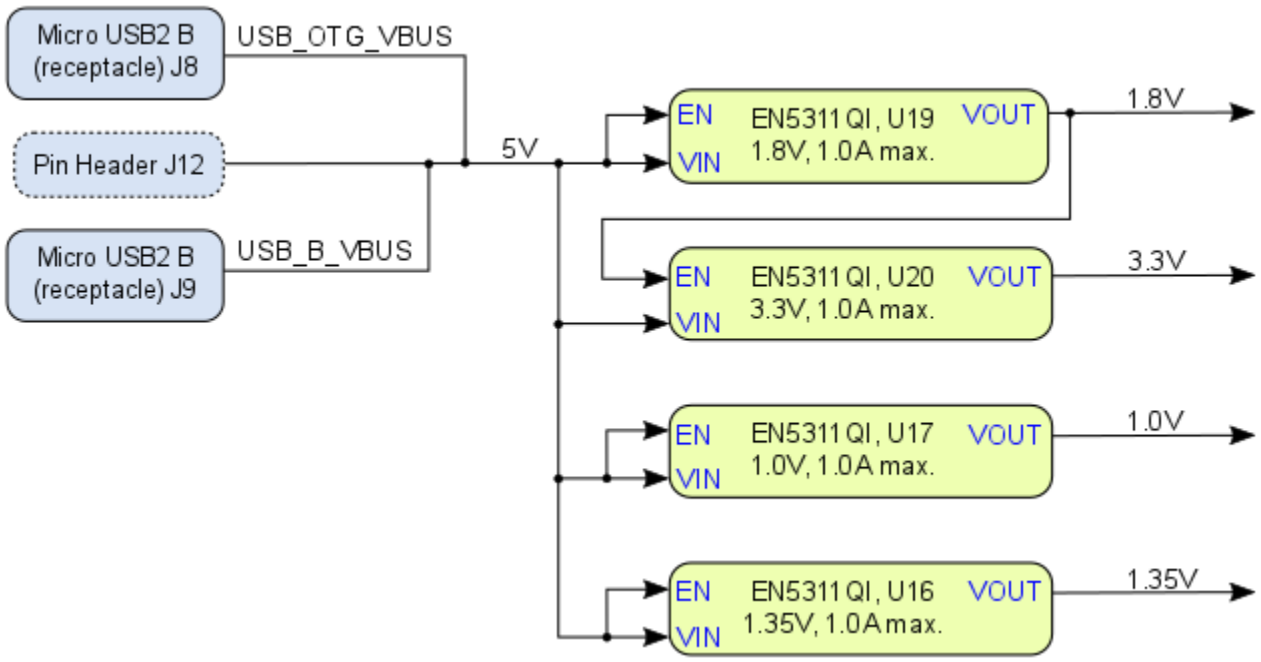

Figure 3: Module power supply dependencies

Power Consumption

Power consumption is to be determined by the user and depends on SoC's FPGA design and connected hardware.

Board Variant	FPGA	Design	Typical Power, 25°C ambient
TE0723-02	XC7Z010-1CLG225C	Not configured	TBD*
TE0723-03M	XC7Z010-1CLG225C	Not configured	TBD*
TE0723-03-07S-1C	XC7Z007S-1CLG225C	Not configured	TBD*

Table 16: Module power consumption

Power-On Sequence

There is no specific power-on sequence, system will power-up automatically when 5V is present either through J8, J9 or J12.

Voltage Monitor Circuit

The voltages 1.0V (core voltage) and 3.3V are monitored by the voltage monitor circuit U23, which generates the POR_B reset signal at power-on. A manual reset is also possible by driving the connector pin J3-3 ('EXT_RST') to GND (leave this pin unconnected or connect to VDD (3.3V) when unused) or press switch button S1, which is assigned to the signal 'NRST'.

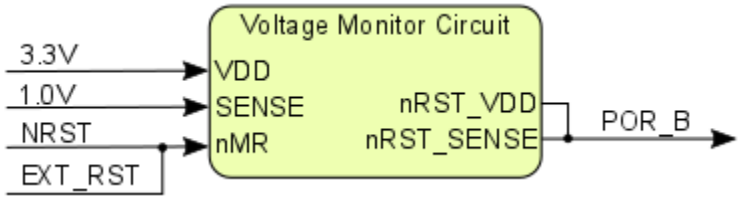

Figure 4: Voltage monitor circuit

Power Rails

The voltage direction of the power rails is directed at on-board connectors' view:

Main Power Pins Designator	VCC / VCCIO	Direction	Pins	Notes
J12	5V	In	1	5V power supply pin header.
J3	3.3V	Out	2, 4	On-board 3.3V voltage level available.
	5V	In / Out	5	On-board 5.0V voltage level available or supply pin.

Table 17: Main power pin header description

I/O pin header	VCC / VCCIO	Direction	Pins	Notes
J5	3.3V	Out	4, 8	I/O header VCCIO.
J6	3.3V	Out	6, 12	I/O header VCCIO.

Table 18: Power pin description of I/O pin header

Peripheral Socket Designator	VCC / VCCIO	Direction	Pins	Notes
J8 / J9	USB-VBUS	In / Out	1	Direction depends on USB2 mode.
J10	3.3V	Out	4	MikroSD Card socket VDD.

Table 19: Power pin description of peripheral connector

Bank Voltages

Bank	Bank I/O Voltage VCCO	Voltage Range
0 (config)	3.3V	fixed
500 (MIO)	3.3V	fixed

501 (MIO)	3.3V	fixed
34 (HR)	3.3V	fixed
35 (HR)	3.3V	fixed

Table 20: Board bank voltages

Variants Currently in Production

Board Variant	Xilinx Zynq SoC	DDR3L SDRAM	ARM Cores	PL Cells	LUTs	Flip-Flops	Block RAM	DSP Slices	Zynq SoC Operating Temp.	Temp. Range
TE0723-02	XC7Z010-1CLG225C	128 MBytes	Dual-core	28K	17,6K	35,2K	2.1 MBytes	80	0°C to +85°C	Commercial
TE0723-03M	XC7Z010-1CLG225C	512 MBytes	Dual-core	28K	17,6K	35,2K	2.1 MBytes	80	0°C to +85°C	Commercial
TE0723-03-07S-1C	XC7Z007S-1CLG225C	512 MBytes	Single-core	23K	14,4K	28,8K	1.8 MBytes	66	0°C to +85°C	Commercial

Table 21: Board variants

Technical Specifications

Absolute Maximum Rating

Parameter	Min	Max	Units	Reference Document
5V power supply voltage	4.75	5.25	V	USB2.0 VBUS voltage specification
HR PL I/O banks input voltage (VCCIO single ended)	-0.4	VCCO + 0.55	V	Xilinx datasheet DS187 (VCCO 3.3V nominal)
PS MIO I/O banks input voltage (VCCIO single ended)	-0.4	VCCO + 0.55	V	Xilinx datasheet DS187 (VCCO 3.3V nominal)
Analog Multiplexer IC pins input voltage	0	3.3V	V	TI CDx4HC405x data sheet
Storage temperature	-40	+85	°C	WL-SMCW SMD LED data sheet

Table 22: Board absolute maximum ratings

Recommended Operating Conditions

Parameter	Min	Max	Units	Reference Document
5V power supply voltage	4.75	5.25	V	USB2.0 VBUS voltage specification
HR PL I/O banks input voltage (VCCIO single ended)	-0.20	VCCO + 0.20	V	Xilinx datasheet DS187 (VCCO 3.3V nominal)
PS MIO I/O banks input voltage (VCCIO single ended)	-0.20	VCCO + 0.20	V	Xilinx datasheet DS187 (VCCO 3.3V nominal)
Analog Multiplexer IC pins input voltage	0	3.3V	V	TI CDx4HC405x data sheet
Operating Temperature Commercial	0	+85	°C	Xilinx datasheet DS190

Table 23: Board recommended operating conditions

Please check Xilinx datasheet DS187 for complete list of absolute maximum and recommended operating ratings for the Zynq-7 device.

Physical Dimensions

- Module size: 68.58 mm × 53.34 mm. Please download the assembly diagram for exact numbers.
- PCB thickness: 1.6 mm.
- Highest part on PCB: approx. 4 mm. Please download the step model for exact numbers.

Please note that two different units are used on the figures below, SI system millimeters (mm) and imperial system thousandths of an inch(mil). To convert mils to millimeters and vice versa use formula 100mil's = 2,54mm.

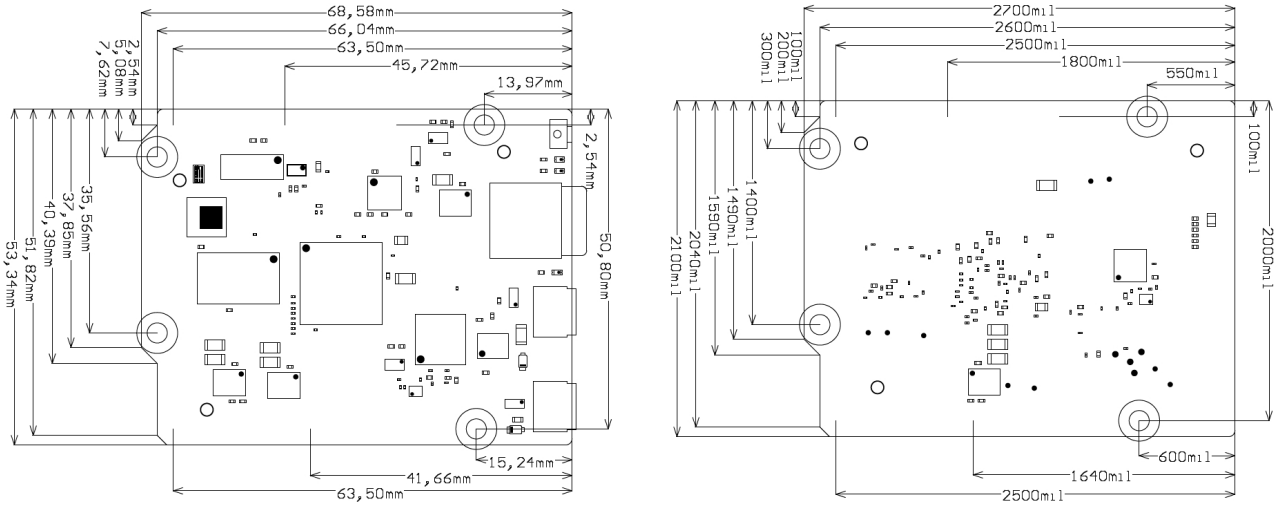

Figure 5: Board physical dimensions

Revision History

Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
2016-07-15	03	Refer to Changes list in Schematic for further details in changes to REV02	-	TE0723-03
2015-11-06	02	Second Production Release	-	TE0723-02
-	01	First Production Release	-	-

Table 24: Board hardware revision history

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.

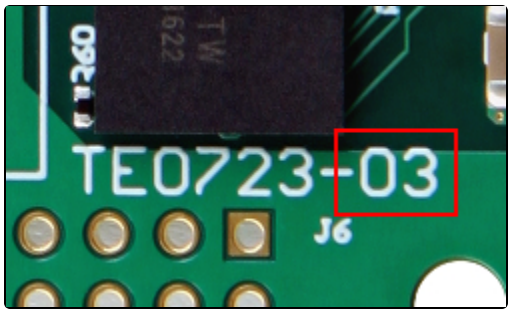

Figure 6: TE0723 board hardware revision number

Document Change History

Date	Revision	Contributors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	Unknown macro: 'metadata'	Ali Naseri, Jan Kumann	• First TRM release

Table 25: Document change history.

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Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]