FAQ

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https://shop.trenz-electronic.de/en/Products/Trenz-Electronic/

EOL of our module series is normally as long as Xilinx and Intel will offer the FPGA/SoC:

Passive components (resistors, capacitors) or components which will not influence the FPGA or HW design can be changed on the modules without notification. We use different manufacturer and best prices, but in any case the characteristics which are specified in the schematics are the same.

In case other active components will be not longer available, we will replace with footprint compatible equivalent alternatives or we update the PCB to support a equivalent alternatives variant. In case we change such a component, we will create also a new article number, so that you can directly see that something was be updated and we write a PCN

Trenz Electronic provides Module series with different assembly options (FPGA size, speed grade, temperature range, DDR size, QSPI size, eMMC size, less components, different stacking height...) Identification can be done with the Article number and the corresponding Schematics in the download area of the modules. Module series name and PCB revision is directly printed on the module. Every module has also an unique serial (number on white sticker with QR code on the module), which can be used to identify the whole article number (and thus the assembly options).
Article number style has changed since 2019, so that you can identify main parts also with the article number encoding table:

Article Number Information

Xilinx device information can be requested with the 2D Bare code or Lot code on the device package.

This can be done via Xilinx App:

- https://www.xilinx.com/about/xilinxgo-app-support.html
- https://www.xilinx.com/video/corporate/introduction-2d-barcode-markings.html

Or over web page:

- https://www.xilinx.com/member/2dbarcode.html

In both cases a Xilinx login is needed.

Deviations from the general copyrights, if any, are indicated at the corresponding boards. If not the following applies:

Copyright for most board with SoC/FPGA (Modules / Motherboards...):

- Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified.
- Modules are protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.
- Schematics and other handouts serve for informational purposes only!

Copyright for most Carrier:

- Carrier are Open Source Hardware and therefore free to use, adapt and can be modified to suit your needs as described
  in the "The MIT License".
- Permission is hereby granted, free of charge, to any person obtaining a copy of this hardware and associated documentation files (the "Product"), to deal in the Product without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Product, and to permit persons to whom the Product is furnished to do so.
- Schematics and other handouts serve for informational purposes only!

Downloads / Documents

You can lookup for file abbreviations on Documents Naming Conventions.

PCB document is available on our wiki pages and download area.

PCB Design

Cooling solution depends mainly on FPGA design and environment. This must therefore always be considered individually.

Trenz Electronic cooling solutions for some modules:

- Cooling Solutions

Xilinx documentation:

- https://www.xilinx.com/support/documentation/user_guides/ug865-Zynq-7000-Pkg-Pinout.pdf
- https://www.xilinx.com/support/documentation/user_guides/ug1075-zynq-ultrascale-pkg-pinout.pdf
- https://www.xilinx.com/support/documentation/user_guides/ug475_7Series_Pkg_Pinout.pdf
- https://www.xilinx.com/support/documentation/user_guides/ug575-ultrascale-pkg-pinout.pdf
- https://www.xilinx.com/support/documentation/application_notes/xapp1301-mechanical-thermal-design-guidelines.pdf

The maximum power consumption of a module manly depends on the design which is running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to generate power consumption of the developed design with Vivado.

Please also observe the TRM of the Trenz Electronic module and the power management of our corresponding carrier boards.

Other related documentation:

- wp482 - Managing Power and Performance with the Zynq UltraScale+ MPSoC

Module pinout files can be generated with our Master Excel Pinout Sheet. You can also use the schematic on our download area.

Trenz Electronic Modules which are offered in the shop are listed on our shop page grouped by FPGA-Family. Wiki overview of the different series is available on Products

See Xilinx Answer Record: AR# 43989

Power sequencing of the FPGA/SoC banks and IOs must be still fulfil restrictions from manufacturer data sheet.

In most case IOs should be enabled after core voltages are powered on. Some module output voltage can be used to enable carrier power regulator for variable bank powers and connected periphery.

See also data-sheet power sequencing of the section of the give device:

7 Series:

- https://www.xilinx.com/support/documentation/data_sheets/ds189-spartan-7-data-sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds181_Artix_7_Data_Sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds182_Kintex_7_Data_Sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds183_Virtex_7_Data_Sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds187-XC7Z010-XC7Z020-Data-Sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds191-XC7Z030-XC7Z045-data-sheet.pdf

U/U+ Series:

- https://www.xilinx.com/support/documentation/data_sheets/ds892-kintex-ultrascale-data-sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds893-virtex-ultrascale-data-sheet.pdf
- https://www.xilinx.com/support/documentation/data_sheets/ds925-zynq-ultrascale-plus.pdf

U+ RFSoC

- https://www.xilinx.com/support/documentation/data_sheets/ds926-zynq-ultrascale-plus-rfsoc.pdf

Xilinx AR#

- AR# 37347 | 7 Series FPGAs - Will driving the I/Os of an unpowered bank cause damage to the part? Do 7 Series devices support hot swap?
- AR# 65036 | UltraScale/UltraScale+ FPGAs - Will driving the I/Os of an unpowered bank cause damage to the part?
- AR# 50802 | 7 Series, UltraScale, and UltraScale+ - What state are the I/Os in at power up?
- AR# 44225 | 7 Series Power Sequencing - Hot-swap/-plug capability
- AR# 45985 | 7 Series - How do you limit reverse biasing of VCCO when input is being driven by a 3.3V signal before Vcco is powered?

Xilinx Forum

- ZynqMP HD Bank Sequencing

Use in Altium, Design "Create integrated library" It will recreate all used lib symbols

These connectors do not self align, so the placement has to be good initially. Connectors should be placed with 50µm accuracy. Not every assembly house can do this. However even with higher tolerances, the connection is normally stable.
We had one customer, who made a mistake in layout, offsetting one connector 125µm in x and 125µm in y. He still had connections, but noticed this only on the MGTs. They failed with high data rates.

Regarding Samtec Product specification: In Revision F of this document 7.1.1 Samtec defines max allowed misaligned 0.03mm, in Revision D it was 0.08mm. Also the recommendation (7.3) you are referring was not there when we designed and tested this B2B interface.
There is also a document describing general multiple connector applications:

- http://suddendocs.samtec.com/processing/multi-connector_applications.pdf

Furthermore we discussed with Samtec and got following hints:

- The Multiple Connector Applications document covers the processing and layout requirements as well as we can. There are not any specific processing requirements for the SX5 components that are not covered in the document.
- The customer should verify that they are following the recommended PCB and Stencil Layouts: SS5, ST5.
- We have seen in our trials with lead-free solder that the components will have a tendency to stay right where they are placed. With a tin-lead soldering process, components are more likely to self-center.
- We recommend .005" Stencil thickness.
- If the components are not placed into the solder paste, but rather just sitting on top with no indentation of the paste, there could be more of a tendency to swim.
- If it is known that the placement is 'perfect', issues with the reflow oven could be causing misalignment: Vibration of the conveyor and/or imbalanced air flow from the convection fans.

As we saw the alignment issue with a few customers, we decided to make a sister series of TE0803, TE0807, TE0808 with other connectors.
These are: TE0813 / TE0817 / TE0818 with self aligning Samtec ADM6 B2B connectors
Samtec ADx have very good self alignment capabilities. We made tests with 6 connectors on one board, and there were no problems. The development of these boards is finished and the first boards will be produced in Q3 2021. If you have any reason for redesign anyway, you could consider using this series. We can sent you module footprint, if you want.

Vivado/SDK/SDSoC/PetaLinux

Links to Xilinx Release Notes are available on Vivado/SDK/SDSoC: Xilinx Software-Product Update Release Notes and Known Issues

Reference Designs will be delivered as scripted project file. Vivado Project files will be generated with these scripts.

Windows and Linux (since Vivado 2016.4) start up command files are available to generate the project: Project Delivery QuickStart

All other options are described on: Vivado Projects - TE Reference Design

Trenz Electronic Board Part Files will be delivered with the reference designs on our download area. They ca be installed in different ways.

1. Select the correct Board Part File: TE Board Part Files
2. Install Board Part Files: Board Part Installation
3. Use Board Part Files: Vivado Board Part Flow

Xilinx Documentation is available on Xilinx Hompage. Some helpful documentation and Links are available on AMD Development Tools

We provide PetaLinux template projects instead of BSPs for our modules. This template are included in our reference design in the subfolder (os/petalinux).

They are available on our download area. You can lookup for instructions on: PetaLinux KICKstart

Xilinx provide a list with supported functionality and devices on: https://www.xilinx.com/products/design-tools/vivado/vivado-webpack.html

1. Activate ES License with Xilinx License Manager
2. Enable Beta Devices for Vivado
    a. open existing init.tcl (create new one if not exist) in one of this locations:
        i. C:/Xilinx/Vivado/<version>/scripts/
        or
        ii. C:/Users/<user>/AppData/Roaming/Xilinx/Vivado/
    b. Add line: enable_beta_device *

Now Vivado check all Beta Devices, but only Devices with valid license are visible. With Beta Device enable, Vivado need longer startup. Select special beta device is supported too. See Xilinx Forum: Synthesis Failure for ZCU102

Insufficient external power supply can cause this issue. If power supply is insufficient, module restarts and FPGA content is erased. Vivado did not recognize this.

Please check following:

1. Xilinx Programming Cable drivers are installed correctly
2. "hw_server.exe" is terminated on task manage after all xilinx programs are closed. (if not kill this process or restart PC)
3. Board Power Supply is sufficient and on
4. JTAG USB Cable is connected to module and PC

Check if the Quad Enable (QE) bit in the Configuration Register of the flash is set to 1. If the QE-Bit is set or not depends on the last access to the flash.

- This will be done automatically, when you configure Flash with Vivado or SDK and Flash in the design is specified as X4.
- This will be not always done automatically, when you use other software to get access. For example Xilinx barmetal lib doesn't check if the QE bit is set or not.