TE0711 TRM

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Overview

Trenz Electronic TE0711 is an industrial-grade FPGA module integrating a Xilinx Artix-7 FPGA, 32 MByte Quad SPI Flash memory for configuration and operation and powerful switching-mode power supplies for all on-board voltages. Numerous configurable I/O's are provided via rugged high-speed strips. All this on a tiny footprint, smaller than a credit card size at very competitive price. All Trenz Electronic SoM's in 4 x 5 cm form factor are mechanically compatible.

Key Features

- Industrial-grade Xilinx Artix-7 (15T to 100T) FPGA, supported by the free Xilinx Vivado WebPACK tool
- Rugged for shock and high vibration
- FTDI FT2232H USB 2.0 high-speed to UART/FIFO
- 32 MByte QSPI Flash memory (with XiP support)
- 100 MHz MEMS oscillator
- Plug-on module with 2 × 100-pin and 1 × 60-pin high-speed hermaphroditic strips
- 178 FPGA I/Os (84 differential pairs) are available on board-to-board connectors
- On-board high-efficiency DC-DC converters

    - 4.0 A x 1.0 V power rail
    - 1.0 A x 1.8 V power rail
    - 1.0 A x 1.5 V power rail
- System management and power sequencing
- eFUSE bit-stream encryption
- AES bit-stream encryption
- User LED
- Evenly-spread supply pins for good signal integrity

Assembly options for cost or performance optimization available upon request.
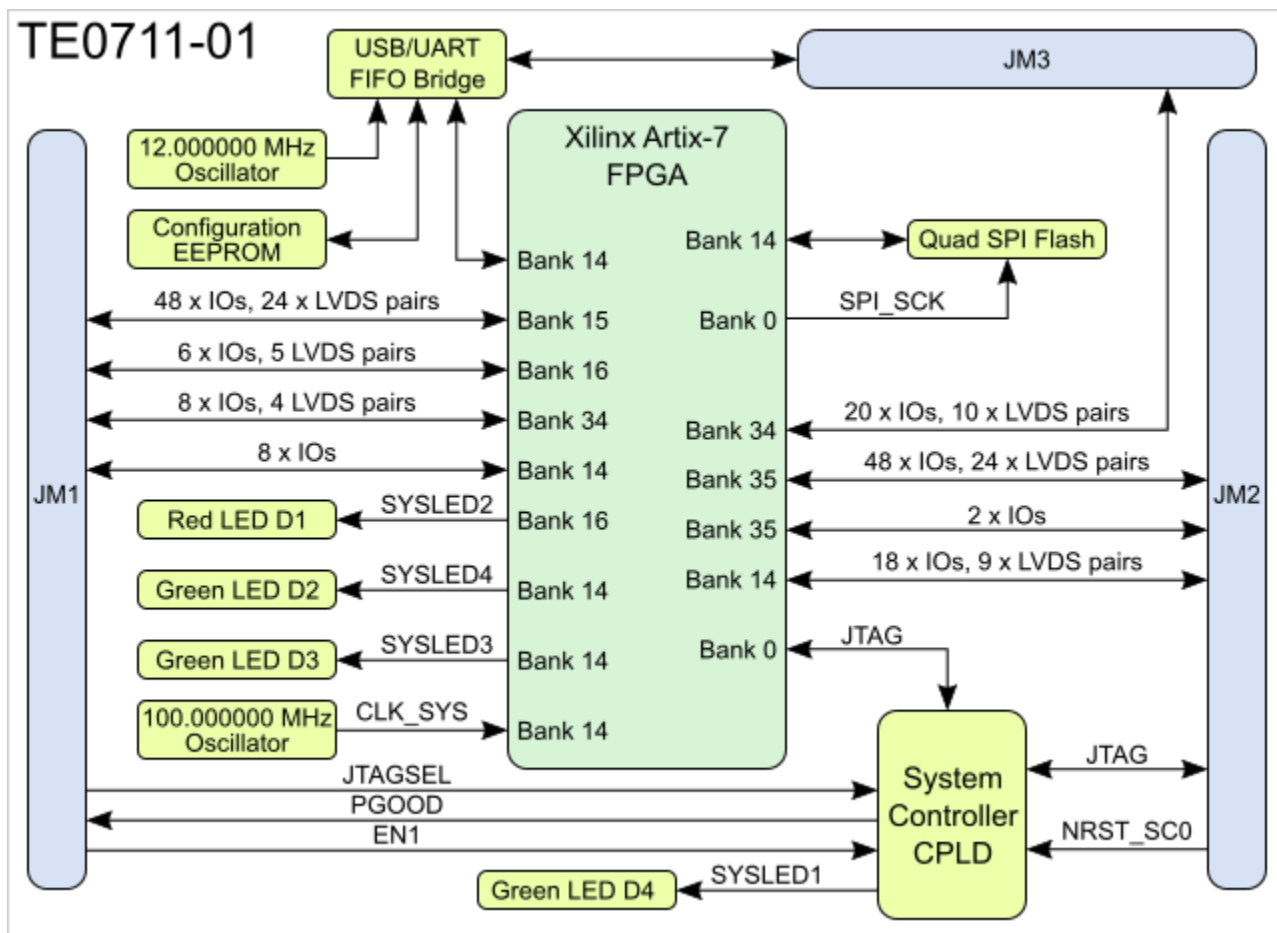
Block Diagram

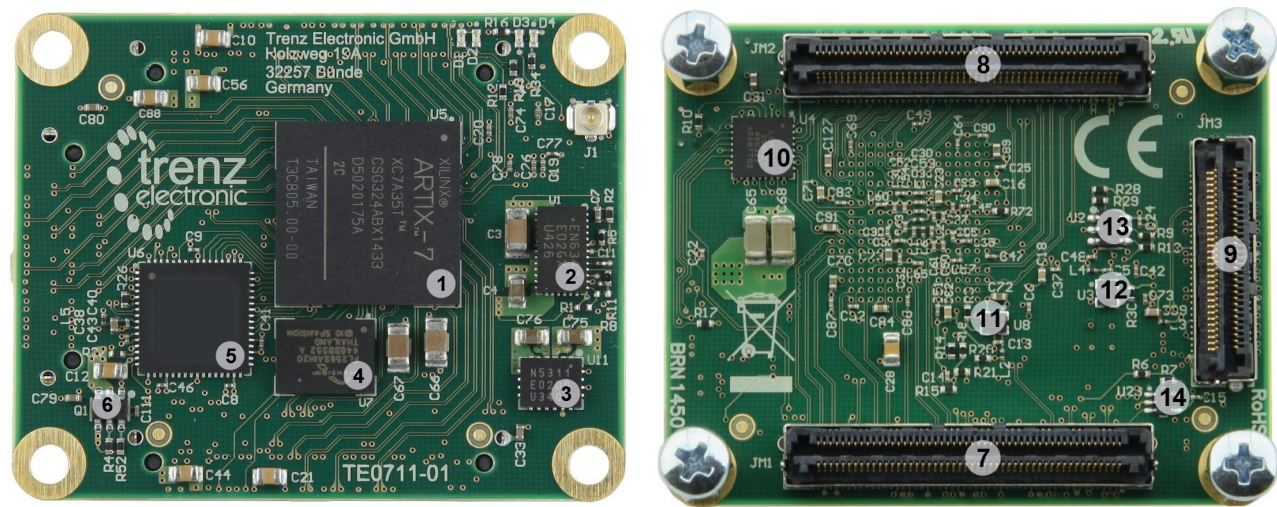**Figure 1:** TE0711-01 block diagram.

Main Components

Figure 2: TE0711-01 PCB.

1. Xilinx Artix-7 FPGA, U5
2. 4A PowerSoC DC-DC converter for 1.0V (Altera EN6347QI), U1
3. 1A PowerSoC DC-DC converter for 1.8V (Altera EN5311QI), U11
4. 32 MByte Quad SPI Flash memory 32 MByte Quad SPI Flash memory (Cypress S25FL256S), U7
5. Dual USB to UART/FIFO bridge (FTDI FT2232H), U6
6. Load switch for 3.3V voltage level (Texas Instruments TPS27082L), Q1
7. B2B connector Samtec Razor Beam™ LSHM-150, JM1
8. B2B connector Samtec Razor Beam™ LSHM-150, JM2
9. B2B connector Samtec Razor Beam™ LSHM-130, JM3
10. System Controller CPLD (Lattice Semiconductor LCMXO2-256HC), U4
11. 100.000000 MHz reference clock connected to the FPGA bank 14 (SiTime SiT8008), U8
12. 12.000000 MHz reference clock connected to the USB to UART/FIFO bridge (SiTime SiT8008), U3
13. Configuration data serial EEPROM for USB to UART/FIFO bridge (Microchip 93AA56), U2
14. Voltage detector for "Power OK" signalling (Texas Instruments TPS3805H3), U23

Initial Delivery State

Storage Component	Content	Notes
SPI Flash OTP Area	Empty, not programmed	Except serial number programmed by flash vendor.
SPI Flash Quad Enable bit	Programmed	-
SPI Flash main array	Demo design	-
EFUSE USER	Not programmed	-
EFUSE Security	Not programmed	-

Table 1: TE0711-01 initial delivery state.

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

I/O signals connected to the FPGA's I/O banks and B2B connector:

Bank	Type	B2B Connector	I/O Signal Count	Voltage	Notes
14	HR	JM1	8 I/O pins	3.3V	HR banks support voltages from 1.2V to 3.3V.
		JM2	18 I/O pins, (9 LVDS pairs)		See Xilinx Artix-7 datasheet (DS181) for voltage ranges.
15	HR	JM1	48 I/O pins	User	As above.
			24 LVDS pairs		
16	HR	JM1	6 I/O pins	1.8V	As above.
			3 LVDS pairs		
34	HR	JM1	48 I/O pins	User	As above.
		JM3	24 LVDS pairs		
35	HR	JM2	50 I/O pins	User	As above.
			24 LVDS pairs		

Table 2: Voltage ranges and pin-outs of available logic banks of the FPGA.

Refer to Master Pin-out Table as primary reference for the pin mapping information.

JTAG Interface

JTAG access to the Xilinx Artix-7 and to the System Controller CPLD is provided through B2B connector JM2.

JTAG Signal	B2B Connector
TCK	JM2-99
TDI	JM2-95
TDO	JM2-97
TMS	JM2-93

Table 3: Pin mapping of JTAG Interface on B2B connector

> ⚠ JTAGSEL pin on B2B connector JM1 is used to control which physical device is accessible via JTAG interface. If this pin is set to low or left open, JTAG interface is enabled for Xilinx Artix-7 FPGA, if set to high, JTAG interface for System Controller CPLD will be enabled.
>
> The use of Xilinx legacy development tools (ISE, iMPACT) is not recommended. iMPACT does not recognize any Xilinx Artix-7 below A100T model.

System Controller I/O Pins

Special purpose pins are connected to smaller System Controller CPLD and have following default configuration:

Pin Name	Mode	Function	Default Configuration	B2B Connector
STAT_SC2	Output	Power Good	Active high when all on-module power supplies are working properly.	JM1-30
NRST_SC0	Input	Reset	Active low reset signal, drive low to keep the system in reset (FPGA pin PROG_B will be driven by CPLD).	JM2-18

JTAGSEL	Input	JTAG Select	Low for normal operation, high (3.3V) to program the System Controller CPLD.	JM1-89
EN_SC3	Input	Enable FPGA Core Voltage supply	High (3.3V) or open for normal operation, low to stop power-on sequencing.	JM1-28

Table 4: Pin description of System Controller CPLD.

On-board LEDs

The TE0711 SoM has total of 4 on-board LED's. LED's D1, D2 and D3 are connected to the Xilinx Artix-7 FPGA and can be freely used by user design. LED D4 is the System Controller CPLD status LED.

LED	Color	Connected to	Description and Notes
D1	Red	SYSLED2	User LED, active HIGH, connected to FPGA Pin A8
D2	Green	SYSLED4	User LED, active HIGH, connected to FPGA Pin R17
D3	Green	SYSLED3	User LED, active LOW, connected to FPGA Pin L15
D4	Green	SYSLED1	System Controller status LED, connected to CPLD

Table 5: Description of on-board LED's.

Clocking

The TE0711-01 is equipped with MEMS oscillator (SiT8008AI-73-XXS-100.000000E, U8) to provide 100 MHz clock signal for Xilinx Artix-7 FPGA pin P17.

On-board Peripherals

32 MByte Quad SPI Flash Memory

On-board SPI flash memory S25FL256S (U7) is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the bus width and clock frequency used.

> ⚠ SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash. By default this bit is set to high at the manufacturing plant.

System Controller CPLD

The system controller is used to coordinate the configuration of the FPGA. The FPGA is held in reset (by driving the PROG_B signal) until the power supplies have sequenced. Low level at NRST_SC0 pin also resets the FPGA. This signal can be driven from the user's PCB via the B2B connector pin JM2-18. Input EN_SC3 is also gated to FPGA Reset and should be open or pulled up for normal operation. EN_SC3 low turns off on board DC-DC converters and stops power-on sequencing.

It is possible for the user to create their own system controller design using the Lattice Diamond software. Once created the design can be programmed into the device using the JTAG pins. The signal JTAGSEL should be set to 3.3V to enable programming mode. For normal operation it should be set to 0V.

There are one status LED connected to the system controller CPLD. When the FPGA is not configured the LED will flash continuously. Finally once FPGA configuration has completed the LEDs can be used in the user's FPGA design.

Dual channel USB to UART/FIFO

The TE0711-01 SoM has on-board high-speed USB 2.0 to UART/FIFO FT2232H controller from FTDI. Channel A can only be used in simple UART mode. Channel B can be used as UART in FT245 FIFO mode, JTAG (MPSSE) mode or in high-speed serial modes.

FT2232H controller is connected to the FPGA bank 14 with fixed 3.3V VCCIO and all signalling must meet the LVCMOS 3.3V I/O standard.

256 Byte EEPROM is connected to the FT2232H-chip to store custom configuration settings. These settings can be changed using FTDI provided tools that can be downloaded from FTDI website.

Power and Power-On Sequence

Power Supply

Power supply with minimum current capability of 2A for system startup is recommended.

Power Input Pin	Voltage Range	Max Current
VIN	3.3V to 5.5V	Typical 200mA, depending on customer design and connections.
3.3VIN	3.3V	Typical 50mA, depending on customer design and connections.

Table 6: Typical power consumption.

> ⊘ VIN and VIN3.3V can be connected to the same power source (3.3V).

Lowest power consumption is achieved when powering the module from single 3.3V supply. When using split 3.3V/5V supplies the power consumption (and heat dissipation) will rise, this is due to the DC/DC converter efficiency (it decreases when VIN/VOUT ratio rises).

Power-On Sequence

For highest efficiency of on board DC-DC regulators, it is recommended to use same 3.3V power source for both VIN and 3.3VIN power rails. Although VIN and 3.3VIN can be powered up in any order, it is recommended to power them up simultaneously.

It is important that all baseboard I/O's are 3-stated at power-on until System Controller sets STAT_SC2 signal high (B2B connector JM1, pin 30), or 3.3V is present on B2B connector JM2 pins 10,12 or 91, meaning that all on-module voltages have become stable and module is properly powered up.

See Xilinx Artix-7 datasheet DS181 for additional information. Also check related baseboard documentation when choosing baseboard design for TE0711-01 module.

A 3.3V supply is also needed and must be supplied from the user's PCB. An output 3.3V supply is available on some of the board connector pins (see section 'Power Rails'). The input 3.3VIN will be switched to the internal 3.3V voltage level after the FPGA 1.0V supply has stabilized. Than 3.3V supply will be available on the B2B connector pins.

The regulators can be powered from the 3.3V supply or a 5V supply if preferred. The options for powering the board are as follows:

- Apply 5V to pins VIN and 3.3 to pins 3.3VIN on the board connector
- Apply 3.3V to pins VIN and 3.3VIN on the board connectors.

Power Rails

Voltages on B2B-Connectors	B2B JM1-Pin	B2B JM2-Pin	Direction	Note
VIN	1, 3, 5	2, 4, 6, 8	input	supply voltage
3.3VIN	13, 15	-	input	supply voltage
VCCIO15	9, 11	-	input	high range bank voltage
VCCIO34	-	1, 3	input	high range bank voltage

VCCIO35		7, 9	input	high range bank voltage
3.3V	-	10, 12	output	internal 3.3V voltage level
JTAG VREF	-	91	output	JTAG reference voltage (3.3V).
1.8V	39	-	output	internal 1.8V voltage level

Table 7: Power rails of SoM on B2B connectors.

Bank Voltages

Bank	Schematic Name	Voltage	Range
0 Config	3.3V	3.3V	-
14	3.3V	3.3V	-
15	VCCIO15	user	HR: 1.2V to 3.3V
16	1.8V	1.8V	-
34	VCCIO34	user	HR: 1.2V to 3.3V
35	VCCIO35	user	HR: 1.2V to 3.3V

Table 8: Range of FPGA's bank voltages.

See the Artix7 datasheet DS181 for the allowable voltage range.

Board to Board Connectors

> ⊙ These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three Samtec Razor Beam LSHM connectors on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

Connectors.

The module can be manufactured using other connectors upon request.

Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

Speed rating.

Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

Manufacturer Documentation

File	Modified
PDF File hsc-report_lshm-lshm-05mm_web.pdf High speed test report	07 04, 2016 by Thorsten Trenz
PDF File lshm_dv.pdf LSHM catalog page	07 04, 2016 by Thorsten Trenz
PDF File LSHM-1XX-XX.X-X-DV-A-X-X-TR-FOOTPRINT(1).pdf Recommended layout and stencil drawing	07 04, 2016 by Thorsten Trenz
PDF File LSHM-1XX-XX.X-XX-DV-A-X-X-TR-MKT.pdf Technical drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189016-01.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189016-02.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189017-01.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189017-02.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File TC0923--2523_report_Rev_2_qua.pdf Design qualification test report	07 04, 2016 by Thorsten Trenz
PDF File tc0929--2611_qua(1).pdf Shock and vibration report	07 04, 2016 by Thorsten Trenz

Download All

Variants Currently In Production

Module Variant	FPGA	FPGA Junction Temperature	Operating Temperature Range
TE0711-01-35-2I	XC7A35T-2CSG324I	-40°C to 100°C	Industrial grade
TE0711-01-100-2I	XC7A100T-2CSG324I	-40°C to 100°C	Industrial grade
TE0711-01-35-2C	XC7A35T-2CSG324C	0°C to 85°C	Commercial grade
TE0711-01-100-2C	XC7A100T-2CSG324C	0°C to 85°C	Commercial grade

Table 9: Differences between TE0711-01 module variants.

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VIN supply voltage	-0.3	7.0	V	EN6347QI, EN5311QI datasheet
3.3VIN supply voltage	-0.1	3.6	V	-
HR I/O banks supply voltage (VCCO)	-0.5	3.6	V	Xilinx datasheet DS181
HR I/O banks input voltage	-0.4	VCCO + 0.55	V	Xilinx datasheet DS181
Voltage on module JTAG pins	-0.5	VCCO_0 + 0.45	V	VCCO_0 is 3.3V nominal
Storage temperature	-55	+125	°C	-

Table 10: Absolute maximum ratings.

Recommended Operating Conditions

Parameter	Min	Max	Units	Notes
VIN supply voltage	2.4	5.5	V	EN5311QI data sheet
3.3VIN supply voltage	3.135	3.465	V	3,3V ± 5%
HR I/O banks supply voltage (VCCO)	1.14	3.465	V	Xilinx datasheet DS181
HR I/O banks input voltage	-0.20	VCCO + 0.2	V	Xilinx datasheet DS181
Voltage on JTAG pins	3.135	3.465	V	3,3V ± 5%

Table 11: Recommended operating conditions.

Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial grade: -40°C to +85°C.

Module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

⚠ Please check Xilinx datasheet (DS181) for complete list of absolute maximum and recommended operating ratings.

⚠️

Physical Dimensions

- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 2.5mm. Please download the step model for exact numbers.

All dimensions are shown in millimeters.
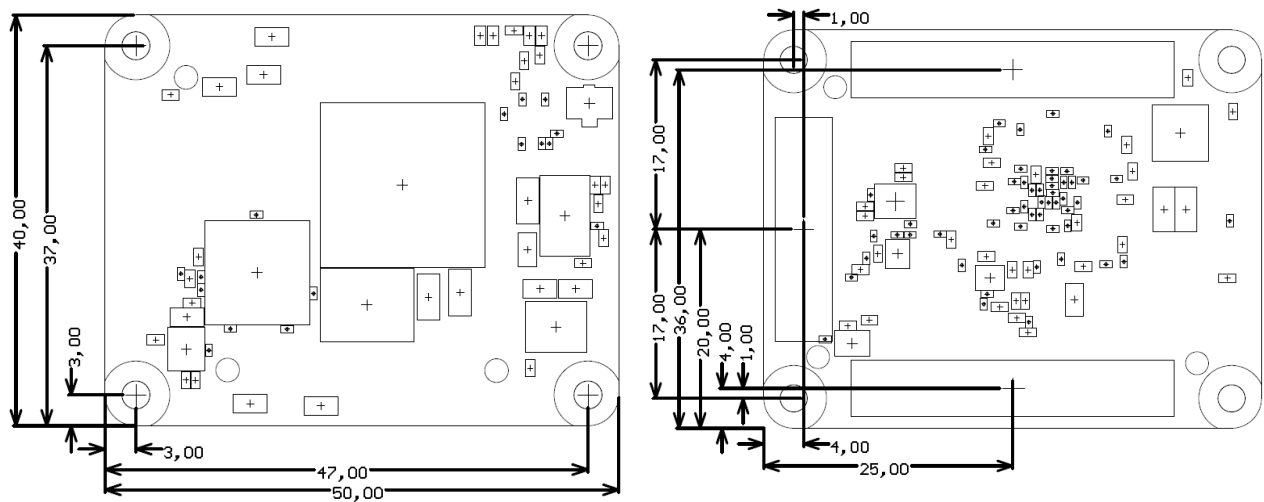
Figure 3: Physical dimensions of the TE0711-01 board.

Weight

20.6 g Plain module.

8.8 g Set of nuts and bolts.

Revision History

Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
2015-01-02	01	First production release		TE0711-01

Table 12: Hardware revisions.

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.

Document Change History

Date	Revision	Contributors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk. proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages. Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core. ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence. core.ContentEntityObject]	Unknown macro: 'metadata'	John Hartfiel	• Update Power Rail Section
2017-11-10	v.33	John Hartfiel	• Replace B2B connector section
2017-01-29	v.30	Jan Kumann	• New block diagram.
2017-01-01	v.10	Ali Naseri, Thorsten Trenz, Jan Kumann	• TRM revision.
2015-06-05	v.1	Antti Lukats	• Initial version.

Disclaimer

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]