TE0728 TRM

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Table of Contents

Overview

Trenz Electronic TE0728 is an automotive-grade FPGA module integrating an Automotive Xilinx Zynq-7 FPGA, two Ethernet transceivers (PHY) , DDR3 SDRAM, QSPI Flash memory for configuration and operation, and powerful switching-mode power supplies for all on-board voltages. Numerous configurable I/Os are provided via rugged high-speed strips.

Within the complete module only Automotive components are installed.

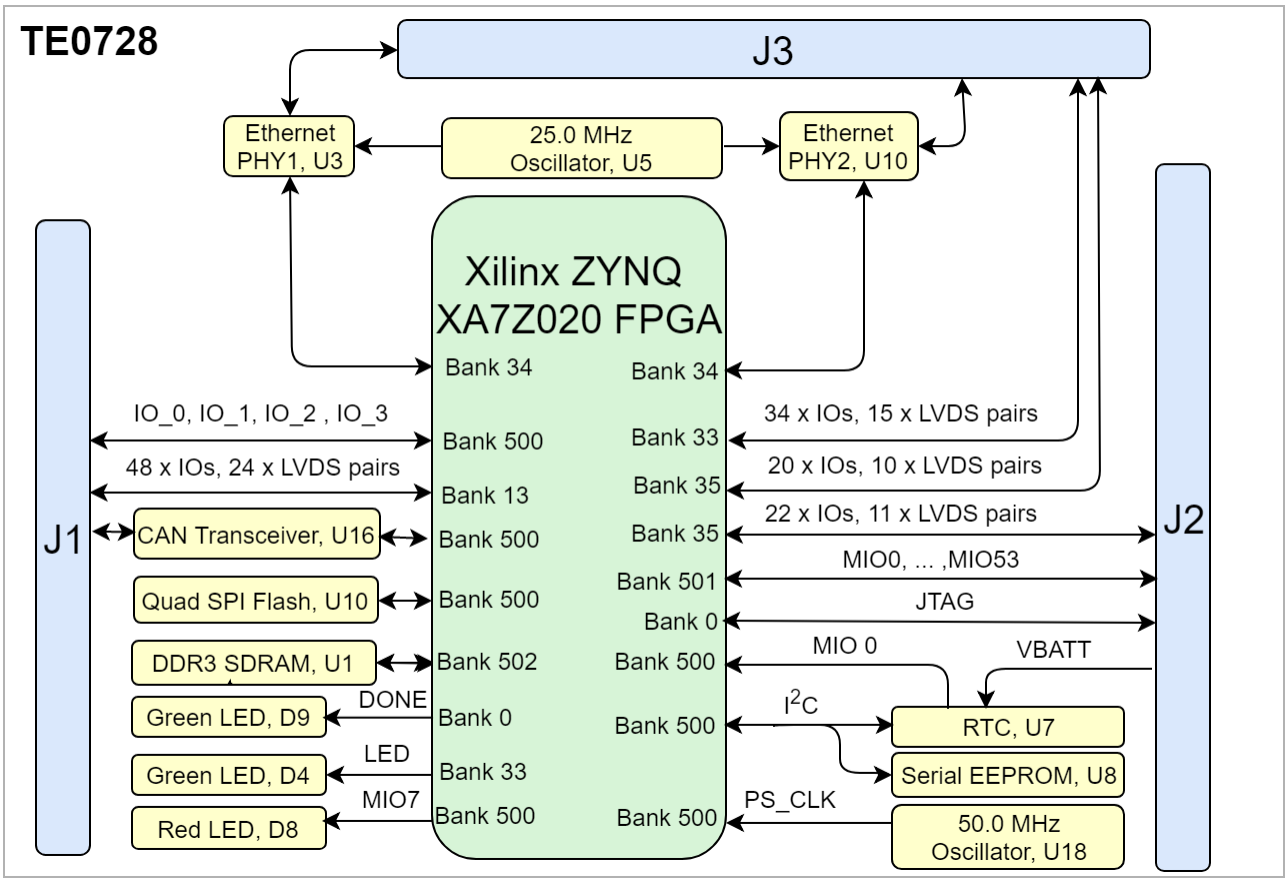
All this in a compact 6 x 6 cm form factor, at the most competitive price.

Refer to http://trenz.org/te0728-info for the current online version of this manual and other available documentation.

Key Features

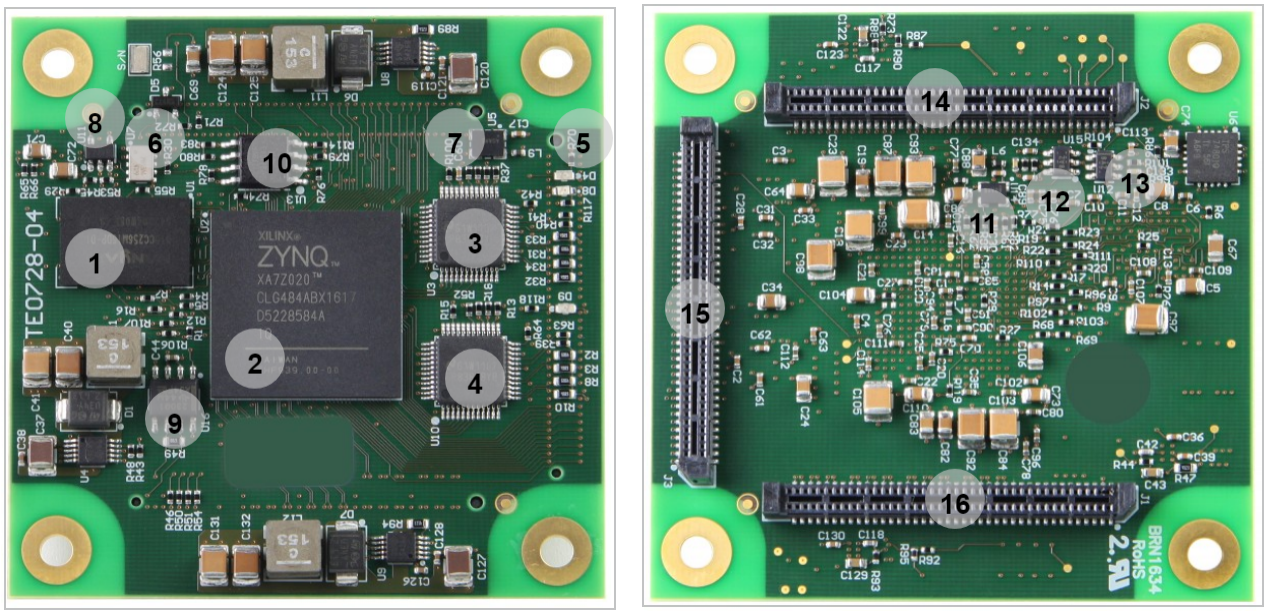
- Xilinx XC7Z020-1CLG484Q (Automotive) [XA7Z014S is available on other assembly options]
  - Package: CL/CLG484
  - Speed Grade: -1
  - Temperature Grade: Expanded (-40 to +128 °C)
- Dual-Core ARM Cortex-A9 MPCore
- DDR3 SDRAM, up to 512MB, up to 1066 Mb/s, connected to PS [different size is available on other assembly options]
- QSPI Flash memory (with XiP support) [different size is available on other assembly options]
- Programmable SIT8918A , PS clock generator
- 2 Kbit serial EEPROM
- Three user LEDs
- CAN transceiver (PHY)
- Temperature compensated RTC (real-time clock)
- 2 x 100 MBit Ethernet transceiver (PHY)
- Board to Board (B2B)
  - Plug-on module with 3 x 80-pin Samtec Micro Tiger Eye(TM) high-speed connectors
- I/O Interface
  - 42x MIO
  - 200x HR
  - 128x PS IO
  - 0x GTP Transceiver
  - 0x GTX Transceiver
- Power Supply
  - 12V power supply with watchdog
- Others:
  - Dimensions: 6 x 6 cm
  - Rugged for shock and high vibration
  - On-board high-efficiency DC-DC converters
  - System management and power sequencing
  - eFUSE bit-stream encryption
  - AES bit-stream encryption
  - Evenly-spread supply pins for good signal integrity

Block Diagram



TE0728 block diagram

Main Components



TE0728 main components

1. DDR3 SDRAM, U1
2. Xilinx Automotive XA7Z020-1CLG484Q ,U2
3. 100 MBit Ethernet transceiver, U3
4. 100 MBit Ethernet transceiver, U10
5. User LED Green, D4
6. Real Time Clock, U7
7. Standard Clock Oscillators, U5
8. 64 Kbit I2C EEPROM, U11
9. CAN Tranceiver, U16
10. QSPI NOR Flash memory, U13
11. Standard Clock Oscillators, U14
12. Low-Quiescent-Current Programmable Delay Supervisory Circuit, U15
13. Low-Quiescent-Current Programmable Delay Supervisory Circuit, U12
14. B2B connector , JM2
15. B2B connector , JM3
16. B2B connector , JM1

FPGA (U2), DDR3 SDRAM (U1) and QSPI (U13) can be varied on other assembly option, for more information contact us.

Initial Delivery State

Storage Device	Symbol	Content
Quad SPI Flash	U13	Not Programmed
EEPROM	U11	Not Programmed

Initial delivery state of programmable devices on the module

Configuration Signals

Signal	FPGA Bank	Pin	B2B	Signal State	Boot Mode

Boot_R	500	E4	J2-11	Low	QSPI
				High	SD Card

Boot process.

Signal	B2B	I/O	Note
Reset	J2-7	Input	Comes from Carrier
RST_OUT	J2-9	Output	PS_PROB_B

Reset process.

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

TE0728 Module has 3 B2B connectors and every connector has 80 pins (2 row, 40 pins).

FPGA bank number and number of I/O signals connected to the B2B connector:

FPGA Bank	Type	B2B Connector	I/O Signal Count	Voltage Level	Notes
13	HR	J1	48 Single ended (24 Diff)	VCCO_13	variable from carrier
500	MIO	J1	4 Singel ended	3.3V	
501	MIO	J2	38 Singel ended	VMIO1	variable from carrier
33	HR	J3	34 Single ended (17 Diff)	3.3V	
35	HR	J3	20 Single ended (10 Diff)	3.3V	
		J2	22 Single ended (11 Diff)		

General PL I/O to B2B connectors information

Ethernet PHY

Ethernet pins connections to Board to Board (B2B). Ethernet components ETH1 and ETH2 are connected to B2B connector J3.

Schematic	ETH1	ETH2	Direction	Notes
CTREF	J3-57	J3-25	In	Magnetics center tap voltage
TD+	J3-58	J3-28	Out	Transfer
TD-	J3-56	J3-26	Out	
RD+	J3-52	J3-22	In	Receive
RD-	J3-50	J3-20	In	
LED1	J3-55	J3-23	Out	LED Yellow on carrier, multiple usage-ACK
LED2	J3-53	J3-21	Out	
LED3	J3-51	J3-19	Out	LED Green on carrier, multiple usage-Link
POWERDOWN/INT	L21	R20	In	
RESET_N	M15	R16	In	Active low PHY Reset

Ethernet PHY B2B connectors.

CAN PHY

CAN pins connections to Board to Board (B2B).

Schematic	B2B	Direction	Notes
CANH/CANL	J1-2/J1-4	Inout/Inout	

CAN B2B connectors.

JTAG Interface

JTAG access to the Xilinx XA7Z020 FPGA through B2B connector JM2.

JTAG Signal	B2B Pin
TMS	J2-12
TDI	J2-10
TDO	J2-8
TCK	J2-6

JTAG pins connection

MIO Pins

MIO Pin	Connected to	B2B	Notes
MIO0	MIO0	-	RTC interrupt
MIO1...MIO6	SPI_CS , SPI_DQ0... SPI_DQ3 SPI_SCK	-	SPI Flash
MIO7	LED RED	-	LED
MIO8/MIO9	Tx/Rx	-	CAN Transceiver
MIO10...MIO13	IO_0 ... IO_3	J1	GPIO
MIO14/MIO15	SCL/SDA	-	I2C
MIO16...MIO39	-	J2	GPIO
MIO40...MIO48	CLK, Cmd, Data0...Data3, wp, cd	J2	SD
MIO48	PS_MIO48_501	J2	LED Red on Carrier
MIO49	PS_MIO49_501	J2	LED Yellow on Carrier
MIO50	PS_MIO49_501	J2	LED Green on Carrier
MIO51	PS_MIO51_501	J2	GPIO
MIO52/MIO53	UART_Txd / UART_Rxd	J2	UART transfer/recieve

MIOs pins

On-board Peripherals

Chip/Interface	Designator	Notes
QSPI Flash	U13	---
EEPROM	U11	EEPROM
RTC	U7	Real Time Clock
DDR3 SDRAM	U1	Volatile Memory
Ethernet	U3, U10	Two 100 Mbit Ethernet PHY
CAN Transceiver	U16	---
User LED	D4	Green LED
Oscillators	U14, U7, U5	Clock Sources

On board peripherals

Quad SPI Flash Memory

On-board QSPI flash memory is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency.

Quad SPI Flash (U7) is connected to the Zynq PS QSPI0 interface via PS MIO bank 500.

MIO Pin	Schematic	Notes
MIO1	SPI_CS	
MIO2	SPI_DQ0/M0	
MIO3	SPI_DQ1/M1	
MIO4	SPI_DQ2/M2	
MIO5	SPI_DQ3/M3	
MIO6	SPI_SCK/M4	

Quad SPI interface MIOs and pins

RTC

The RTC has an I^2C Bus (2-wire SerialInterface) and offers temperature compensated time. The STC-Smart Temperature Compensation is calibrated in the factory and leads to a very high time-accuracy.

RTC interrupt is connected to MIO0 connected to Bank 500 through pin G6.

MIO Pin	I2C Address	Designator	Notes
MIO14...15	0x56	U7	Slave address

I2C Address for RTC

EEPROM

The Microchip Technology Inc. 24xx64 is a 64 Kbit Electrically Erasable PROM. The device is organized as a single block of 8K x 8-bit memory with a 2-wire serial interface. The 24xx64 also has a page write capability for up to 32 bytes of data. Functional address lines allow up to eight devices on the same bus, for up to 512 Kbits address space.

MIO Pin	I2C Address	Designator	Notes
MIO14...15	0x50	U11	Slave address

I2C address for EEPROM

LEDs

Designator	Color	Connected to	Active Level
D9	Green	DONE	Low
D8	RED	MIO7	High
D4	Green	Bank 33 - V18	High

On-board LEDs

DDR3 SDRAM

The TE0728 SoM has a volatile DDR3 SDRAM, 256Mx16bit (512MB), IC for storing user application code and data. Size of DDR3 can be varied in different assembly versions.

- Part number: NT5CB256M16CP-DIH
- Supply voltage: 1.5V
- Organization: 256M x 16 bits

DDR3 SDRAM can be varied on demand for other assembly options. DDR3 can have density of maximum 512MB due to available addressing. The maximum possible speed for DDR3 SDRAM is 1066 Mb/s.

Ethernet

There are two 100 MBit Extreme Temperature Ethernet provided by Texas Instrumen on the board. Datasheet is provided at TI website. Both PHY's are connected with all I/O Pins to FPGA Bank 34 (VCCIO = 3.3V). PHY Clock 25 MHz sources is provided from MEMS Oscillator. There is no sharing of signals for the two PHY's.

PUDC pin is connected with pull-up to 3.3V those pre-configuration pull-ups are disabled by default. Strapping resistor exist to change the PUDC mode.

Bank	Signal Name	ETH1	ETH2	Signal Description
34	ETH-RST	M15	R16	Ethernet reset, active-low.
34	ETH_COL	L16	P20	
34	MDC	P16	T17	Ethernet management clock.
34	MDIO	M16	T16	Ethernet management data.
34	ETH_TX_D0	J22	N22	Ethernet transmit data 0. Output to Ethernet PHY.
34	ETH_TX_D1	M17	P21	Ethernet transmit data 1. Output to Ethernet PHY.
34	ETH_TX_D2	K21	P22	Ethernet transmit data 2. Output to Ethernet PHY.
34	ETH_TX_D3	M22	R21	Ethernet transmit data 3. Output to Ethernet PHY.
34	ETH_TX_EN	J21	M21	Ethernet transmit enable.
34	ETH_RX_D0	L17	R18	Ethernet receive data 0. Input from Ethernet PHY.
34	ETH_RX_D1	K18	R19	Ethernet receive data 1. Input from Ethernet PHY.
34	ETH_RX_D2	J18	T18	Ethernet receive data 2. Input from Ethernet PHY.

34	ETH_RX_D3	J20	T19	Ethernet receive data 3. Input from Ethernet PHY.
34	ETH_RX_DV	N17	P15	Ethernet receive data valid.

Ethernet PHY to Zynq SoC connections

CAN Transceiver

Controller Area Network (CAN) transceivers are designed for use with the Texas Instruments TMS320Lx240x 3.3-V DSPs with CAN controllers. The datasheet is available in TI website. Each CAN transceiver is designed to provide differential transmit capability to the bus and differential receive capability to a CAN controller at speeds up to 1 Mbps.

Bank	Signal name	Notes
500	D - Tx	Driver Input
500	R - Rx	Reciever Output

CAN Tranciever interface MIOs

Oscillators

Designator	Description	Frequency	Used as
U14	MEMS Oscillator	50 MHz	PS_CLK
U5	MEMS Oscillator	25 MHz	Ethernet PHY Clock
U7	RTC (internal oscillator)	32.768 KHz	CLKOUT of RTC is not connected

Osillators

Power and Power-On Sequence

Power Supply

Power supply with minimum current capability of 2.5A for system startup is recommended.

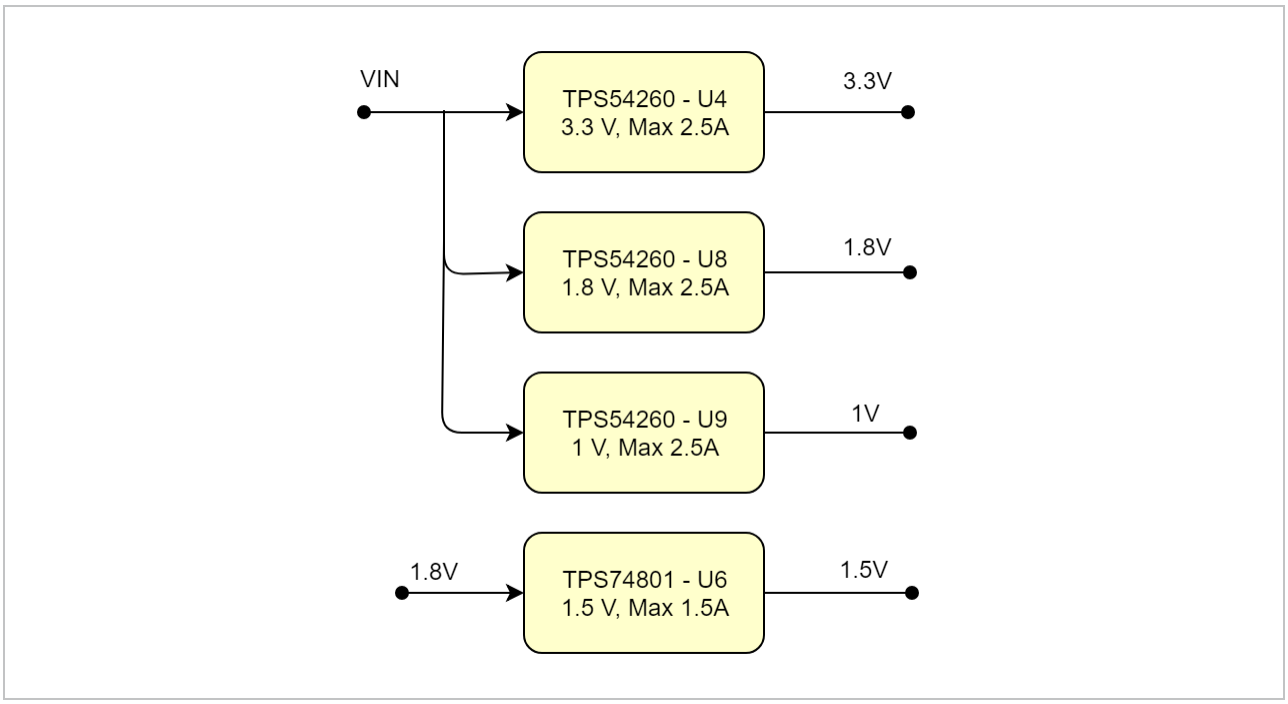
Power Consumption

Power Input Pin	Typical Current
VIN	TBD*

Power Consumption

* TBD - To Be Determined

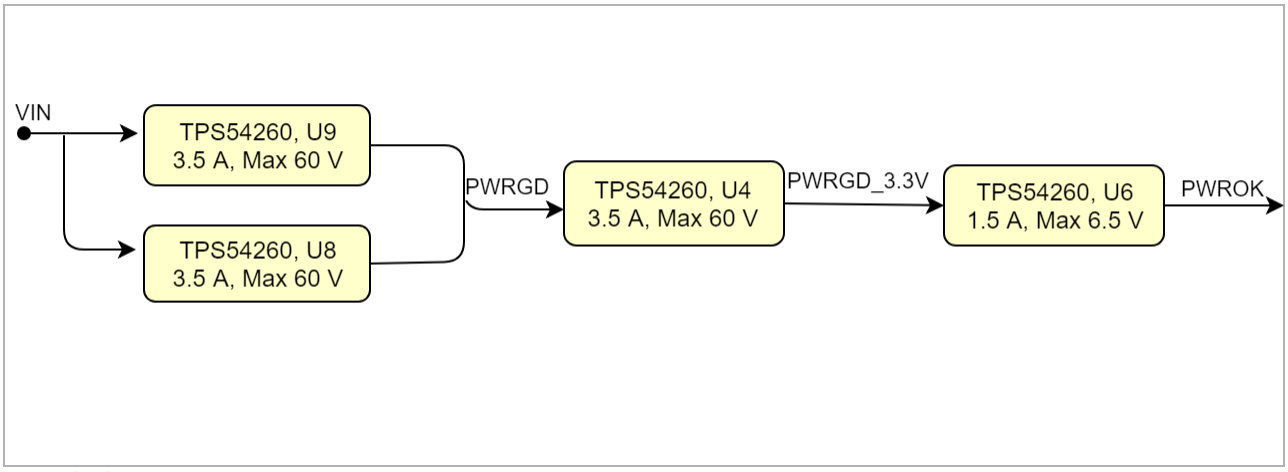
Power Distribution Dependencies



Power Dependencies

Power on Sequence

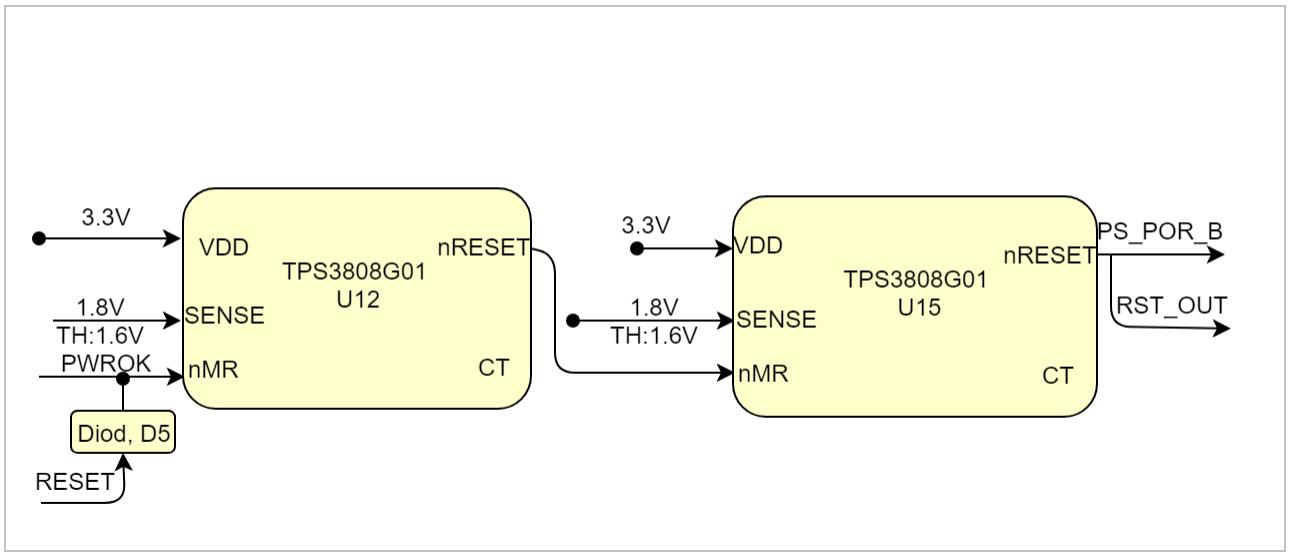
The TE07028 SoM meets the recommended criteria to power up the Xilinx Zynq properly by keeping a specific sequence of enabling the on-board DC-DC converters and regulators dedicated to the particular functional units of the Zynq chip and powering up the on-board voltages. When the U8 and U9 generates PWRGD signal, it turns on the U4 which generates PWRGD_3.3V, it turns on the U6 and it generates PWROK signal which is connected to MR. Whenever the supply voltage for U12 drops down below the threshold it resets the system. Actually it resets the system when all regulators are working.



Power On Sequence

Voltage Monitor Circuit

The microprocessor supervisory circuits monitor system voltages asserting an open-drain RESET signal when the SENSE voltage drops below a preset threshold or when the manual reset (MR) pin drops to a logic low. The RESET output remains low for the user adjustable delay time after the SENSE voltage and MR return above their thresholds. Datasheet is available in Texas Instruments website.



Voltage Monitor Circuit

Power Rails

Power Signal	B2B JM1 Pin	B2B JM2 Pin	B2B JM3 Pin	Direction	Notes
VIN	1,3	-	-	Input	Supply voltage from carrier board.
VCCO_13	39	-	-	Input	
VBATT	-	1	-	Output	RTC Supply voltage
3.3V	19	4	25,57	Output	Internal 3.3V voltage level.
VMIO	-	2		Input	Variable and supplied by carrier
1.8V	-	5	-	Output	Internal 1.8V voltage level.

Module power rails.

Bank Voltages

Bank	Schematic Name	Voltage	I/O Type	Notes
500	VCCO_MIO0_500	3.3V	MIO	
501	VCCO_MIO1_501	2.5V or 3.3V	MIO	supplied by carrier.
502	VCCO_DDR_502	1.5V	DDR3	
13	VCCO_13	1.8V or 3.3V	HR	Supplied by the carrier board. J1
33	3.3V	3.3V	HR	Supplied by carrier board. J3
34	3.3V	3.3V	HR	
35	3.3V	3.3V	HR	Supplied by the carrier board. J2, J3

Zynq SoC bank voltages.

Board to Board Connectors

6 x 6 modules use two or three Samtec Micro Tiger Eye Socket Strip on the bottom side.

- 3 x REF-189018-01 (compatible to TEM-140-02-03.0-H-D-A), (80 pins, "40" per row)

Connector Specifications	Value
Insulator material	Black Liquid Crystal Polymer
Stacking height	6 mm
Contact material	Phosphor-bronze
Plating	Au or Sn over 50 " (1.27 m) Ni
Current rating	2.9 A per pin (2 pins powered)
Operating temperature range	-55 °C to +125 °C
RoHS compliant	Yes

Connector specifications.

Connector Mating height

When using the same type on baseboard, the mating height is 6mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
26056	REF-189018-01	TEM-140-02-03.0-H-D-A	6 mm
	SEM-140-02-03.0-H-D-A	TEM-140-02-03.0-H-D-A	6 mm

Connectors.

The module can be manufactured using other connectors upon request.

Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
6 mm, Single-Ended	12 GHz
10 mm, Differential	17 GHz
6 mm, Single-Ended	14.5 GHz
10 mm, Differential	17.5 GHz

Speed rating.

Current Rating

Current rating of Samtec Micro Tiger Eye Connector™ LSHM B2B connectors is 2.9A per pin (2 adjacent pins powered).

Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

Manufacturer Documentation

File	Modified
PDF File SEM-140-02-03.0-H-D-A.pdf	11 02, 2019 by Pedram Babakhani
PDF File TEM-140-02-03.0-H-D-A.pdf	11 02, 2019 by Pedram Babakhani

Download All

Technical Specifications

Absolute Maximum Ratings

Symbols	Min	Max	Unit	Description
VIN supply voltage	-0.3	65	V	TPS54260-Q1 datasheets.
VMIO	-0.5	3.6	V	PS MIO I/O supply voltage
VCCO	-0.5	3.6	V	PL supply voltage for HR I/O banks
Storage Temperature	-40	+85	°C	

Absolute maximum ratings

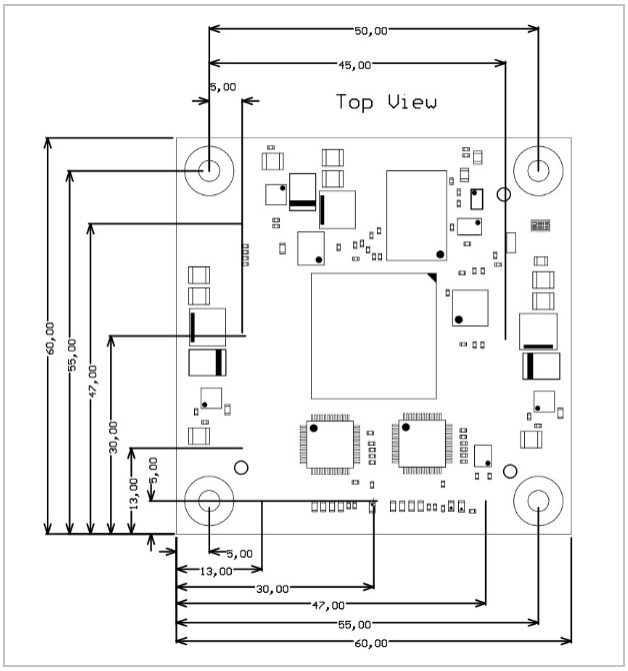
Recommended Operating Conditionse

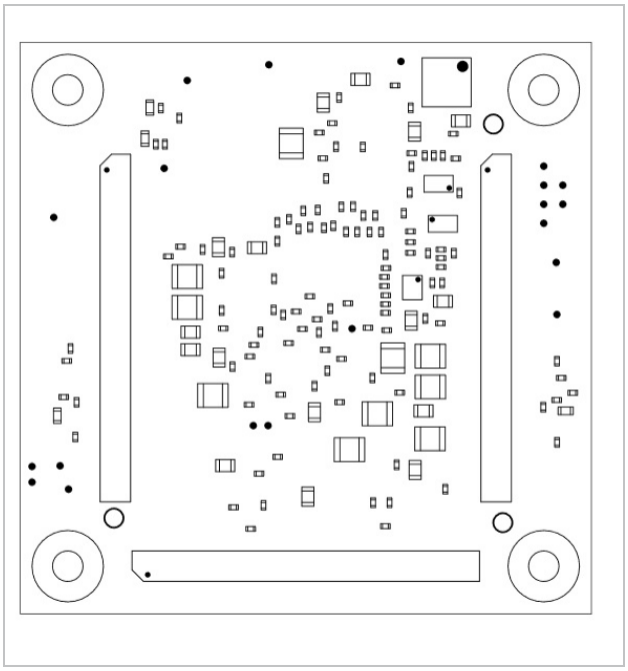
Symbol	Min	Max	Units	Reference Document
VIN supply voltage	3.5	60	V	TPS54260-Q1 datasheets.
VMIO	1.71	3.465	V	See Xilinx DS187 data sheet.
VCCO	1.14	3.465	V	See Xilinx DS187 datasheet.
Operating Temperature	-40	+105	°C	

Recommended operating conditions

Physical Dimensions

- Module size: 60 mm × 60 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 7 mm.
- PCB thickness: 1.6 mm.





Physical Dimension

Currently Offered Variants

Trenz shop TE0728 overview page	
English page	German page

Trenz Electronic Shop Overview

Revision History

Hardware Revision History

Product changes can be seen in PCN page.

Date	Revision	Changes
2016-08-18	04	• U1 DDR3 IC changed from NT5CB256M16CP-DIH to NT5CC256M16CP-DIH • Net DDR3-ODT0: added series resistor R55 • Added Traceability pad • Net PS-POR-B: added pull-down resistor R56
2015-12-01	03	• ...

2015-06-12	02	• ...
2015-03-03	01	• ...

Hardware Revision History

Hardware revision number is printed on the PCB board next to the module model number separated by the dash.

Document Change History

Date	Revision	Contributor	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• smale style update
2019-05-16	v. 367	Pedram Babakhani	• initial release

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Document change history.

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Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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