TE0745 TRM

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Overview

The Trenz Electronic TE0745 is an industrial/commercial/extended grade module integrating a Xilinx Zynq SoC (XC7Z-030, XC7Z-035 or XC7Z-045), 1 GByte DDR3/L SDRAM, 32/64 MByte SPI Flash memory for configuration and operation and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/O's is provided via rugged high-speed stacking strips.

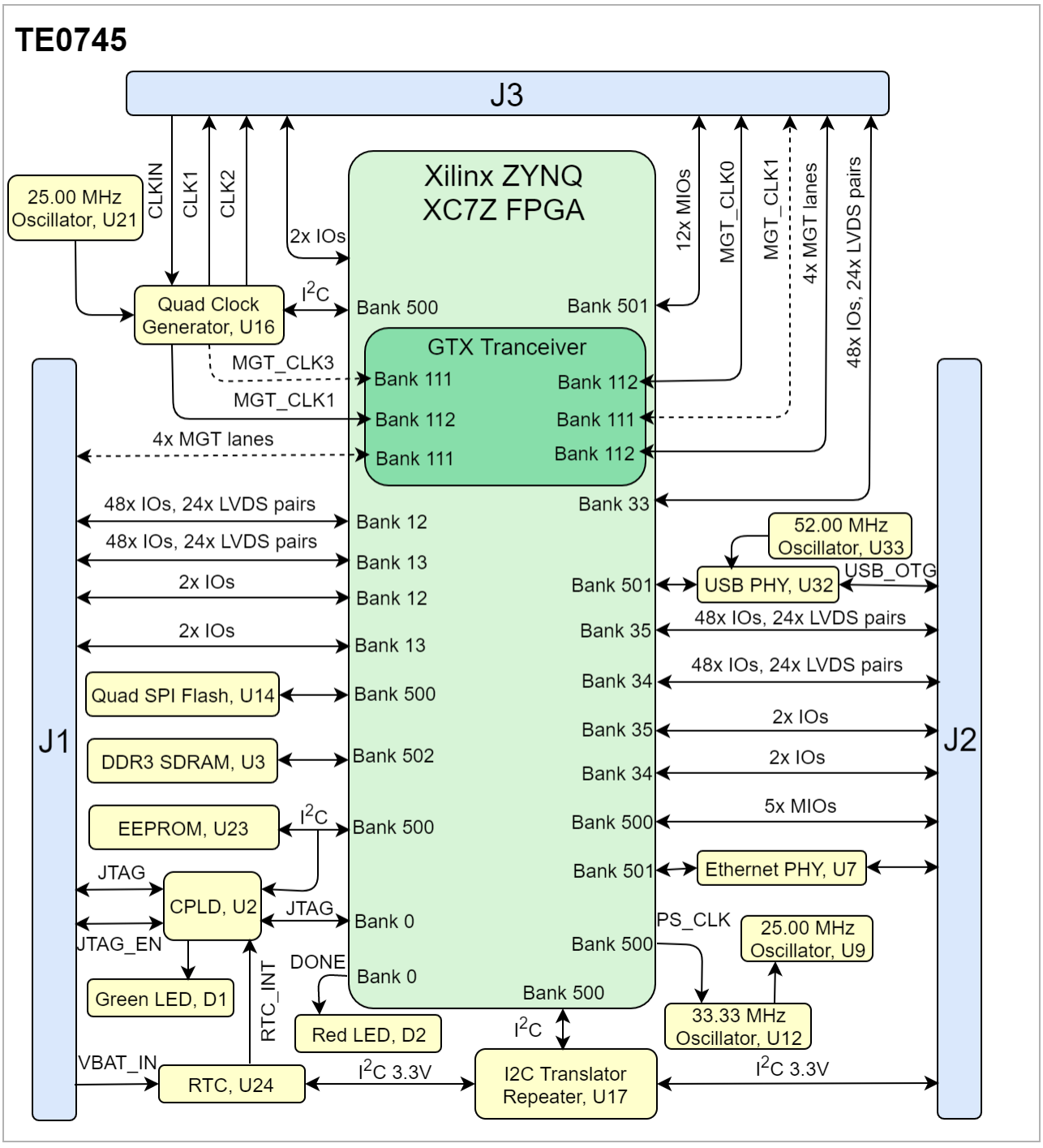
Refer to http://trenz.org/te0745-info for the current online version of this manual and other available documentation.

Key Features

- Industrial grade Xilinx Zynq SoC (XC7Z030, XC7Z035, XC7Z045)
- Dual core ARM Cortex-A9 MPCore™ with CoreSight™
- 32 (2x16) bit wide DDR3L SDRAM
- 32/64 MByte QSPI Flash memory
- 4 or 8 GTX transceiver lanes (XC7Z030 variant has 4)
- 1 Gigabit Ethernet transceiver PHY
- Two User LEDs
- EEPROM storing Ethernet MAC Address
- High-speed USB 2.0 ULPI transceiver with full OTG support
- Programmable quad clock generator
- Temperature compensated RTC (real-time clock)
- Board to Board (B2B)
  - Plug-on module with 3 × 160-pin high-speed connectors
- Power supply
  - 3.3V
- Others
- On-board high efficiency DC-DC converters
- System management
  - eFUSE bit-stream encryption
  - AES bit-stream encryption
  - Evenly spread supply pins for good signal integrity
- Rugged for shock and high vibration

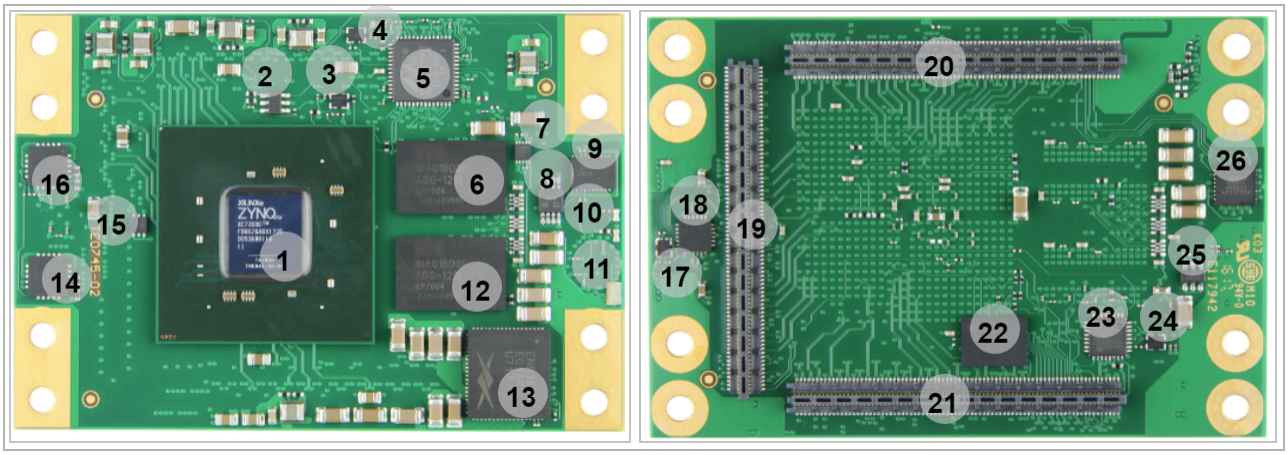
Additional assembly options are available for cost or performance optimization upon request.

Block Diagram



TE0745 block diagram

Main Components



TE0745 main components

1. Xilinx Zynq XC7Z family SoC, U1
2. Quad SPI Flash memory, U14
3. Reference clock signal oscillator, U12
4. Reference clock signal oscillator, U9
5. 1 Gigabit Ethernet PHY, U7
6. DDR3L SDRAM (8 Banks a 32 MWords, 16-bit word width), U3
7. DDR3 memory termination regulator with buffered reference voltage VTTREF, U18
8. Real-Time-Clock, U24
9. level-shifting I^2C bus repeater, U17
10. Red LED, D2
11. Green LED, D1
12. DDR3L SDRAM (8 Banks a 32 MWords, 16-bit word width), U5
13. 12A DC-DC PowerSoC (VCCINT), U4
14. DC-DC regulator (MGTAVTT), U8
15. DC-DC regulator (MGTAUX), U6
16. DC-DC regulator (MGTAVCC), U11
17. I^2C Programmable Quad Clock Generator, U13
18. Reference clock signal oscillator, U21
19. B2B Connector, J3
20. B2B Connector, J1
21. B2B Connector, J2
22. Quad SPI Flash memory, U14
23. USB transceiver PHY , U32
24. Reference clock signal oscillator, U33
25. EEPROM for MAC address, U23
26. System Controller CPLD, U2

Initial Delivery State

Storage device name	Content	Notes
EEPROM	User content, not programmed	Valid MAC Address from manufacturer.
SPI Flash OTP Area	not programmed	Except serial number programmed by flash vendor.
SPI Flash Quad Enable bit	Programmed	-
SPI Flash main array	Not programmed	-

eFUSE USER	Not programmed	-
eFUSE Security	Not programmed	-
Si5338 OTP NVM	Not programmed	OTP not re-programmable after delivery from factory

Initial delivery state of programmable devices on the module

Configuration Signals

BOOTMODE is connected to MIO4 and B2B Connector J2 (Pin 133) and BOOTMODE_1 is connected to MIO5 and System Controller CPLD and default high.

Boot Mode	BOOTMODE_1 (MIO5)	BOOTMODE (MIO4)	Note
JTAG Boot mode	0	0	JTAG only is only possible with other CPLD Firmware
----	0	1	not supported
QSPI	1	0	
SD Card	1	1	

Boot process.

Signal	B2B	Direction	Note
RST_IN_N	J2-131	Input	Low-active Power-On reset pin, controls POR_B-signal (Bank 500 - C23)
PS_SRST	J2-152	Input	Low-active PS system-reset pin of Zynq chip.
JTAG_EN	J1-148	Input	Low FPGA access, high CPLD access

Control Pins

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

FPGA bank number and number of I/O signals connected to the B2B connector:

FPGA Bank	Type	B2B Connector	I/O Signal Count	Voltage Level	Notes
12	HR	J1	48 Diff (24 LVS pair), 2 Single ended	VCCIO_12 pins J1-54, J1-55	Voltage range 1.2V to 3.3V
13	HR	J1	48 Diff (24 LVS pair), 2 Single ended	VCCIO_13 pins J1-112, J1-113	Voltage range 1.2V to 3.3V
33	HP	J3	48 Diff (24 LVS pair), 2 Single ended	VCCIO_33 pins J3-115, J3-120	Voltage range 1.2V to 1.8V

34	HP	J2	48 Diff (24 LVS pair), 2 Single ended	VCCIO_34 pins J2-29, J2-30	Voltage range 1.2V to 1.8V
35	HP	J2	48 Diff (24 LVS pair), 2 Single ended	VCCIO_35 pins J2-87, J2-88	Voltage range 1.2V to 1.8V
500	MIO	J2	5	1.8V	MIO0, MIO12 ... MIO15, user configurable I /O's on B2B
501	MIO	J3	12	1.8V	MIO40 ... MIO51 , user configurable I /O's on B2B

General PL I/O to B2B connectors information

System Controller I/O Pins

Pin Name	Direction	Function	B2B	Default Configuration
JTAG_EN	Input	JTAG select	J1-148	During normal operating mode the JTAG_EN pin should be in the low state for JTAG signals to be forwarded to the Zynq SoC. If JTAG_EN pin is set to high or left open the JTAG signals are forwarded to the System Controller CPLD.
RST_IN_N	Input	Reset	J2-131	Low-active Power-On reset pin, controls POR_B-signal (bank 500, pin C23) of Zynq chip.
PS_SRST	Input	Reset	J2-152	Low-active PS system-reset pin of Zynq chip.
BOOTMODE	Input	Boot mode	J2-133	Control line which sets in conjunction with signal 'BOOTMODE_1' connected to CPLD (BOOTMODE_1 default high) the boot source of the Zynq chip. See section "Configuration Signals".
PWR_PL_OK	Input	Power good	J2-135	Indicates stable state of PL supply voltage (low-active) after power-up sequence.

PWR_PS_OK	Input	Power good	J2-139	Indicates stable state of PS supply voltage (low-active) after power-up sequence.
MIO0	Input	PS MIO	J2-137	User I/O also connected to CPLD.

System Controller CPLD pins connection over B2B

JTAG Interface

JTAG interface access is provided through the SoC's PS configuration bank 0, it is connected to B2B connector J1.

JTAG Signal	B2B Connector
TMS	J1- 144
TDI	J1- 142
TDO	J1- 145
TCK	J1- 143
JTAG_EN	J1- 148

JTAG pins connection

I2C Interface

The I^2C interface on B2B connector J2 has PS_3.3V as reference voltage and is connected to the Zynq SoC via voltage level translating (3.3V 1.8V) I^2C bus repeater (U17).

Schematic	B2B	Notes
I2C_33_SCL	J2-119	3.3V reference voltage
I2C_33_SDA	J2-121	3.3V reference voltage

Pin assignment of the B2B I2C interface.

Following on-module I^2C interface are connected to the same I2C bus:

I2C Device	I2C Address	Notes
Quad programmable PLL clock generator U16: pins 12 (SCL), 19 (SDA)	0x70	-
MAC Address EEPROM U23, pins 1 (SCL), 3 (SDA)	0x53	-
SC CPLD U2, bank 2, pins 16 (SDA), 17 (SCL)	User programmable.	-
RTC, U24	0x6F	-
RTC RAM, U24	0x57	-

MIO-pin assignment of the on-module I2C interface.

I2C bus is accessible from SoC over following MIO:

MIO Pin	Signal Schematic Name	Notes
MIO 10	I2C_SCL	1.8V reference voltage
MIO 11	I2C_SDA	1.8V reference voltage

Module's I2C-Slave address overview.

MGT Lanes

Lane	Bank	Type	Signal Name	B2B Pin	Note
0	112	GTX	MGT_RX0_P	J3-50	
			MGT_RX0_N	J3-52	
			MGT_TX0_P	J3-51	
			MGT_TX0_N	J3-53	
1	112	GTX	MGT_RX1_P	J3-56	
			MGT_RX1_N	J3-58	
			MGT_TX1_P	J3-57	
			MGT_TX1_N	J3-59	
2	112	GTX	MGT_RX2_P	J3-62	
			MGT_RX2_N	J3-64	
			MGT_TX2_P	J3-63	
			MGT_TX2_N	J3-65	
3	112	GTX	MGT_RX3_P	J3-68	
			MGT_RX3_N	J3-70	
			MGT_TX3_P	J3-69	
			MGT_TX3_N	J3-71	
4	111 [1)]	GTX	MGT_RX4_P	J1-23	
			MGT_RX4_N	J1-21	
			MGT_TX4_P	J1-22	
			MGT_TX4_N	J1-20	
5	111 [1)]	GTX	MGT_RX5_P	J1-17	
			MGT_RX5_N	J1-15	
			MGT_TX5_P	J1-16	
			MGT_TX5_N	J1-14	
6	111 [1)]	GTX	MGT_RX6_P	J1-11	
			MGT_RX6_N	J1-9	
			MGT_TX6_P	J1-10	
			MGT_TX6_N	J1-8	

7	111 [1]	GTX	MGT_RX7_P MGT_RX7_N MGT_TX7_P MGT_TX7_N	J1-5 J1-3 J1-4 J1-2	

MGT connections to B2B connector

[1] **Note:** MGT bank 111 not available at XC7Z030 Zynq SoC.

MIO Pins

MIO Pin	Connected to	B2B	Notes
MIO0	CPLD and B2B J2-137	J2	Configurable, def. used for SD CD
MIO1...6	SPI_CS , SPI_DQ0... SPI_DQ3, SPI_SCK	-	QSPI Flash
MIO7	USB_RESET_N	-	10k pullup to PS_1.8V
MIO8	Used for CPLD Status	-	10k pullup to PS_1.8V
MIO9	ETH_PHY_RST_N	-	ETH PHY
MIO10....11	SCL/SDA	-	I2C
MIO12...13	-	J2	Configurable, def GPIO
MIO14...15	UART		Configurable, def. used for UART
MIO16...27	ETH_TXCK, ETH_TXD0..3, ETH_TXCTL ETH_RXCK, ETH_RXD0..3, ETH_RXCTL	-	Ethernet Signals
MIO28...39	OTG_DATA4, OTG_DIR, OTG_STP, OTG_NXT, OTG_DATA0...3, OTG_CLK, OTG_DATA5...7	-	USB
MIO40...45	MIO40..45	J3	Configurable, def. used for SD
MIO46...50	-	J3	GPIO
MIO51	I2C Reset	J3	Configurable, def. used for I2C Reset
MIO52	PHY_MDC	J3	ETH PHY
MIO53	PHY_MDIO	J3	ETH PHY

MIOs pins

On-board Peripherals

Chip/Interface	Designator	Notes
Quad SPI Flash Memory	U14	

DDR3 SDRAM	U3, U5	
RTC	U24	
EEPROM	U23	
System Controller CPLD	U2	
Ethernet PHY	U7	
USB ULPI PHY	U32	
Programmable PLL Clock	U16	
LEDs	D1, D2	
Oscillators	U21, U12, U33, U9	

On board peripherals

Quad SPI Flash Memory

On-board QSPI flash memory (U14) on the TE0745-02 is provided by Micron Serial NOR Flash Memory 256/512 Mbit (32/64 MByte) storage capacity. This non volatile memory is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used. Quad SPI Flash (U14) is connected to the Zynq PS QSPI0 interface via PS MIO bank 500, pins MIO1 ... MIO6.

MIO Pin	Schematic	Notes
MIO1	SPI-CS	
MIO2	SPI-DQ0/M0	
MIO3	SPI-DQ1/M1	
MIO4	SPI-DQ2/M2	
MIO5	SPI-DQ3/M3	
MIO6	SPI-SCK/M4	

Quad SPI interface MIOs and pins

DDR3 SDRAM

The TE0745 SoM has two volatile Intelligent Memory 512 MByte DDR3L-1600 SDRAM IC for storing user application code and data.

- Part number: IM4G16D3FABG-125I
- Supply voltage: 1.5V
- Organization: 256M x 16 bits

DDR3 SDRAM can be varied on demand for other assembly options. DDR3 can have density of maximum 512MB due to available addressing. The maximum possible speed for DDR3 SDRAM is 1600 Mb/s.

RTC

An temperature compensated is used as Real Time Clock (U24). Battery voltage must be supplied to the clock from the base board via pin 'VBAT_IN' (J1-146). Battery backed registers can be accessed over I^2C bus at slave address mentioned in the table below. General purpose RAM of the RTC can be accessed at I^2C slave address 0x57. RTC IC is supported by Linux so it can be used as hwclock device.

The interrupt line 'RTC_INT' of the RTC is connected to System Controller CPLD bank 3 pin 4.

Schematic	B2B	I2C Address	Designator	Notes
I2C_33_SCL	J2-119	0x6F	U24	
I2C_33_SDA	J2-121			

I2C Address for RTC

Programmable PLL Clock

There is a Silicon Labs I^2C programmable quad PLL clock generator (U16) on-board. It's output frequencies can be programmed by using the I^2C-bus with address 0x70.

A 25.00 MHz (U21) oscillator is connected to pin 3 (IN3) and is used to generate the output clocks.

Once running, the frequency and other parameters can be changed by programming the device using the I^2C-bus connected between the Zynq module (master) and reference clock signal generator (slave).

U16 Pin	Signal Name / Description	Connected To	Direction	Default	Note
IN1	CLKIN_P	B2B, J3-76	Input		Reference input clock from base board.
IN2	CLKIN_N	B2B, J3-74	Input		
IN3	Reference input clock.	Oscillator U21, pin 3	Input		25.000000 MHz oscillator, Si8008BI.
IN4	-	GND	Input		I^2C slave device address LSB (0x70 default address).
IN5	-	Not connected.	Input		Not used.
IN6	-	GND	Input		Not used.
CLK0A	MGT_CLK1_P	Zynq Soc U1, pin U6	Output	Not programmed	MGT bank 112 reference clock.
CLK0B	MGT_CLK1_N	Zynq Soc U1, pin U5	Output	Not programmed	
CLK1A	CLK1_P	B2B, J3-80	Output	Not programmed	Reference clock output to base board.
CLK1B	CLK1_N	B2B, J3-82	Output	Not programmed	
CLK2A	CLK2_P	B2B, J3-86	Output	Not programmed	Reference clock output to base board.
CLK2B	CLK2_P	B2B, J3-88	Output	Not programmed	
CLK3A	MGT_CLK3_P	Zynq Soc U1, pin AA6	Output	Not programmed	MGT bank 111 reference clock.
CLK3B	MGT_CLK3_N	Zynq Soc U1, pin AA6	Output	Not programmed	

Programmable quad PLL clock generator inputs and outputs.

System Controller CPLD

The System Controller CPLD (U2) is central system management unit where essential control signals are logically linked by the implemented logic in CPLD firmware, which generates output signals to control the system, the on-board peripherals and the interfaces. Interfaces like JTAG and I^2C between the on-board peripherals and to the FPGA-module are by-passed, forwarded and controlled by the System Controller CPLD.

Other tasks of the System Controller CPLD are the monitoring of the power-on sequence and to display the programming state of the FPGA module.

For current CPLD Firmware description, check **TE0745 CPLD**

USB ULPI PHY

Hi-speed USB ULPI PHY (U32) is provided on the board. The ULPI interface is connected to the Zynq PS USB0 via MIO28..39, bank 501 (see also section). The I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 52.00 MHz oscillator (U33).

MAC Address EEPROM

A serial EEPROM (U23) contains a globally unique 48-bit node address, which is compatible with EUI-48 (TM) specification. The device is organized as two blocks of 128 x 8-bit memory. One of the blocks stores the 48-bit node address and is write protected, the other block is available for application use.

EEPROM

Schematic	MIO	I2C Address	Designator	Notes
I2C_SCL	MIO10	0x53	U23	
I2C_SDA	MIO11			

I2C address for EEPROM

Ethernet PHY

On-board Gigabit Ethernet PHY (U7) is provided on the board. The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from an on-board 25.00 MHz oscillator (U9), the 125MHz output clock signal CLK_125MHZ is connected to the pin J2-150 of B2B connector J2.

Schematic	B2B	Notes
PHY_MDIO	-	Connected to MIO52
PHY_MDIO0+/ MDIO0-	J2-120/122	
PHY_MDIO1+/ MDIO1-	J2-126/128	
PHY_MDIO2+/ MDIO2-	J2-132/134	
PHY_MDIO3+/ MDIO3-	J2-138/140	
PHY_LED1	J2-144	
PHY_LED2	J2-146	
PHY_LED3	J2-148	

PHY_CLK125M	J2-150	
PHY_MDC	-	Connected to MIO53

Ethernet PHY B2B connectors.

LEDs

Schematic	Color	Connected to	Active level	Note	Note
D1	Green	System Controller CPLD (bank 3, pin 5)	High	System main status LED, blinking indicates system activity	
D2	Red	Zynq chip, bank 0 (config bank), 'DONE' pin	Low	Reflects inverted DONE signal. ON when FPGA is not configured, OFF as soon as PL is configured. This LED remains OFF if System Controller CPLD can not power up the PL supply voltage.	

On-board LEDs

Clock Sources

Designator	Schematic Name	Frequency	Note
U21	-	25.00 MHz	Quad PLL clock generator U16, pin 3
U12	PS_CLK	33.33 MHz	Bank 500 (MIO0 bank), pin B24
U33	OTG-RCLK	52.00 MHz	USB 2.0 transceiver PHY U32, pin 26
U9	ETH_CLKIN	25.00 MHz	Gigabit Ethernet PHY U7, pin 34

Osillators

Power and Power-On Sequence

Power Supply

Power supply with minimum current capability of 3.0 A for system startup is recommended.

Power Consumption

The maximum power consumption of a module mainly depends on the design which is running on the FPGA.

Power Input Pin	Typical Current
PL_VIN	TBD*
PS_VIN	TBD*
PS_3.3V	TBD*

Power Consumption

* TBD - To Be Determined

For the lowest power consumption and highest efficiency of on board DC-DC regulators it is recommended to powering the module from one single 3.3V supply. All input power supplies have a nominal value of 3.3V. Although the input power supplies can be powered up in any order, it is recommended to power them up simultaneously.

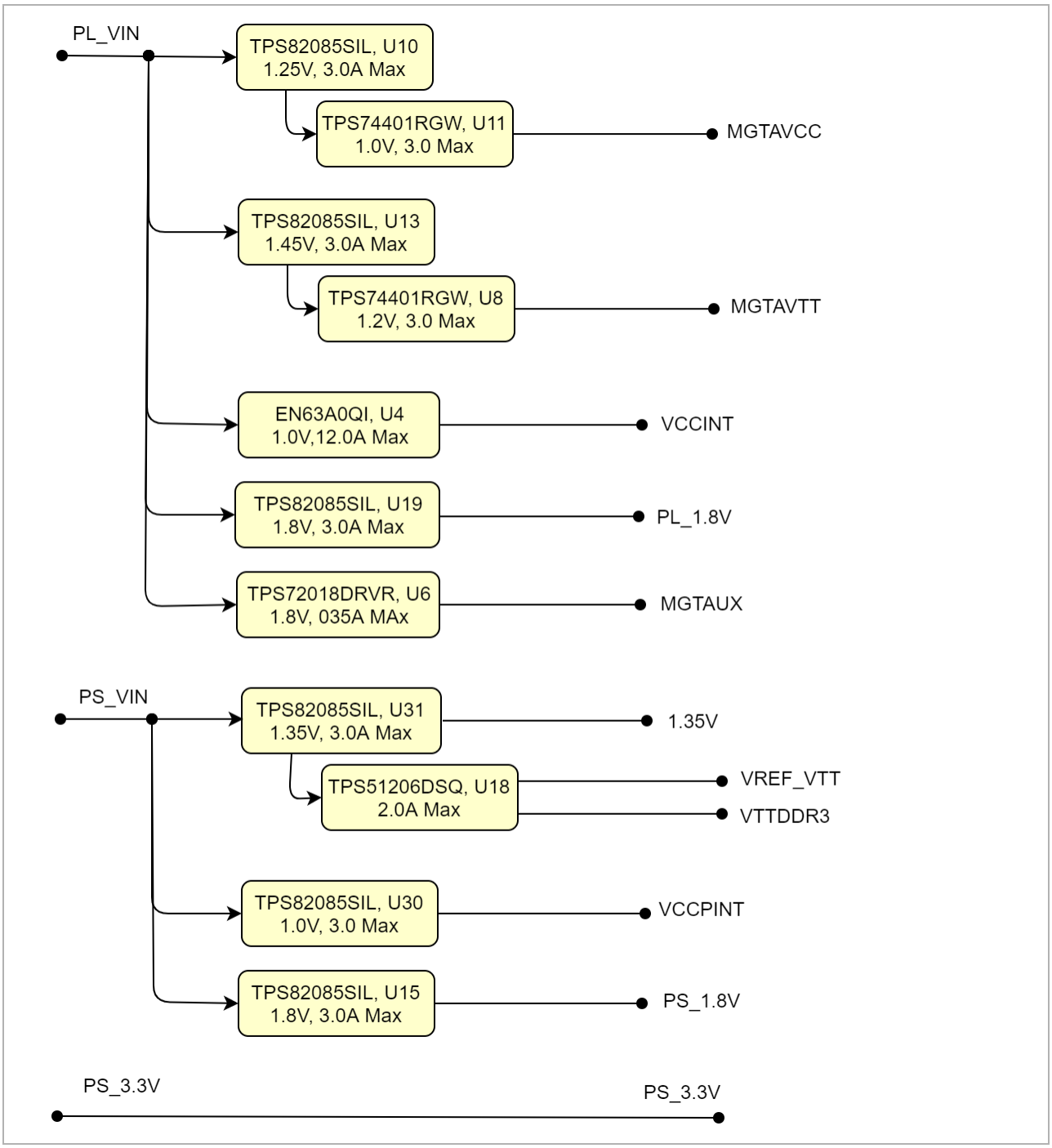
The on-board voltages of the TE0745 SoC module will be powered-up in order of a determined sequence after the external voltages 'PL_VIN', 'PS_VIN' and 'PS_3.3V' are available. All those power-rails can be powered up, with 3.3V power sources, also shared.

To avoid any damage to the module, check for stabilized on-board voltages should be carried out(i.e. power good and enable signals) before powering up any SoC's I/O bank voltages VCCO_x. All I/Os should be tri-stated during power-on sequence.

Core voltages and main supply voltages have to reach stable state and their "Power Good"-signals have to be asserted before other voltages like PL bank's I/O voltages can be powered up.

It is important that all baseboard I/Os are tri-stated at power-on until the "Power Good"-signals 'PWR_PS_OK' (J2-139) and 'PWR_PL_OK' (J2-135) are high, meaning that all on-module voltages have become stable and module is properly powered up.

Power Distribution Dependencies



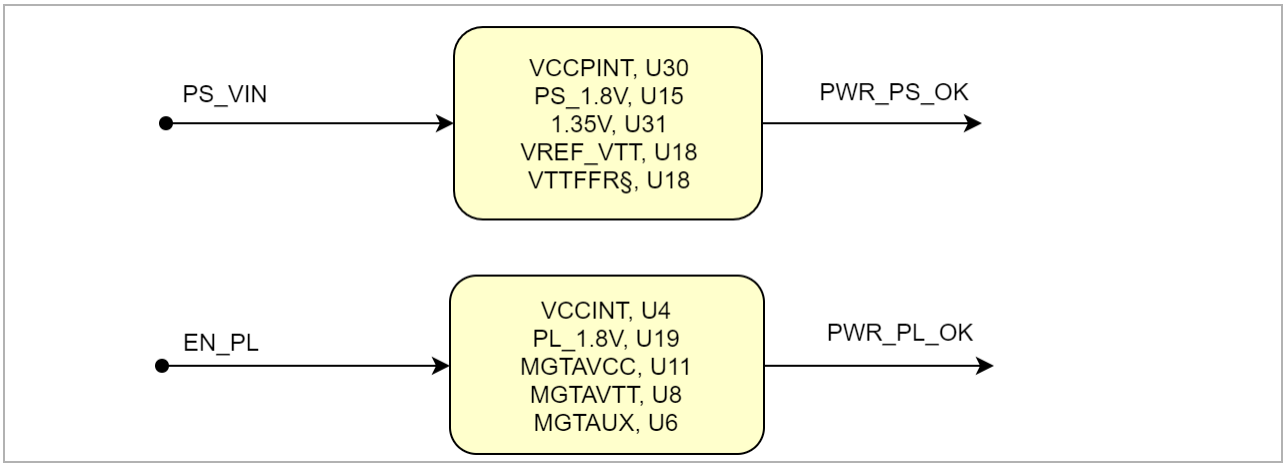
Power Distribution

⚠ Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

Power-On Sequence

The TE0745 SoM meets the recommended criteria to power up the Xilinx Zynq MPSoC properly by keeping a specific sequence of enabling the on-board DCDC converters dedicated to the particular functional units of the Zynq chip and powering up the on-board voltages.

Following diagram clarifies the sequence of enabling the particular on-board voltages, which will power-up in descending order as listed in the blocks of the diagram:

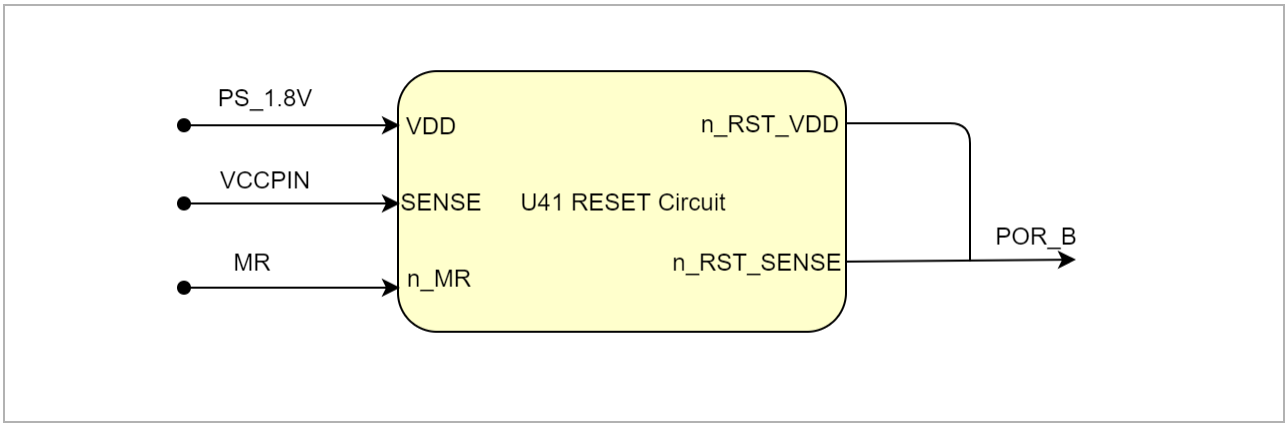


Power Sequency

The Enable-Signal 'EN_PL' is permanently logic high in standard SC-CPLD firmware. The "Power Good"-signals 'PWR_PS_OK' and 'PWR_PL_OK' (latter low-active, extern pull-up needed) are available B2B-connector J2 (pins J2-139, J2-135) and on the SC-CPLD.

Voltage Monitor Circuit

The voltages 'VCCPINT' and 'PS_1.8V' are monitored by the voltage monitor circuit U41, which generates the POR_B reset signal at Power-On. A manual reset is also possible by driving the MR-pin (available on J2-131 or SC-CPLD) to GND. Leave this pin unconnected or connect to VDD (PS_1.8V) when unused.



Voltage Monitor Circuit

Power Rails

Power Rail Name	B2B Connector JM1 Pin	B2B Connector JM2 Pin	B2B Connector JM3 Pin	Direction	Notes
PL_VIN	147, 149, 151, 153, 155, 157, 159	-	-	Input	module supply voltage
PS_VIN	-	154, 156, 158	-	Input	module supply voltage
PS_3.3V	-	160	-	Input	module supply voltage
VCCIO12	54, 55	-	-	Input	high range bank I/O voltage
VCCIO13	112, 113	-	-	Input	high range bank I/O voltage
VCCIO33	-	-	115, 120	Input	high performance bank I/O voltage
VCCIO34	-	29, 30	-	Input	high performance bank I/O voltage
VCCIO35	-	87, 88	-	Input	high performance bank I/O voltage
VBAT_IN	146	-	-	Input	RTC (battery-backed) supply voltage
PS_1.8V	-	130	-	Output	internal 1.8V voltage level (Process System)
PL_1.8V	-	-	84,85	Output	internal 1.8V voltage level (FPGA)

Module power rails.

Bank Voltages

Bank	Schematic Name	Voltage	Notes
0 (config)	VCCIO_0	PL_1.8V, if R67 is equipped PS_1.8V, if R68 is equipped	-
500 (MIO0)	PS_1.8V	1.8V	-
501 (MIO1)	PS_1.8V	1.8V	-
502 (DDR3)	1.35V	1.35V	-
12 HR	VCCIO_12	User	HR: 1.2V to 3.3V
13 HR	VCCIO_13	User	HR: 1.2V to 3.3V
33 HP	VCCIO_33	User	HP: 1.2V to 1.8V

Zynq SoC bank voltages.

Board to Board Connectors

5.2 x 7.6 cm SoM Kintex modules use three Samtec Razor Beam LP Terminal Strip (ST5) on the bottom side.

- 3x REF-192552-02 (160-pins)
  - ST5 Mates with SS5

5.2 x 7.6 cm SoM Kintex carrier use three Samtec Razor Beam LP Socket Strip (SS5) on the top side.

- 3x REF192552-01 (160-pins)
  - SS5 Mates with ST5

Technical Specifications

Absolute Maximum Ratings

Symbols	Description	Min	Max	Unit
PL_VIN	-0.3	5	V	TI TPS720 data sheet
PS_VIN	-0.3	7	V	TI TPS82085 data sheet
PS_3.3V	3.135	3.465	V	3.3V nominal ± 5%
VBAT supply voltage	-1	6.0	V	ISL12020MIRZ data sheet
PL IO bank supply voltage for HR I/O banks (VCCO)	-0.5	3.6	V	-
PL IO bank supply voltage for HP I/O banks (VCCO)	-0.5	2.0	V	-
I/O input voltage for HR I/O banks	-0.4	VCCO_X+0.55	V	-
I/O input voltage for HP I/O banks	-0.55	VCCO_X+0.55	V	-
GT receiver (RXP/RXN) and transmitter (TXP /TXN)	-0.5	1.26	V	-
Voltage on module JTAG pins	-0.3	3.6	V	MachX02 Family data sheet
Storage temperature	-40	+128	°C	Limits of ISL12020MIRZ RTC chip.
Storage temperature without the ISL12020MIRZ	-55	+100	°C	Limits of DDR3 memory chip.

PS absolute maximum ratings

Attention: PS_3.3V is directly connected to numerous on-board peripherals as supply and I/O voltage.

Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

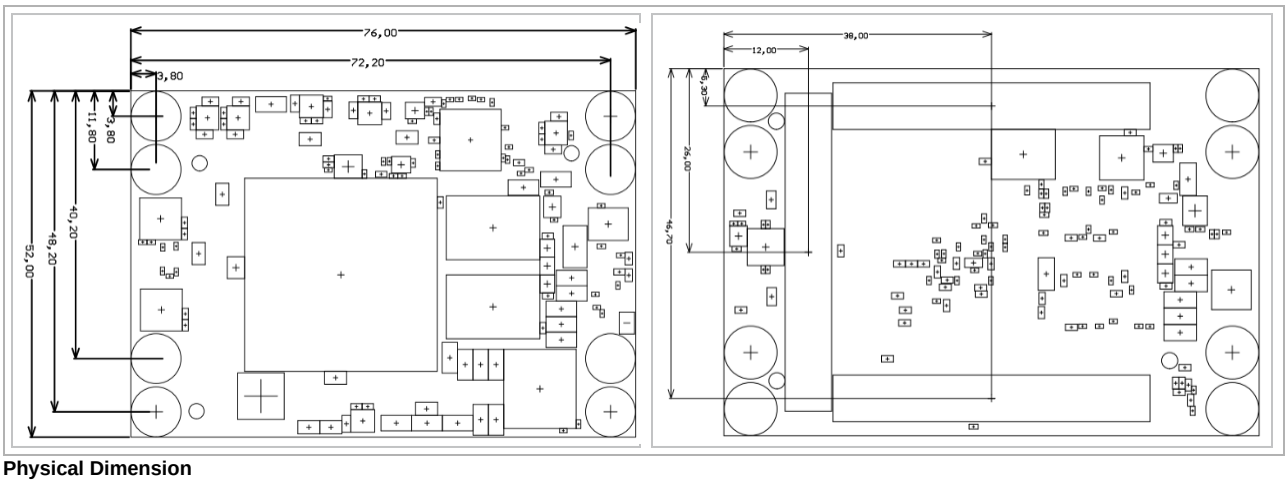
Parameter	Min	Max	Units	Reference Document	
PL_VIN	3.2	4.5	V	-	TI TPS720 data sheet
PS_VIN	3.135	3.6	V	-	CPLD data sheets
PS_3.3V	3.135	3.465	V	-	3.3V nominal ± 5%
VBAT_IN supply voltage	2.7	5.5	V	-	ISL12020MIRZ data sheet
PL I/O bank supply voltage for HR I/O banks (VCCO)	1.14	3.465	V	-	Xilinx datasheet DS191
PL I/O bank supply voltage for HP I/O banks (VCCO)	1.14	1.89	V	-	Xilinx datasheet DS191
I/O input voltage for HR I/O banks	-0.20	VCCO_X+0.20	V	-	Xilinx datasheet DS191
I/O input voltage for HP I/O banks	-0.20	VCCO_X+0.20	V	-	Xilinx datasheet DS191
GT receiver (RXP/RXN) and transmitter (TXP /TXN)	(*)	(*)	V	(*) Check datasheet	Xilinx datasheet DS191
Voltage on Module JTAG pins	3.135	3.6	V	JTAG signals forwarded to Zynq module config bank 0	MachX02 Family Data Sheet
Recommended Operating Temperatur	-40	+85	°C		

Recommended operating conditions.

The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

Physical Dimensions

- Module size: 52 mm × 76 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 4mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 3mm. Please download the step model for exact numbers



Physical Dimension

Currently Offered Variants

Trenz shop TE0745 overview page	
English page	German page

Trenz Electronic Shop Overview

Revision History

Hardware Revision History

Product changes can be seen in TE0745 Product Change Notifications page.

Date	Revision	Changes	Documentation Link
2016-11-02	02	• MAC EEPROM Address patch fixed on PCB	REV02
2016-05-12	01	• Prototypes	REV01

Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.



Board hardware revision number.

Document Change History

Date	Revision	Contributor	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy24.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy24.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy24.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to	• Corrected limits for operating conditions of PL/PS_VIN • Corrected MIO section (UARt)

invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.

invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.

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Content EntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	Content EntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	Content EntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	
18 Oct 2021	v.102	Martin Rohrmüller	• Corrected key features power supply voltage
05 Feb 2021	v.98	John Hartfiel	• typographical correction • block diagram correction
2020-02-18	v.94	John Hartfiel	• correction power rails
2019-11-19	v.93	John Hartfiel	• correction key features
2019-10-10	v.92	Pedram Babakhani	• document style update • description bug fix
2019-03-01	v.83	Pedram Babakhani	• Add power note

2018-04-11	v.81	John Hartfiel	• correction PDF link
2017-11-14	v.80	John Hartfiel	• Update B2B Section
2017-11-13	v.79	Ali Naseri, Jan Kumann, John Hartfiel	• First TRM release
--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy24 4.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String,	• --

class com. atlassian . confluen ce. pages. Page] due to overlapp ing prototyp es between : [interfac e com. atlassian . confluen ce.user. Conflue nceUser , class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian

		.user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	

Document change history.

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Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

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Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]