

TEBF0808 Slave CPLD

Table of contents

- 1 [Table of contents](#)
- 2 [Overview](#)
- 3 [Product Specification](#)
 - 3.1 [Port Description](#)
 - 3.2 [Functional Description](#)
 - 3.2.1 [JTAG](#)
 - 3.2.2 [Power](#)
 - 3.2.3 [Enable](#)
 - 3.2.4 [Reset](#)
 - 3.2.5 [Boot Mode](#)
 - 3.2.6 [UART](#)
 - 3.2.7 [Module SI5345](#)
 - 3.2.8 [SD Card](#)
 - 3.2.9 [RGPIO](#)
 - 3.2.10 [LED](#)
- 4 [Appx. A: Change History](#)
 - 4.1 [Revision Changes](#)
 - 4.2 [Document Change History](#)
- 5 [Appx. B: Legal Notices](#)
 - 5.1 [Data Privacy](#)
 - 5.2 [Document Warranty](#)
 - 5.3 [Limitation of Liability](#)
 - 5.4 [Copyright Notice](#)
 - 5.5 [Technology Licenses](#)
 - 5.6 [Environmental Protection](#)
 - 5.7 [REACH, RoHS and WEEE](#)

Overview

Firmware for PCB-Slave CPLD with designator U39. Second CPLD Device in Chain: LCMX02-1200HC

Feature Summary

- Power Management
- Reset Management
- Boot Mode
- LEDs
- RGPIO
- SD Selection
- UART

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Description
1.8V_EN / EN_1V8	out	106	Power
5V_EN / EN_5V	out	115	Enable 5V, can be permanently enabled by S4-4
C_TCK		131	JTAG J28 (XMOD2) / <i>internal currently_not_used</i>
C_TDO		137	JTAG J28 (XMOD2) / <i>internal currently_not_used</i>
C_TDO1		136	JTAG J28 (XMOD2) / <i>internal currently_not_used</i>
C_TMS		130	JTAG J28 (XMOD2) / <i>internal currently_not_used</i>
CLK_A / AUD_CLK	out	1	AUDIO U3 CLK
CLK_CPLD / MEMS_CLKIN	in	128	U25 24,576MHz
DONE	in	67	PS Done
EN_DDR	out	86	Enable DDR Power
EN_FMC / FMC_EN	out	104	FMC
EN_FPD	out	81	Enable PS FPD Power
EN_GT_L	out	77	Enable GT Power
EN_GT_R	out	93	Enable GT Power
EN_LPD	out	84	Enable PS LPL Power
EN_PL	out	95	Enable PL Power
EN_PLL_PWR	out	78	Enable SI5345 Power
EN_PSGT / EN_PSGTR	out	75	Enable PS GT Power
ERR_OUT / ERROR	in	70	PS Error Out / Status / readable via RGIO
ERR_STATUS / ERROR_STAT	in	69	PS Error Status / Status / readable via RGIO
F1PWM	out	121	FAN1
F1SENSE	in	125	FAN1
FAN_FMC_EN / FMC_FAN_EN	out	132	FMC FAN
FMC_PG_C2M	out	141	FMC PG
HD_LED_N / HDLED_N	out	112	J10 HD LED
HD_LED_P / HDLED_P	out	110	J10 HD LED
HDIO_SC0 / SC0	in	32	FPGA IO / forward to HD_LED_P / HDLED_P
HDIO_SC1 / SC1	in	33	FPGA IO / <i>currently_not_used</i>
HDIO_SC2 / SC2	in	34	FPGA IO / <i>currently_not_used</i>
HDIO_SC3 / SC3	out	35	FPGA IO / <i>currently_not_used</i>
HDIO_SC4 / SC4	out	25	FPGA IO / <i>currently_not_used</i>
HDIO_SC5 / SC5	out	26	FPGA IO / RGPIO
HDIO_SC6 / SC6	in	27	FPGA IO / RGPIO CLK
HDIO_SC7 / SC7	in	28	FPGA IO / RGPIO
I2C_SCL / SCL	in	50	I2C / <i>currently_not_used</i>
I2C_SDA / SCA	in	52	I2C / <i>currently_not_used</i>
INIT_B / INIT	in	68	PS init B

JTAGENB		120	external Pin for CPLD Firmware Update
LP_GOOD / PG_LPD	in	83	LP Power Good
MIO24		38	MIO / currently_not_used
MIO25		39	MIO / currently_not_used
MIO30	in	48	MIO / force reboot after FSBL-PLL config for PCIe
MIO31	in	49	MIO / PCIe reset
MIO32		40	MIO / currently_not_used
MIO33		41	MIO / currently_not_used
MIO34		42	MIO / currently_not_used
MIO35		43	MIO / currently_not_used
MIO36		44	MIO / currently_not_used
MIO37		45	MIO / currently_not_used
MIO40	in	54	MIO / forwarded to PWRLED_P / LED_P
MIO41		55	MIO / currently_not_used
MIO42	out	60	FPGA UART RX
MIO43	in	61	FPGA UART TX
MIO44	out	47	MIO / SD_WP to FPGA
MOD_EN	out	119	Module Power 3.3V Enable
MODE0	out	6	Boot Mode
MODE1	out	9	Boot Mode
MODE2	out	10	Boot Mode
MODE3	out	11	Boot Mode
MR / MRESETn	out	92	PS Reset
PCI_SFP_EN	out	76	SFP
PER_EN	out	117	Baseboard Power 3.3V Enable
PERST / PERSTn	out	139	PCIE Resetn
PG_DDR	in	91	Power Good / Status / readable via RGIO
PG_FPD	in	85	Power Good / Status / readable via RGIO
PG_GT_L	in	96	Power Good / Status / readable via RGIO
PG_GT_R	in	94	Power Good / Status / readable via RGIO
PG_PL	in	82	Power Good / Status / readable via RGIO
PG_PLL_1V8 / PG_PLL	in	73	Power Good / Status / readable via RGIO
PG_PSGT	in	74	Power Good / Status / readable via RGIO
PLL_LOLN / PLL_LOL	in	58	Module U5 Si5345 / readable via RGIO / currently_not_used
PLL_RST / PLL_RSTn	out	56	Module U5 Si5345
PLL_SEL0	out	57	Module U5 Si5345
PLL_SEL1	out	59	Module U5 Si5345
POK_1V8	in	107	Power
POK_FMC	in	99	FMC Power/ readable via RGIO
PROG_B	inout	71	PS_PROG_B

PSON	out	105	ATX J20 PS_ON_N
PWR_BTN	in	113	Power Button S1 or J10
PWRLED_N / LED_N	out	111	J10 PWR
PWRLED_P / LED_P	out	109	J10 PWR
PWROK	in	100	ATX J20 PWROK / readable via RGIO
RST_BTN	in	114	Reset Button S2 or J10
S_1		127	Beeper/ currently_not_used
SC_IO0 / X0	out	12	Master-Slave SC-Communication / Power Reset
SC_IO1 / X1	out	13	Master-Slave SC-Communication / Power Reset
SC_IO2 / X2	out	14	Master-Slave SC-Communication / currently_not_used
SC_IO3 / X3	out	20	Master-Slave SC-Communication / currently_not_used
SC_IO4 / X4	in	21	Master-Slave SC-Communication /MMC SD WP
SC_IO5 / X5	in	22	Master-Slave SC-Communication / currently_not_used
SC_IO6 / X6	in	23	Master-Slave SC-Communication / Sanity check from other CPLD (FMC VADJ Enable)
SC_IO7 / X7	in	24	Master-Slave SC-Communication / Sanity check from other CPLD (FMC VADJ Enable)
SC_IO8 / dummy		126	/ currently_not_used / ! not available on PCB REV2 !
SC2_SW1	in	133	S5-1 / Boot Mode Selection / readable via RGIO
SC2_SW2	in	138	S5-2 / Boot Mode Selection / readable via RGIO
SD_A_EN	out	140	Micro SD
SD_B_EN	out	122	MMC SD
SD_CD / SD_CD_OUT	out	65	SD Card detect to FPGA
SD_CD_B	in	143	MMC SD / readable via RGIO
SD_CD_S	in	142	Micro SD / readable via RGIO
SEL_SD / SD_SEL	out	62	Select SD
SRST_B / SRSTn	out	19	PS_SRST_B
STAT_LED2 / LED2	out	98	LED D6 Green
STAT_LED3 / LED3	out	97	LED D7 Red
XMOD2_A / XMOD_TXD	out	5	J12 (XMOD 1)
XMOD2_B / XMOD_RXD	in	4	J12 (XMOD 1)
XMOD2_E / XMOD_LED	out	3	J12 (XMOD 1)
XMOD2_G / XMOD_BTN	in	2	J12 (XMOD 1) / readable via RGIO

Functional Description

JTAG

JTAGENB set carrier board CPLD into the chain for firmware update. For Update set DIP S4-3 to ON.

Power

PSON signal will be enabled/disabled after delay, when Power Button is pressed. Power Button is debounced.

Stage	Power Enable Signal	Enable Power domain	Note
1	PSON	ATX PSON (12V from ATX power supply)	Signal will be enabled/disabled after delay, when Power Button is pressed.Power Button is debounced.
2	PWROK(ATX Power)	5V_EN (5V)	Note 1: If S4-4 is on, 5V is always on. S4-4 must be on, if TEBF0808 is used with external 12V instead of ATX Power. Note 2: CPLD Pullup is used for PWROK to works without external 12V only.
2	PWROK	MOD_EN (Module 3.3V), EN_LPD, EN_FPD, EN_PL	Module B2B connector Main Power and enables
3	PG_FPD	EN_DDR, EN_PLL_PWR, EN_PSGTR	Module periphery power
3	PG_PL	EN_GT_R, EN_GT_L	Module periphery power
4	PG_FPD and PG_PL	PER_EN(Periphery 3.3V), EN_1V8(Periphery 1.8V), PCI_SFP_EN (PCIe and SFP)	Carrier periphery power
4	PWROK and PG_FPD and PG_PL and PSON and Master CPLD status	FMC_EN (FMC VADJ)	FMC VADJ
5	PWROK and PG_FPD and PG_PL and PSON and POK_FMC(VADJ)	FMC_PG_C2M	FMC supply power status to FMC connector

Note: Power Status is visible on LEDs, see LED section



TE0808 module is not completely powered off with power button, if 12V power jack (J25) is used for power supply. 12V Power ON/OFF is only with ATX power supply usable.

Enable

SD's will be enabled by PWROK and PG_FPD and PG_PL and PSON;.

FMC_FAN_EN will be enabled by PWROK and PG_FPD and PG_PL and PSON_i or RGPIO (11) controlled, when active. F1PWM is constant on.

Reset

Power Button is debounced.

Reset will be also set via modified FSBL, if PCIe is detected.

Name	Description
PLL_RSTn	not RGPIO (0) when active else '1'
SRSTn	'1'
MRESETn	RST_BTN and PWROK and PG_FPD and PG_PL and PSON and "PS reboot via FSBL"
PERSTn	not RGPIO (1) and MIO31 when active else rst_btn_i and MIO31
Master CPLD Reset	PWROK and PG_FPD and PG_PL and PSON and Reset Button over CPLD interconnect.
PS reboot via FSBL	Reboot possible over FSBL over MIO30 (need for proper PCI initialization on first power on without press Reset Button)

Note: Reset Status is visible on LEDs, see LED section

Boot Mode

S5-1	S5-2	Description
------	------	-------------

ON	ON	Default, boot from SD/microSD or SPI Flash if no SD is detected
OFF	ON	Boot from eMMC
ON	OFF	Boot mode PJTAG0
OFF	OFF	Boot mode main JTAG

Note: Boot Mode Status is visible on LEDs, see LED section

UART

XMOD_TXD is sourced by MIO43 and MIO42 by XMOD_RXD.

Module SI5345

Module U5 Selection Pins are constant zero.

SD Card

SD Card selection is done via Micro SD Card detection.

SD WP is forwarded to ZynqMP from Master CPLD.

RGPIO

RGPIO Pin to FPGA	Value
0	SW1
1	SW2
2	XMOD_BTN
3	Force FSBL reboot done
4	SD_CD_S
5	SD_CD_B
6	Error
7	ERR_STAT
11-8	Boot Mode
12	PG_LPD
13	PG_DDR
14	PG_FPD
15	PG_PSGT
16	PG_GT_L
17	PG_GT_R
18	POK_FMC
19	DET_POWROK

20	PWROK
21	PG_PL
22	PG_PLL
23	PLL_LOL
24-27	reserved
28-31	Interface detection

RGPIO Pin from FPGA	Value
0	PLL_RSTn
1	PERSTn
2	FMC_FAN_EN
7	LED_N
8	LED_P
9	HDLED_N
10	HDLED_P
12-23	unused
24-27	reserved
28-31	Interface detection

LED

LED2 D6 Green (near FAN1 connector on PCB)		
Power Flags	Blink Sequence	Comment
PWROK	*****	ATX Power failed or PCB is powered off
PG_LPD	****000	Module Low Power Domain failed
PG_FPD	***0000	Module Full Power Domain failed
PG_PL	**00000	Module PL Power Domain failed
POK_1V8 or POK_FMC	*000000	Carrier 1V8 or FMC VADJ Power Domain failed
PG_DDR='0' or PG_GT_L='0' or PG_GT_R='0' or PG_PSGT='0' or PG_PLL='0'	*0000000	Module DDR, PL GT, PS GT or PLL Power Domain failed
	OFF	All Ready

LED3 D7 Red (near FAN1 connector on PCB)		
Bode Mode	Blink Sequence	Comment

Error	*****	ERROR
JTAG	*****000	JTAG
PJTAG0	****0000	Boot Mode is set to PJTAG0
eMMC	***00000	Boot Mode is set to eMMC
SPI Boot	**000000	Boot Mode is set to QSPI
SD Boot	*0000000	Boot Mode is set to SD
	ON	Reset is on

XMOD LED Red (XMOD1 on J12 with green dot)

Status	Blink Sequence	Comment
PS_INIT_B	*****	Indicates the PS is not initialized after a power-on reset (POR).
PS_ERROR_OUT	*****000	The PS_ERROR_OUT signal is asserted for accidental loss of power, an error, or an exception in the PMU.
DONE	ON or OFF	Indicates the PL configuration is completed (LED is OFF).

LED_P/N (BLUE Power LED on enclosure)

Status/ User	Blink Sequence	Comment
Power	***** (slow blink)	Indicate board is powered off.
RGPIO controlled	User Defined	RGPIO 14 and 15, if RGPIO is active.
MIO40	User Defined	MIO40, if RGPIO is deactivated

HDLED_P/N (Red HD LED on enclosure)

Status/ User	Blink Sequence	Comment
PS_INIT_B	*****	Indicates the PS is initialized after a power-on reset (POR).
PS_ERROR_OUT	*****000	The PS_ERROR_OUT signal is asserted for accidental loss of power, an error, or an exception in the PMU.
ERR_STAT	****0000	The PS_ERROR_STATUS indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.
RGPIO controlled	User Defined	RGPIO 16 and 17, if RGPIO is active
SC0	User Defined	SC0 (PL IO), if RGPIO is deactivated

Blink Frequency:

Blink Sequence	Comment
*****	~5,8 Hz
*****000	~0,7 Hz, duty cycle 5/8

***0000	~0,7 Hz, duty cycle 4/8
***00000	~0,7 Hz, duty cycle 3/8
**000000	~0,7 Hz, duty cycle 2/8
*0000000	~0,7 Hz, duty cycle 1/8

Appx. A: Change History

Revision Changes

CPLD REV05 to REV06

- LED Status changes of LED D2 D3 and HD_LED, XMOD LED
- extended Power Management

CPLD REV04 to REV05

- PS reboot via FSBL over MIO30 (need for proper PCI initialization on first power on without press Reset Button)
- SD Boot from micoSD only if switch S5-1/-2 is selected to ON
- RGPIO connection
- Add SD WP to FPGA
- Power, Rest Button debounced
- direct LED access via MIO and PL

Older Revision (PCB REV03) to CPLD REV04

- Bugfix: PCIe Reset Pin location.
- Bugfix: Swapping HDLED and PWRLED location.
- Bugfix: MEMS_CLKIN Pin location.
- Add XMOD 1 LED

Older Revision (PCB REV02) to CPLD REV04

- Add all functionality from older Revision (PCB REV03)

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV06	REV02, REV03, REV04	Error rendering macro 'page-info' Ambig	• typo correction

**Error rendering macro
'page-info'**

Ambiguous method
overloading for method
jdk.
proxy241.\$Proxy3496#h
asContentLevelPermissi
on. Cannot resolve
which method to invoke
for [null, class java.lang.
String, class com.
atlassian.confluence.
pages.Page] due to
overlapping prototypes
between: [interface com.
atlassian.confluence.
user.ConfluenceUser,
class java.lang.String,
class com.atlassian.
confluence.core.
ContentEntityObject]
[interface com.atlassian.
user.User, class java.
lang.String, class com.
atlassian.confluence.
core.
ContentEntityObject]

Error rendering macro 'page-info'

Ambiguous method overloading for
method jdk.
proxy241.\$Proxy3496#hasContentLevel
Permission. Cannot resolve which
method to invoke for [null, class java.
lang.String, class com.atlassian.
confluence.pages.Page] due to
overlapping prototypes between:
[interface com.atlassian.confluence.user.
ConfluenceUser, class java.lang.String,
class com.atlassian.confluence.core.
ContentEntityObject] [interface com.
atlassian.user.User, class java.lang.
String, class com.atlassian.confluence.
core.ContentEntityObject]



Unknown macro: 'metadata'

uous
metho
d
overlo
ading
for
metho
d jdk.
proxy2
41.\$Pr
oxy349
6#has
Conten
tLevel
Permis
sion.
Cannot
resolve
which
metho
d to
invoke
for
[null,
class
java.
lang.
String,
class
com.
atlassi
an.
confue
nce.
pages.
Page]
due to
overla
pping

prototy
pes
betwee
n:
[interfa
ce
com.
atlassi
an.
conflue
nce.
user.
Conflu
enceU
ser,
class
java.
lang.
String,
class
com.
atlassi
an.
conflue
nce.
core.
Conten
tEntity
Object]
[interfa
ce
com.
atlassi
an.
user.
User,
class
java.
lang.

				String, class com. atlassi an. conflue nce. core. Conten tEntity Object]	
2017-11-15	v.38	REV06	REV02, REV03, REV04	John Hartfiel	• Correctio n Boot Mode Section
2017-10-18	v.36	REV06	REV02, REV03, REV04	John Hartfiel	• Revision 06 finished
2017-06-20	v.29	REV05	REV02, REV03, REV04	John Hartfiel	• descriptio n and style bug- fix
2017-06-09	v.28	REV05	REV02, REV03, REV04	John Hartfiel	• Revision 05 finished
2017-06-08	v.23	REV05	REV02, REV03, REV04	John Hartfiel	• Documen t style update
2017-05-08	v.22	REV05	REV02, REV03, REV04	John Hartfiel	• Revision 05 working in process
2017-02-08	v.19	REV04	REV02, REV03, REV04	John Hartfiel	• Revision 04 finished
2016-04-11	v.1	---			• Initial release

Error
render
ing
macro
'page-
info'

Ambig
uous
metho
d
overlo
ading
for
metho
d jdk.
proxy2
41.\$Pr
oxy349
6#has
Conten
tLevel
Permis
sion.
Cannot
resolve
which
metho
d to
invoke
for
[null,
class
java.
lang.
String,
class
com.
atlassi
an.

confluence.
pages.
Page]
due to
overlapping
prototypes
between:
[interface
com.
atlassian.
confluence.
user.
ConfluenceUser,
class
java.
lang.
String,
class
com.
atlassian.
confluence.
core.
ContentEntity
Object]
[interface
com.

				atlassi an. user. User, class java. lang. String, class com. atlassi an. conflue nce. core. Conten tEntity Object]	
	All			Error render ing macro 'page- info' Ambig uous metho d overlo ading for metho d jdk. proxy2	

41.\$Pr
oxy349
6#has
Conten
tLevel
Permis
sion.
Cannot
resolve
which
metho
d to
invoke
for
[null,
class
java.
lang.
String,
class
com.
atlassi
an.
conflue
nce.
pages.
Page]
due to
overla
pping
prototy
pes
betwee
n:
[interfa
ce
com.
atlassi
an.

confluence.
user.
ConfluenceUser,
class
java.
lang.
String,
class
com.
atlassian.
confluence.
core.
ContentEntity
Object]
[interface
com.
atlassian.
user.
User,
class
java.
lang.
String,
class
com.
atlassian.
confluence.
core.
Content

				tEntity Object]	
--	--	--	--	--------------------	--

Appx. B: Legal Notices

Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

Document Warranty

The material contained in this document is provided "as is" and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method `jdk.proxy241.$Proxy3496#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`