

Custom Block Design IPs

Create user defined AXI4 peripheral IP-Core

1. Start Vivado
2. Start IP Manager --> New IP Location...



- a. Creating a new IP Core Location - this will be a location for an Vivado Project that "hosts" all your IP Cores you develop. It is recommended to set the default part in this project to some device you use more frequently.

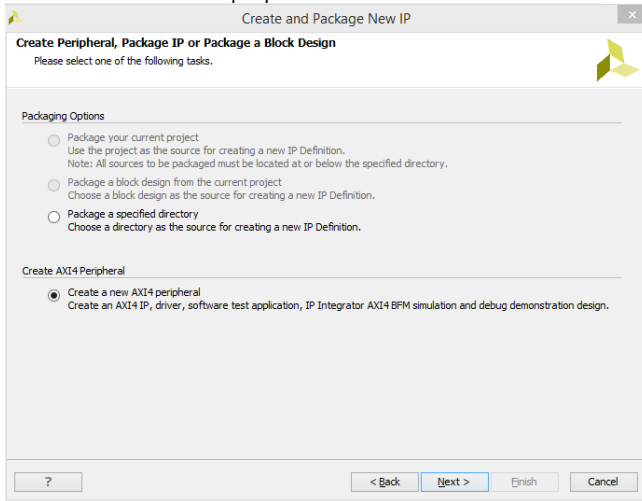


It is not recommended to Create New IP Cores, or start IP Core Editor from existing Projects that use Board Part Flow.

3. Select FPGA, Language, Location... Click Finished
4. Click Tools Create and Package IP
5. Click Next

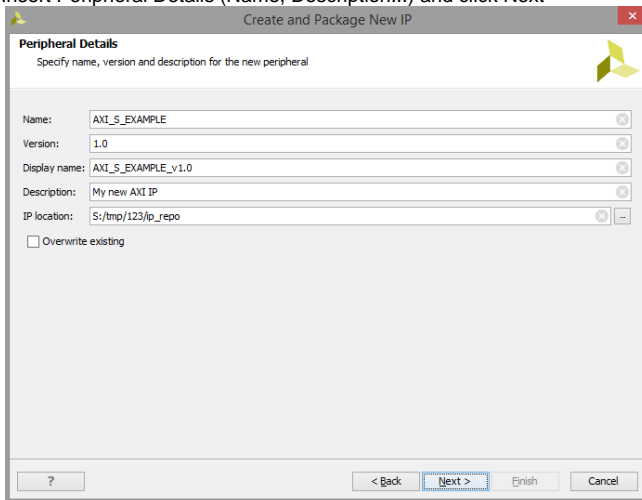


6. Select "Create a new AXI peripheral" and click Next



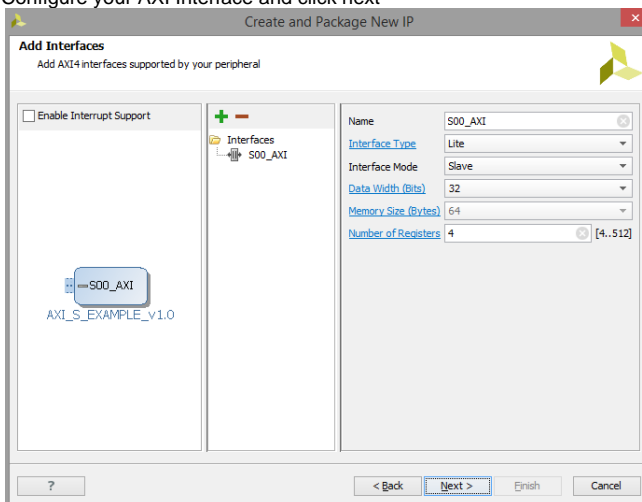
The dialog box is titled "Create and Package New IP". It has a sub-header "Create Peripheral, Package IP or Package a Block Design" and a note "Please select one of the following tasks." Below this, there are two sections. The first section, "Packaging Options", has three radio buttons: "Package your current project" (with a note "Use the project as the source for creating a new IP Definition. Note: All sources to be packaged must be located at or below the specified directory."), "Package a block design from the current project" (with a note "Choose a block design as the source for creating a new IP Definition."), and "Package a specified directory" (with a note "Choose a directory as the source for creating a new IP Definition."). The second section, "Create AXI4 Peripheral", has a selected radio button "Create a new AXI4 peripheral" with a note "Create an AXI4 IP, driver, software test application, IP Integrator AXI4 BFM simulation and debug demonstration design." At the bottom, there are buttons for "< Back", "Next >", "Finish", and "Cancel".

7. Insert Peripheral Details (Name, Description...) and click Next



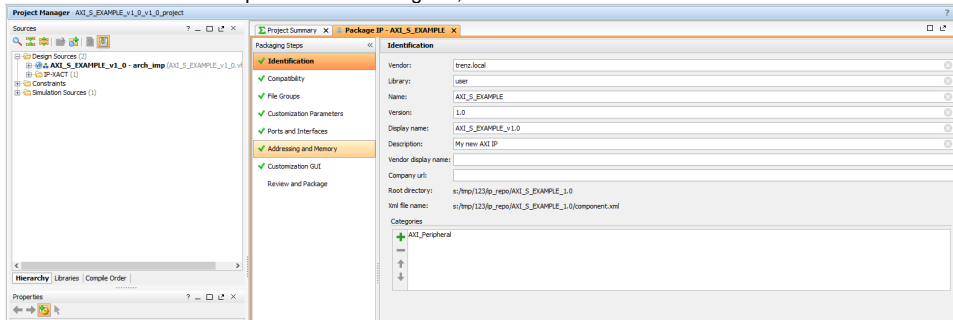
The dialog box is titled "Create and Package New IP" and has a sub-header "Peripheral Details" with a note "Specify name, version and description for the new peripheral". It contains several text input fields: "Name:" (AXI_S_EXAMPLE), "Version:" (1.0), "Display name:" (AXI_S_EXAMPLE_v1.0), "Description:" (My new AXI IP), and "IP location:" (S:/tmp/123/ip_repo). There is a checkbox "Overwrite existing" which is unchecked. At the bottom, there are buttons for "< Back", "Next >", "Finish", and "Cancel".

8. Configure your AXI Interface and click next



The dialog box is titled "Create and Package New IP" and has a sub-header "Add Interfaces" with a note "Add AXI4 interfaces supported by your peripheral". It has a checkbox "Enable Interrupt Support" which is unchecked. On the left, there is a tree view showing "Interfaces" and "S00_AXI". Below this, there is a diagram showing a block labeled "S00_AXI" connected to a block labeled "AXI_S_EXAMPLE_v1.0". On the right, there are configuration fields for the selected interface: "Name" (S00_AXI), "Interface Type" (Lite), "Interface Mode" (Slave), "Data Width (Bits)" (32), "Memory Size (Bytes)" (64), and "Number of Registers" (4) with a range of [4..512]. At the bottom, there are buttons for "< Back", "Next >", "Finish", and "Cancel".

9. Select Edit IP and click Finish
10. Edit your IP-Core and insert your own HDL-Code into the project
 - a. Your own HDL Files should be located into the sub-folter <IP Management Project Location>/ip_repo/<IP-Name>/hdl/...
 - b. All other relevant IP Files should also located into the IP-Repo folder <IP-Name>
 - c. For detailed description of customizing IPs, see Xilinx documentation



Reference

- Vivado Design Suite - Creating, Packaging Custom IP Tutorial (UG1119)
- Vivado Design Suite - Creating, Packaging Custom IP (UG1118)