Custom Block Design IPs

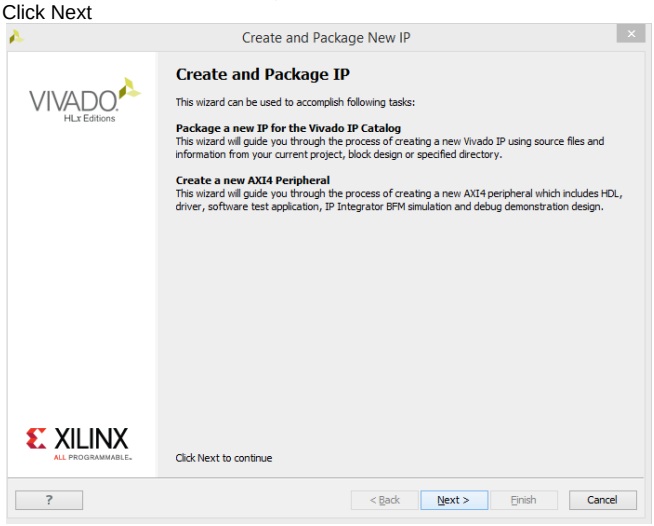
Create user defined AXI4 peripheral IP-Core

1. Start Vivado
2. Start IP Manager --> New IP Location...

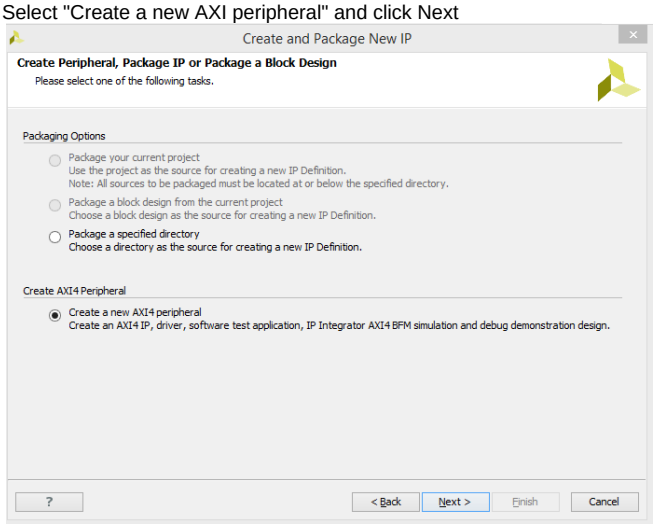
   a. Creating a new IP Core Location - this will be a location for an Vivado Project that "hosts" all your IP Cores you develop. It is recommended to set the default part in this project to some device you use more frequently.

> ⚠ It is not recommended to Create New IP Cores, or start IP Core Editor from existing Projects that use Board Part Flow.

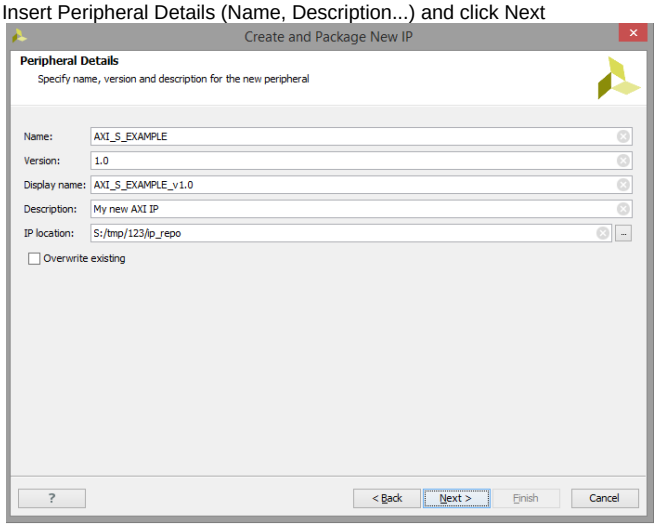
3. Select FPGA, Language,Location... Click Finished
4. Click Tools Create and Package IP
5. Click Next



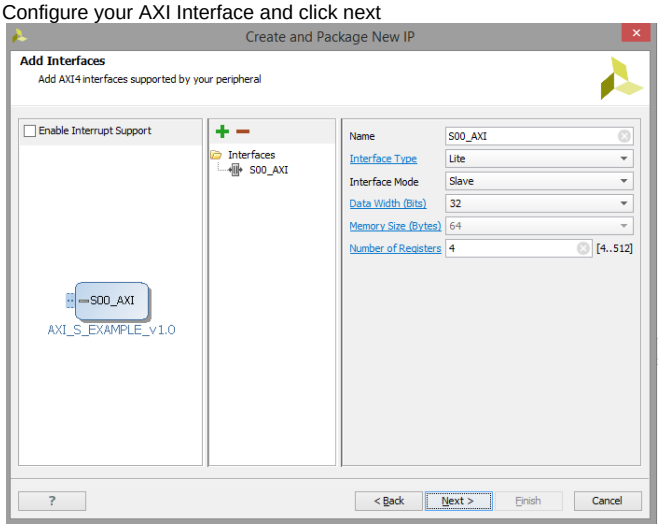
6. Select "Create a new AXI peripheral" and click Next



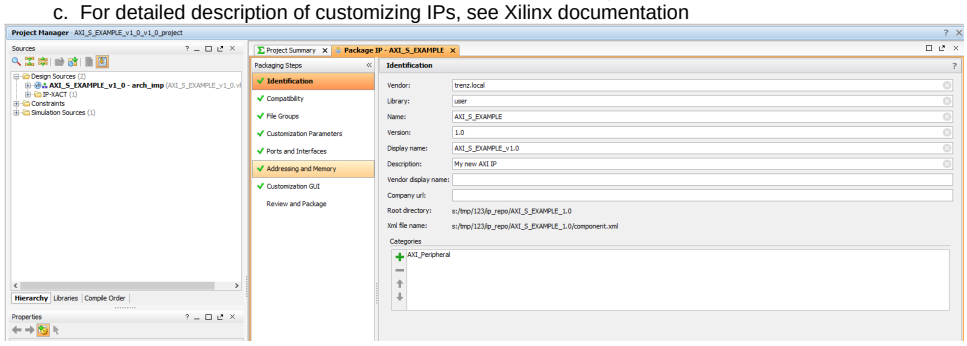
7. Insert Peripheral Details (Name, Description...) and click Next



8. Configure your AXI Interface and click next



9. Select Edit IP and click Finish
10. Edit your IP-Core and insert your own HDL-Code into the project
    a. Your own HDL Files should be located into the sub-folter <IP Management Project Location>/ip_repo/<IP-Name>/hdl/...
    b. All other relevant IP Files should also located into the IP-Repo folder <IP-Name>
    c. For detailed description of customizing IPs, see Xilinx documentation



Reference

- Vivado Design Suite - Creating, Packaging Custom IP Tutorial (UG1119)
- Vivado Design Suite - Creating, Packaging Custom IP (UG1118)