# TE Board Part Files

Most of the TE modules are available in different assembly options. Assembly option with different FPGA/SOC devices or other DDR sizes need an own board part file. In some cases also a PCB revision changes or a special carrier module combination needs a separate board part.

It's recommended to use the board part files only for this Vivado Version, for which it has been provided. Depending on the Schema Version of the XML-Files and Xilinx IP definitions, it is possible to use them with other Vivado versions, see Xilinx ug895.

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## Naming Conventions and Version

This Naming Convention will be used for the most Vivado 2016.2 Board Part Files and newer one.

Board Part Files consists on a base folder, a version sub folder with three xml files and one picture:

- Every assembly option of a module/carrier series where FPGA-Typ (Size, Speed/Temperature Grade) is changed, gets a new base folder.
- Every other assembly option or PCB-revision change, which has affects on the reference design settings, gets a new version sub folder.

### Board Part Base Folder

Board Part Names of the base folder consists of max. three parts separated by underline character.

| | Usage of the part of name | Example 1 | Example 2 | Example 3 | Example 4 |
|---|---|---|---|---|---|
| **Name of the PCB Series** | Always | TE0726 | TE0745 | TE0720 | TE0711 |
| **FPGA Size** | Optional | | 30 | | 35 |
| **FPGA Speed/Temperature Grade** | Optional | | | 1C | 2C |

### Board Part Version Folder

Version folder Name consists on a major and minor number separated by a dot (<major>.<minor>, example 1.0) Different Version folder means:

| | |
|---|---|
| **Major** | • Changes on assembly option, which has effects on the reference design, for example DDR Size<br>• Boart Part for special Carrier/Module combination |
| **Minor** | • Changes on PCB-Revision, which has effects on the reference design |

Attention: Changes on the settings of the TE Board Part Files by itself are not under version control at the moment, like described in Xilinx ug895. XML file includes a comment header with the date of the last change of the selected file.

# Location

Board Part Files will be delivered with our Reference Designs on our https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/<group>/<form factor>/<module_name>/Reference_Design/<vivado_version>/<design_name>.

Board Part Files are locate in the sub folder <design_name>/board_files/ of the downloadable Reference Design. For detailed information of the zip-file folder structure see: Project Delivery - Directory Structure.

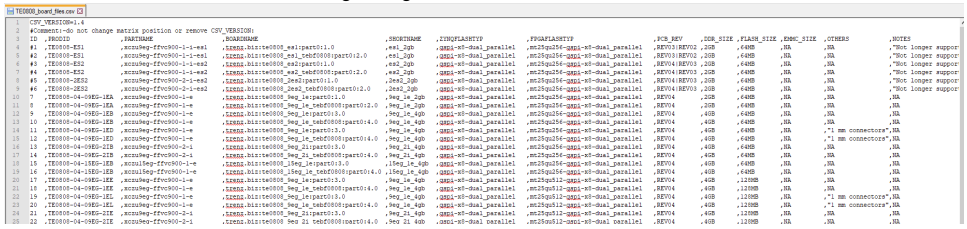
This folder includes also a *_board_files.csv file with a list of all available board parts. This list is only used by TE-Scripts.

# Select Correct Board Part Files

Since 2018.3 special "Module Selection Guide" is included into "_create_win_setup.cmd" and "_create_linux_setup.sh"

- **Execute** "_create_win_setup.cmd" or "_create_linux_setup.sh"
- **Select** "Module Selection Guide" (press "0" and Enter)
- **Follow instructions**

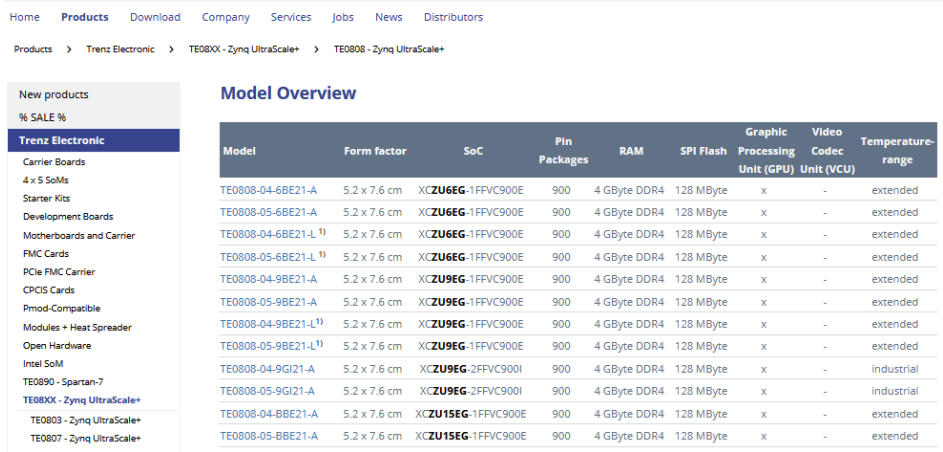
- Check <design_name>/board_files/<board_series>_board_files.csv for available board part of the reference design:
  - The table shows all available board parts, which are delivered with the reference design
  - "ID" Unique ID for every board file in the project delivery
  - "PRODID" is the  whole article name, latest reference design are available with all variants
  - "PARTNAME is the FPGA device setting of Vivado for the assembly variant
  - "BOARDNAME" is  the corresponding board part file, which is used, files location is in "./board_files/<basename>/<Xil file id>/"
  - "SHORTNAME" is the name for the board part specific sub folders in the reference design
  - "ZYNQFLASHTYP" is the setting to configure the Flash via SDK
  - "FPGAFLASHTYP" is the setting to configure the Flash via Vivado (first part only), the second and third part are QSPI mode and memory size in MB
  - "PCB_REV" is supporte PCB Revision
  -"DDR_SIZE"  is DDR size if available
  -"FLASH_SIZE"  is Flash size if available
  -"EMMC_SIZE"  is eMMC size if available
  -"OTHERS"  other HW notes
  -"NOTES"  additional notes
  -"DESIGN"  filter for the reference design usage



| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | CSV_VERSION=1.4 | | | | | | | | | | | | |
| 2 | #Comment:-Do not change matrix position or remove CSV_VERSION! | | | | | | | | | | | | |
| 3 | ID ,PRODID | ,PARTNAME | ,BOARDNAME | ,SHORTNAME | ,ZYNQFLASHTYP | ,FPGAFLASHTYP | ,PCB_REV | ,DDR_SIZE | ,FLASH_SIZE | ,EMMC_SIZE | ,OTHERS | ,NOTES | |
| 4 | #1 ,TE0808-ES1 | ,xczu9eg-ffvc900-1-i-es1 | ,trenz.biz:te0808_es1:part0:1.0 | ,es1_2gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV03\|REV02 | ,2GB | ,64MB | ,NA | ,NA | ,"Not longer suppor | |
| 5 | #2 ,TE0808-ES1 | ,xczu9eg-ffvc900-1-i-es1 | ,trenz.biz:te0808_es1_tebf0808:part0:2.0 | ,es1_2gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV03\|REV02 | ,2GB | ,64MB | ,NA | ,NA | ,"Not longer suppor | |
| 6 | #3 ,TE0808-ES2 | ,xczu9eg-ffvc900-1-i-es2 | ,trenz.biz:te0808_es2:part0:1.0 | ,es2_2gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04\|REV03 | ,2GB | ,64MB | ,NA | ,NA | ,"Not longer suppor | |
| 7 | #4 ,TE0808-ES2 | ,xczu9eg-ffvc900-1-i-es2 | ,trenz.biz:te0808_es2_tebf0808:part0:2.0 | ,es2_2gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04\|REV03 | ,2GB | ,64MB | ,NA | ,NA | ,"Not longer suppor | |
| 8 | #5 ,TE0808-2ES2 | ,xczu9eg-ffvc900-2-i-es2 | ,trenz.biz:te0808_2es2:part0:1.0 | ,2es2_2gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04\|REV03 | ,2GB | ,64MB | ,NA | ,NA | ,"Not longer suppor | |
| 9 | #6 ,TE0808-2ES2 | ,xczu9eg-ffvc900-2-i-es2 | ,trenz.biz:te0808_2es2_tebf0808:part0:2.0 | ,2es2_2gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04\|REV03 | ,2GB | ,64MB | ,NA | ,NA | ,"Not longer suppor | |
| 10 | 7 ,TE0808-04-09EG-1EA | ,xczu9eg-ffvc900-1-e | ,trenz.biz:te0808_9eg_1e:part0:1.0 | ,9eg_1e_2gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04 | ,2GB | ,64MB | ,NA | ,NA | ,NA | |
| 11 | 8 ,TE0808-04-09EG-1EA | ,xczu9eg-ffvc900-1-e | ,trenz.biz:te0808_9eg_1e_tebf0808:part0:2.0 | ,9eg_1e_2gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04 | ,2GB | ,64MB | ,NA | ,NA | ,NA | |
| 12 | 9 ,TE0808-04-09EG-1EB | ,xczu9eg-ffvc900-1-e | ,trenz.biz:te0808_9eg_1e:part0:3.0 | ,9eg_1e_4gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,64MB | ,NA | ,NA | ,NA | |
| 13 | 10 ,TE0808-04-09EG-1EB | ,xczu9eg-ffvc900-1-e | ,trenz.biz:te0808_9eg_1e_tebf0808:part0:4.0 | ,9eg_1e_4gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,64MB | ,NA | ,NA | ,NA | |
| 14 | 11 ,TE0808-04-09EG-1ED | ,xczu9eg-ffvc900-1-e | ,trenz.biz:te0808_9eg_1e:part0:3.0 | ,9eg_1e_4gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,64MB | ,NA | ,"1 mm connectors" | ,NA | |
| 15 | 12 ,TE0808-04-09EG-1ED | ,xczu9eg-ffvc900-1-e | ,trenz.biz:te0808_9eg_1e_tebf0808:part0:4.0 | ,9eg_1e_4gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,64MB | ,NA | ,"1 mm connectors" | ,NA | |
| 16 | 13 ,TE0808-04-09ED-21B | ,xczu9eg-ffvc900-2-i | ,trenz.biz:te0808_9eg_2i:part0:3.0 | ,9eg_2i_4gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,64MB | ,NA | ,NA | ,NA | |
| 17 | 14 ,TE0808-04-09EG-21B | ,xczu9eg-ffvc900-2-i | ,trenz.biz:te0808_9eg_2i_tebf0808:part0:4.0 | ,9eg_2i_4gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,64MB | ,NA | ,NA | ,NA | |
| 18 | 15 ,TE0808-04-15EG-1EB | ,xczu15eg-ffvc900-1-e | ,trenz.biz:te0808_15eg_1e:part0:3.0 | ,15eg_1e_4gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,64MB | ,NA | ,NA | ,NA | |
| 19 | 16 ,TE0808-04-15EG-1EB | ,xczu15eg-ffvc900-1-e | ,trenz.biz:te0808_15eg_1e_tebf0808:part0:4.0 | ,15eg_1e_4gb | ,qspi-x8-dual_parallel | ,mt25qu256-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,64MB | ,NA | ,NA | ,NA | |
| 20 | 17 ,TE0808-04-09EG-1EE | ,xczu9eg-ffvc900-1-e | ,trenz.biz:te0808_9eg_1e:part0:3.0 | ,9eg_1e_4gb | ,qspi-x8-dual_parallel | ,mt25qu512-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,128MB | ,NA | ,NA | ,NA | |
| 21 | 18 ,TE0808-04-09EG-1EE | ,xczu9eg-ffvc900-1-e | ,trenz.biz:te0808_9eg_1e_tebf0808:part0:4.0 | ,9eg_1e_4gb | ,qspi-x8-dual_parallel | ,mt25qu512-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,128MB | ,NA | ,NA | ,NA | |
| 22 | 19 ,TE0808-04-09EG-1EL | ,xczu9eg-ffvc900-1-e | ,trenz.biz:te0808_9eg_1e:part0:3.0 | ,9eg_1e_4gb | ,qspi-x8-dual_parallel | ,mt25qu512-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,128MB | ,NA | ,"1 mm connectors" | ,NA | |
| 23 | 20 ,TE0808-04-09EG-1EL | ,xczu9eg-ffvc900-1-e | ,trenz.biz:te0808_9eg_1e_tebf0808:part0:4.0 | ,9eg_1e_4gb | ,qspi-x8-dual_parallel | ,mt25qu512-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,128MB | ,NA | ,"1 mm connectors" | ,NA | |
| 24 | 21 ,TE0808-04-09ED-2IE | ,xczu9eg-ffvc900-2-i | ,trenz.biz:te0808_9eg_2i:part0:3.0 | ,9eg_2i_4gb | ,qspi-x8-dual_parallel | ,mt25qu512-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,128MB | ,NA | ,NA | ,NA | |
| 25 | 22 ,TE0808-04-09ED-2IE | ,xczu9eg-ffvc900-2-i | ,trenz.biz:te0808_9eg_2i_tebf0808:part0:4.0 | ,9eg_2i_4gb | ,qspi-x8-dual_parallel | ,mt25qu512-qspi-x8-dual_parallel | ,REV04 | ,4GB | ,128MB | ,NA | ,NA | ,NA | |

- Check your order number and/or TE shop page to get module information of your PCB:
  - https://shop.trenz-electronic.de/en/Products/Trenz-Electronic/<device familie>/<TE module serie>

- "Model Overview" shows the basic difference between the assembly options, in the most cases different footprint compatible FPGAs or RAM size. Assembly options (like different connector) which has no affect on board parts settings, has no separate board part files.



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TE0803 - Zynq UltraScale+
TE0807 - Zynq UltraScale+

## Model Overview

| Model | Form factor | SoC | Pin Packages | RAM | SPI Flash | Graphic Processing Unit (GPU) | Video Codec Unit (VCU) | Temperature-range |
|---|---|---|---|---|---|---|---|---|
| TE0808-04-6BE21-A | 5.2 x 7.6 cm | XC**ZU6EG**-1FFVC900E | 900 | 4 GByte DDR4 | 128 MByte | x | - | extended |
| TE0808-05-6BE21-A | 5.2 x 7.6 cm | XC**ZU6EG**-1FFVC900E | 900 | 4 GByte DDR4 | 128 MByte | x | - | extended |
| TE0808-04-6BE21-L [1)] | 5.2 x 7.6 cm | XC**ZU6EG**-1FFVC900E | 900 | 4 GByte DDR4 | 128 MByte | x | - | extended |
| TE0808-05-6BE21-L [1)] | 5.2 x 7.6 cm | XC**ZU6EG**-1FFVC900E | 900 | 4 GByte DDR4 | 128 MByte | x | - | extended |
| TE0808-04-9BE21-A | 5.2 x 7.6 cm | XC**ZU9EG**-1FFVC900E | 900 | 4 GByte DDR4 | 128 MByte | x | - | extended |
| TE0808-05-9BE21-A | 5.2 x 7.6 cm | XC**ZU9EG**-1FFVC900E | 900 | 4 GByte DDR4 | 128 MByte | x | - | extended |
| TE0808-04-9BE21-L [1)] | 5.2 x 7.6 cm | XC**ZU9EG**-1FFVC900E | 900 | 4 GByte DDR4 | 128 MByte | x | - | extended |
| TE0808-05-9BE21-L [1)] | 5.2 x 7.6 cm | XC**ZU9EG**-1FFVC900E | 900 | 4 GByte DDR4 | 128 MByte | x | - | extended |
| TE0808-04-9GI21-A | 5.2 x 7.6 cm | XC**ZU9EG**-2FFVC900I | 900 | 4 GByte DDR4 | 128 MByte | x | - | industrial |
| TE0808-05-9GI21-A | 5.2 x 7.6 cm | XC**ZU9EG**-2FFVC900I | 900 | 4 GByte DDR4 | 128 MByte | x | - | industrial |
| TE0808-04-BBE21-A | 5.2 x 7.6 cm | XC**ZU15EG**-1FFVC900E | 900 | 4 GByte DDR4 | 128 MByte | x | - | extended |
| TE0808-05-BBE21-A | 5.2 x 7.6 cm | XC**ZU15EG**-1FFVC900E | 900 | 4 GByte DDR4 | 128 MByte | x | - | extended |

- Select your board part file on design_basic_settings.cmd/sh:
  Use unique name from CSV list (see 1.)
  - Unique names are ID or PRODID (in the most cases) or BOARDNAME or SHORTNAME
  - Revision number of the PRODID is the last one, which was available on last board part update. If there is no special board part for older revisions, this will be backward compatible. Please verify this on Vivado, see 4.

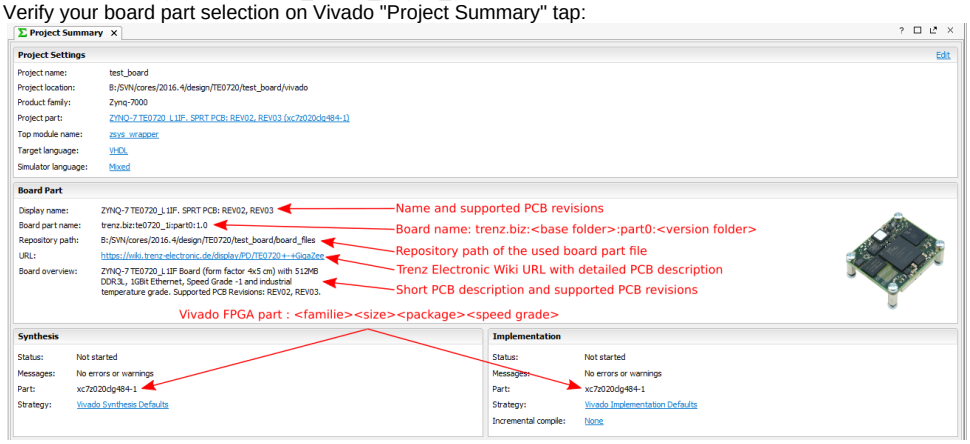


```
29  $REM ------------------
30  $REM Set Board part number of the project which should be created
31  $REM   -Available Numbers: (you can use ID, PRODID, BOARDNAME or SHORTNAME from \board_files\TExxxx_board_file.csv list) or special name "LAST_ID" to get the board with the highest ID in the *.csv list
32  $REM   -variable is used for project creation and programming
33  $REM   -Example TE0726 Module :
34  $REM      -USE ID              |USE PRODID              |Use BOARDNAME                          |Use SHORTNAME
35  $REM      -$set PARTNUMBER=1|$set PARTNUMBER=te0726-3m  |$set PARTNUMBER=trenz.biz:te0726_m:part0:3.1  |$set PARTNUMBER=te0726_m
36  $set PARTNUMBER=LAST_ID
```

Select your board part here

See Reference Design: Getting Started for more details.

- Create Vivado Project with vivado_create_project_guimode.cmd/sh
- Verify your board part selection on Vivado "Project Summary" tap:



Project Summary

**Project Settings** Edit

Project name: test_board
Project location: B:/SVN/cores/2016.4/design/TE0720/test_board/vivado
Product family: Zynq-7000
Project part: ZYNQ-7 TE0720_1_1IF. SPRT PCB: REV02, REV03 (xc7z020clg484-1)
Top module name: zsys_wrapper
Target language: VHDL
Simulator language: Mixed

**Board Part**

Display name: ZYNQ-7 TE0720_1_1IF. SPRT PCB: REV02, REV03 ← Name and supported PCB revisions
Board part name: trenz.biz:te0720_1i:part0:1.0 ← Board name: trenz.biz:<base folder>:part0:<version folder>
Repository path: B:/SVN/cores/2016.4/design/TE0720/test_board/board_files ← Repository path of the used board part file
URL: https://wiki.trenz-electronic.de/display/PD/TE0720+-+GigaZee ← Trenz Electronic Wiki URL with detailed PCB description
Board overview: ZYNQ-7 TE0720_1_1IF Board (form factor 4x5 cm) with 512MB DDR3L, 1GBit Ethernet, Speed Grade -1 and industrial temperature grade. Supported PCB Revisions: REV02, REV03. ← Short PCB description and supported PCB revisions

Vivado FPGA part : <familie><size><package><speed grade>

**Synthesis**
Status: Not started
Messages: No errors or warnings
Part: xc7z020clg484-1
Strategy: Vivado Synthesis Defaults

**Implementation**
Status: Not started
Messages: No errors or warnings
Part: xc7z020clg484-1
Strategy: Vivado Implementation Defaults
Incremental compile: None

# Installation

See Vivado Board Part Installation and Project Delivery - QuickStart