

TE0726 CPLD

Table of contents

- 1 [Table of contents](#)
- 2 [Overview](#)
 - 2.1 [Feature Summary](#)
 - 2.2 [Firmware Revision and supported PCB Revision](#)
- 3 [Product Specification](#)
 - 3.1 [Port Description](#)
 - 3.2 [Functional Description](#)
 - 3.2.1 [UART](#)
 - 3.2.2 [CSI-GPIO](#)
 - 3.2.3 [DSI](#)
 - 3.2.4 [LED](#)
- 4 [Appx. A: Change History](#)
 - 4.1 [Revision Changes](#)
 - 4.2 [Document Change History](#)
- 5 [Appx. B: Legal Notices](#)
 - 5.1 [Data Privacy](#)
 - 5.2 [Document Warranty](#)
 - 5.3 [Limitation of Liability](#)
 - 5.4 [Copyright Notice](#)
 - 5.5 [Technology Licenses](#)
 - 5.6 [Environmental Protection](#)
 - 5.7 [REACH, RoHS and WEEE](#)

Overview

CPLD Device with designator U11: LCMX02-256HC

Feature Summary

- FPGA UART routing
- CSI_GPIO routing

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Description
C_TCK / BDBUS0	in	30	UART from FTDI
C_TDI / BDBUS1	out	32	UART to FTDI
C_TDO / BDBUS2	in	1	/ currently_not_used
C_TMS / BDBUS3	in	29	/ currently_not_used

CSI_GPIO0 / CSI_IO0	out	25	drive by MIO52
CSI_GPIO1 / CSI_IO1	out	23	drive by MIO53
DONE	in	8	FPGA DONE Pin
DSI_C_N		12	/ currently_not_used
DSI_C_P		11	/ currently_not_used
DSI_D0_N		10	/ currently_not_used
DSI_D0_P		9	/ currently_not_used
DSI_D1_N		14	/ currently_not_used
DSI_D1_P		13	/ currently_not_used
DSI_XA		16	/ currently_not_used
DSI_XB		17	/ currently_not_used
GLD	out	5	LED
JMODE		26	Enable JTAG access to CPLD for Firmware update (zero: normal IOs, one: CPLD JTAG access). Selectable over J15 Jumper
MIO52	in	20	connected to CSI_GPIO0
MIO53	in	21	connected to CSI_GPIO1
MIO8	in	28	UART from Zynq
MIO9	out	27	UART to Zynq
RLED	out	4	LED

Functional Description

UART

UART connection between MIO8/9 and BDBUS0/1.

CSI-GPIO

CSI_GPIO0 drives by MIO52, CSI_GPIO1 drives by MIO53.

DSI

Not used

LED


LED	Description
GREEN	ON when Zynq Done pin is down else OFF
RED	UART activity

Appx. A: Change History

Revision Changes

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
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2017-05-22	v.3	REV01	REV01, REV02, REV03	John Hartfiel	Revision 01 finished
2017-03-02	v.1	REV01	REV01, REV02, REV03	<div></div>	Initial release

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Appx. B: Legal Notices

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REACH, RoHS and WEEE

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