TEB0911 Master CPLD

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Overview

Firmware for PCB-Master CPLD with designator U27:LCMXO2-1200HC

Feature Summary

- Power Management
- Reset Management
- FMC JTAG Management
- FPGA Boot Mode
- RGPIO Interface to FPGA

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name/ opt. VHD Name	Direction	Pin	Description
B64_T1	out	20	FPGA IO / Master RGPIO TX

DC4 T2	in	10	EDCA IO / Moster DCDIO DV
B64_T2	in .	19	FPGA IO / Master RGPIO RX
B64_T3	in	21	FPGA IO / Master RGPIO CLK
B65_T1	out	22	FPGA IO / Slave RGPIO TX
B65_T2	in	24	FPGA IO / Slave RGPIO RX
B65_T3	in	23	FPGA IO / Slave RGPIO CLK
С_ТСК	in	131	JTAG
C_TDI	in	136	JTAG
C_TDO1	out	137	JTAG
C_TMS	in	130	JTAG
DDR_EN/EN_DDR	out	126	Power control
DDR_PG		121	Power control / currently_not_used
DONE	in	4	FPGA Control
DP_EN	out	34	Power control
EN_12V	out	114	Power control
EN_3.3V	out	112	Power control
EN_A_3V3	out	143	Power control
EN_AF_1V8	out	110	Power control
EN_B_3V3	out	74	Power control
EN_BC_1V8	out	84	Power control
EN_C_3V3	out	76	Power control
EN_D_3V3	out	78	Power control
EN_DE_1V8	out	77	Power control
EN_E_3V3	out	82	Power control
EN_F_3V3	out	104	Power control
EN_GT_L	out	122	Power control
EN_GT_R	out	125	Power control
EN_SFP	out	111	Power control
EN_SFP_SSD	out	3	Power control
EN_VCCINT	out	119	Power control
FAN_A_EN	out	106	Fan control
FAN_B_EN	out	83	Fan control
FAN_C_EN	out	81	Fan control
FAN_D_EN	out	75	Fan control
FAN_E_EN	out	73	Fan control
FAN_F_EN	out	109	Fan control
FMC12V_EN/EN_FMC_12V	out	95	Power control
FMC12V_PG		93	Power control / currently_not_used
FMCA_PG_C2M		142	Power control / currently_not_used
FMCA_PG_M2C		141	Power control / currently_not_used
FMCA_PRSNT	in	140	FMC

FMCA_TCK	out	139	FMC / JTAG
FMCA_TDI	out	138	FMC / JTAG
FMCA_TDO	in	133	FMC / JTAG
FMCA_TMS	out	132	FMC / JTAG
FMCB_PG_C2M		38	FMC / currently_not_used
FMCB_PG_M2C		39	FMC / currently_not_used
FMCB_PRSNT	in	40	FMC
FMCB_TCK	out	41	FMC / JTAG
FMCB_TDI	out	42	FMC / JTAG
FMCB_TDO	in	43	FMC / JTAG
FMCB_TMS	out	44	FMC / JTAG
FMCC_PG_C2M		54	FMC / currently_not_used
FMCC_PG_M2C		55	FMC / currently_not_used
FMCC_PRSNT	in	56	FMC
FMCC_TCK	out	57	FMC / JTAG
FMCC_TDI	out	58	FMC / JTAG
FMCC_TDO	in	59	FMC / JTAG
FMCC_TMS	out	60	FMC / JTAG
FMCD_PG_C2M		45	FMC / currently_not_used
FMCD_PG_M2C		47	FMC / currently_not_used
FMCD_PRSNT	in	61	FMC
FMCD_TCK	out	48	FMC / JTAG
FMCD_TDI	out	49	FMC / JTAG
FMCD_TDO	in	50	FMC / JTAG
FMCD_TMS	out	52	FMC / JTAG
FMCE_PG_C2M		62	FMC / currently_not_used
FMCE_PG_M2C		65	FMC / currently_not_used
FMCE_PRSNT	in	67	FMC
FMCE_TCK	out	68	FMC / JTAG
FMCE_TDI	out	69	FMC / JTAG
FMCE_TDO	in	70	FMC / JTAG
FMCE_TMS	out	71	FMC / JTAG
FMCF_PG_C2M		107	FMC / currently_not_used
FMCF_PG_M2C		105	FMC / currently_not_used
FMCF_PRSNT	in	100	FMC
FMCF_TCK	out	99	FMC / JTAG
FMCF_TDI	out	98	FMC / JTAG
FMCF_TDO	in	97	FMC / JTAG
FMCF_TMS	out	96	FMC / JTAG
INIT_B	in	5	FPGA Control
	1		I .

JTAGENB		120	enable JTAG access to CPLD (one CPLD, zero FMC chain)
MIO24		1	FGPA MIO / currently_not_used
MIO25		2	FGPA MIO / currently_not_used
MODE0	out	10	FPGA Boot Mode
MODE1	out	12	FPGA Boot Mode
MODE2	out	9	FPGA Boot Mode
MODE3	out	11	FPGA Boot Mode
MR	out	92	FPGA Control
PG_12V	in	113	Power control
PG_FPD	in	115	Power control
PG_GT_L	in	13	Power control
PG_GT_R	in	35	Power control
PG_PSGT	in	128	Power control
PROG_B	out	6	FPGA Control
PSGT_EN/EN_GT_PS	out	117	Power control
SC_IO0	out	25	Slave CPLD / Reset
SC_IO1		26	Slave CPLD / currently_not_used
SC_IO2		27	Slave CPLD / currently_not_used
SC_IO3	in	28	Slave CPLD / Slave RGPIO TX_IN
SC_IO4	out	32	Slave CPLD / Slave RGPIO RX_OUT
SC_IO5	out	33	Slave CPLD / Slave RGPIO CLK_out
SC_SW1	in	127	DIP Switch S3-3
SC_SW2	in	85	DIP Switch S3-4
SC1_IO_SB		91	Slave CPLD / currently_not_used
SC2_IO_SB		86	Slave CPLD / currently_not_used

Functional Description

JTAG

JTAGENB set CPLD into the Chain for Firmware update. In normal mode every FMC JTAG will be set into the chain, when his FMCx_PRSNT is detected.

Power

EN_12V and EN_VCCINT are enabled on power up. All other power enables will be set, if PG_12V and PG_FPD are valid.

Reset

PROG_B always one. MR and SC_IO0 controlled by USR_BUT2 (S2) and power management.

Bootmode

SD Boot, when SC_SW1 is one else SQPI Boot.

S4-3	S4-5	Description
OFF	OFF	SD1 Boot
OFF	ON	PJTAG0
ON	OFF	QSPI32
ON	ON	JTAG

FANs

6 FMC FANs controlled by corresponding FMCx_PRSNT signals to enable FANs only for active FMC slots.

RGPIO

RGPIO Master is a 32Bit Remote GPIO Interface to talk with FPGA over 3 lanes.

RGPIO Pin to FPGA	Value
0-3	current Boot Mode
4	SC_SW1
5	SC_SW2
6-7	unused
8-13	FMCAF_PRSNT
14-19	unused
20	PG_PSGT
21	PG_GT_L
22	PG_GT_R
23	unused
24-27	reserved
28-31	interface detection

RGPIO Pin from FPGA	Value
0-23	unused
24-27	reserved
28-31	interface detection

RGPIO slave is routed directly to Slave CPLD.

Appx. A: Change History

Revision Changes

CPLD REV04 to REV05

- more Boot Modes selectable
- Power startup sequence

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

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2017-05-24	v.26	REV02	REV01	John Hartfiel	Revision 02 finished
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Appx. B: Legal Notices

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