

TEB0911 Slave CPLD

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Overview

Firmware for PCB-Slave CPLD with designator U83: LCMXO2-1200HC

Feature Summary

- FAN Control and PWN generation with I2C control
- Reset Management
- FPGA UART routing
- Displayport routing
- LED Access
- RGPIO Interface to FPGA

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Description
B66_T1	in	83	FPGA / dp_aux_data_out
B66_T2	in	82	FPGA / dp_aux_data_oe_n
B66_T3	out	81	FPGA / dp_aux_data_in
B67_T1	out	78	FPGA / dp_hot_plug_detect
B67_T2	in	76	FPGA / <i>currently_not_used</i>
B67_T3	in	77	FPGA / / <i>currently_not_used</i>
C_TCK	in	131	/ <i>currently_not_used</i>
C_TDO	out	137	/ <i>currently_not_used</i>
C_TDO1/TDI	in	136	/ <i>currently_not_used</i>
C_TMS	in	130	/ <i>currently_not_used</i>
CAN_FAULT		26	/ <i>currently_not_used</i>
CAN_RX		24	/ <i>currently_not_used</i>
CAN_S		25	/ <i>currently_not_used</i>
CAN_TX		23	/ <i>currently_not_used</i>
DP_AUX_DE	out	133	Display Port
DP_AUX_RX	in	132	Display Port
DP_AUX_TX	out	138	Display Port
DP_TX_HPD	in	139	Display Port
ERR_OUT	in	98	FPGA PS / <i>currently_not_used</i>
ERR_STATUS	in	97	FPGA PS / <i>currently_not_used</i>
ETH_RST	out	93	Reset
F1_EN	out	65	FAN
F1PWM	out	68	FAN
F1SENSE	in	67	FAN
F2_EN	out	61	FAN
F2PWM	out	110	FAN
F2SENSE	in	109	FAN
F3_EN	out	62	FAN
F3PWM	out	28	FAN
F3SENSE	in	27	FAN
I2C_RST	out	94	Reset_n for I2C Switches
JTAGENB	--	120	enable JTAG access to CPLD (one CPLD)
LED_1A	out	119	Yellow LED
LED_2A	out	122	Green/Orange LEDs
LED_2B	out	121	Green/Orange LEDs
LED1	out	22	Green LED D13
LED2	out	21	Green LED D14

LED3	out	20	Green LED D15
LED4	out	19	Green LED D16
MEM_SCL	in	35	I2C 100kHz supported
MEM_SDA	inout	34	I2C
MIO24		95	Zynq MIO / currently_not_used
MIO25		96	Zynq MIO / currently_not_used
MIO26		42	Zynq MIO / currently_not_used
MIO27		57	Zynq MIO / currently_not_used
MIO28		44	Zynq MIO / currently_not_used
MIO29		59	Zynq MIO / currently_not_used
MIO30	in	48	Zynq MIO / PCIe reset_n
MIO31		54	Zynq MIO / currently_not_used
MIO32		60	Zynq MIO / currently_not_used
MIO33		41	Zynq MIO / currently_not_used
MIO34		58	Zynq MIO / currently_not_used
MIO35		43	Zynq MIO / currently_not_used
MIO36		50	Zynq MIO / currently_not_used
MIO37		55	Zynq MIO / currently_not_used
MIO40		56	Zynq MIO / currently_not_used
MIO41		52	Zynq MIO / currently_not_used
MIO42	out	47	Zynq MIO / Zynq UART RX
MIO43	in	49	Zynq MIO / Zynq UART TX
MIO44		45	Zynq MIO / currently_not_used
PHY_CLK125M	in	85	Ethernet
PHY_LED0	in	92	Ethernet
PHY_LED1	in	91	Ethernet
PHY_LED2	in	86	Ethernet
PLL_RST	out	73	Reset
PLL_SEL0	out	74	PLL
PLL_SEL1	out	75	PLL
SC_IO0	in	107	Master CPLD / Reset
SC_IO1		106	Master CPLD / currently_not_used
SC_IO2		105	Master CPLD / currently_not_used
SC_IO3	out	104	Master CPLD / Slave RGPIO TX data
SC_IO4	in	100	Master CPLD / Slave RGPIO RX DATA
SC_IO5	in	99	Master CPLD / Slave RGPIO RX CLK
SC1_IO_SB		112	Master CPLD / currently_not_used
SC2_IO_SB		111	Master CPLD / currently_not_used
SD_EN	out	38	SD Power enable
SD_WP		39	SD Write Protection / currently_not_used

SFP_LED1	out	142	SFP Red LED D2
SFP_LED2	out	143	SFP Green LED D4
SFP_LED3	out	141	SFP Red LED D3
SFP_LED4	out	140	SFP Green LED D5
SFP0_LOS		113	SFP / <i>currently_not_used</i>
SFP0_TX_DIS	out	115	SFP
SFP1_LOS		114	SFP / <i>currently_not_used</i>
SFP1_TX_DIS	out	117	SFP
SFP2_LOS		6	SFP / <i>currently_not_used</i>
SFP2_TX_DIS	out	10	SFP
SSD1_LED	in	128	SSD
SSD1_PERSTN	out	126	SSD / Reset_n M2 PCIe
SSD1_SLEEP	in	127	SSD
SSD1_WAKE	out	125	SSD
U_SW1	in	14	Switch S4 / <i>currently_not_used</i>
U_SW2	in	13	Switch S4 / <i>currently_not_used</i>
U_SW3	in	12	Switch S4 / <i>currently_not_used</i>
U_SW4	in	11	Switch S4 / <i>currently_not_used</i>
USB0_RST	out	84	USB / Reset
USBH_MODE0	out	69	USB
USBH_MODE1	out	71	USB
USBH_RST	out	70	USB / Reset
USR_BUT1	in	9	Button
XMOD1_A	out	1	XMOD UART RX
XMOD1_B	in	3	XMOD UART TX
XMOD1_E	out	2	XMOD LED
XMOD1_G	in	4	XMOD Button / Debug Reset

Functional Description

JTAG

Used only for CPLD Firmwareupdate. Second chip in JTAG chain when switch S3:2 is ON.

RESET

Name	Description
SSD1_PERSTn	SC_IO0
ETH_RST	Slow Reset from SC_IO0
USB0_RST	Slow Reset from SC_IO0

USBH_RST	Slow Reset from SC_IO0
PLL_RST	Slow Reset from SC_IO0

LEDs

LED	Value	Description
XMOD1_E	Counter Bit or XMOD1_G	
LED1_1A	not PHY_LED1	Yellow LED is PHY RX Indicator (with default PHY settings)
LED_2A	not PHY_LED0	Green LED is PHY LINK Indicator (with default PHY settings)
LED_2B	0	Stub to use only green from dual Green/Orange LED
LED1	DP_TX_HPD	DisplayPort Hotplug Detection
LED2	hub_rst_n	USB hub reset indicator
LED3	SSD1_LED	LED output from M2 slot
LED4	F1_SENSE	
SFP_LED1	0	
SFP_LED2	0	
SFP_LED3	0	
SFP_LED4	0	

UART

Output	Input
MIO42	XMOD1_B
XMOD1_A	MIO43

Display Port

Output	Input
DP_AUX_TX	B66_T1
DP_AUX_DE	not B66_T2
B66_T3	DP_AUX_RX
B67_T1	DP_TX_HPD

SD

SD_EN is "0". Enable power for SD slot.

SFP

Transmit for all SFP is enabled.

USB

USB Mode pins constant "11" (default boot mode).

SSD

SSD1_WAKE is "0".

I2C RAM

I2C Baseaddress: 0x74. I2C with 8Bit Register Address with 8Bit Data. I2C CLK currently 100 MHz supported.

Write access

Register Address	Name	Description
0	FAN CTRL	Enable FAN, Bit 0-2 Fan1 to Fan2, Default all 1
1	FAN1 PWM	FAN1 PWM (0%-100%, Default 30%)
2	FAN2 PWM	FAN2 PWM (0%-100%, Default 30%)
3	FAN3 PWM	FAN3 PWM (0%-100%, Default 30%)

Read access

Register Address	Name	Description
0	FAN CTRL	FAN Control register
1	FAN1 RPS	FAN1 Revolutions per second
2	FAN2 RPS	FAN2 Revolutions per second
3	FAN3 RPS	FAN3 Revolutions per second

FANs

[See I2C RAM.](#)

PLL

PLL Selection pins constant "00".

RGPIO

RGPIO is a 32Bit Remote GPIO Interface to talk with FPGA over 3 lanes.

RGPIO Pin to FPGA	Value
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0-2	FAN Enable 1..3
3	unused
4	Slow Reset
5	Slow HUB Reset
6	unused
7	Counter Bit 32
8-23	unused
24-27	reserved
28-31	interface detection

RGPIO Pin from FPGA	Value
0-23	unused
24-27	reserved
28-31	interface detection

Appx. A: Change History

Revision Changes

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV01	REV01	<div>Error render ing macro 'page- info'</div> <div>Ambig uous metho</div>	document style update

**Error rendering macro
'page-info'**

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class com.atlassian.
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Appx. B: Legal Notices

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REACH, RoHS and WEEE

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Error rendering macro 'page-info'

Ambiguous method overloading for method `jdk.proxy279.$Proxy4022#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`