TEBB0714 TRM

Download PDF version of this document.

Table of Contents

- Overview
  - Key Features
  - Block Diagram
  - Main Components
  - Initial Delivery State
- Signals, Interfaces and Pins
  - B2B Connector
  - On-board Pin Header
  - SFP+ Connector
  - Ultra Small SMT Coaxial Connectors
  - JTAG Interface
    - XMOD FTDI JTAG-Adapter Header JX1
    - JTAG/UART Header J3
  - UART Interface
  - QSPI Interface
- On-board Peripherals
  - On-board LEDs
  - VCCIO Selection Jumper
- Power and Power-On Sequence
  - Power Consumption
  - Power Supply
  - Power Distribution Dependencies
  - Power Rails
- Board to Board Connector
  - Connector Mechanical Ratings
  - Manufacturer Documentation
- Technical Specifications
  - Absolute Maximum Ratings
  - Recommended Operating Conditions
  - Operating Temperature Ranges
  - Physical Dimensions
- Revision History
  - Hardware Revision History
  - Document Change History
- Disclaimer
  - Data Privacy
  - Document Warranty
  - Limitation of Liability
  - Copyright Notice
  - Technology Licenses
  - Environmental Protection
  - REACH, RoHS and WEEE

Overview

The Trenz Electronic TEBB0714 is a Carrier Board for testing, evaluation and development purposes, especially for the Multi Gigabit Transceiver units of the TE0714 module. Although this base-board is dedicated to the TE0714 module, it is also compatible with other Trenz Electronic 4 x 3 cm SoMs. See page "4 x 3 cm carriers" to get information about the SoMs supported by the TEBB0714 Carrier Board.

This base-board provides also through hole pads for pin headers to get access to the PL I/O-bank pins and further interfaces of the mounted TE 4 x 3 SoM.

Key Features

- SFP+ connector (Enhanced small form-factor pluggable), support data transmission rates up to 10 Gbit/s
- 4 Hirose Ultra small SMT coaxial connectors, support data transmission rates up to 6 Gbit/s

- TE 4 x 3 cm SoM programmable by XMOD header (JX1)
- 2 x user LEDs routed to I/O-pins of the SoM
- Solder pads J17 and J20 for optional pin headers for access to SoM's PL I/O-bank pins, usable as LVDS pairs
- Solder pads J3 and J4 for optional pin headers for access to further interfaces and I/O's of the SoM

Additional assembly options are available for cost or performance optimization upon request.

Block Diagram

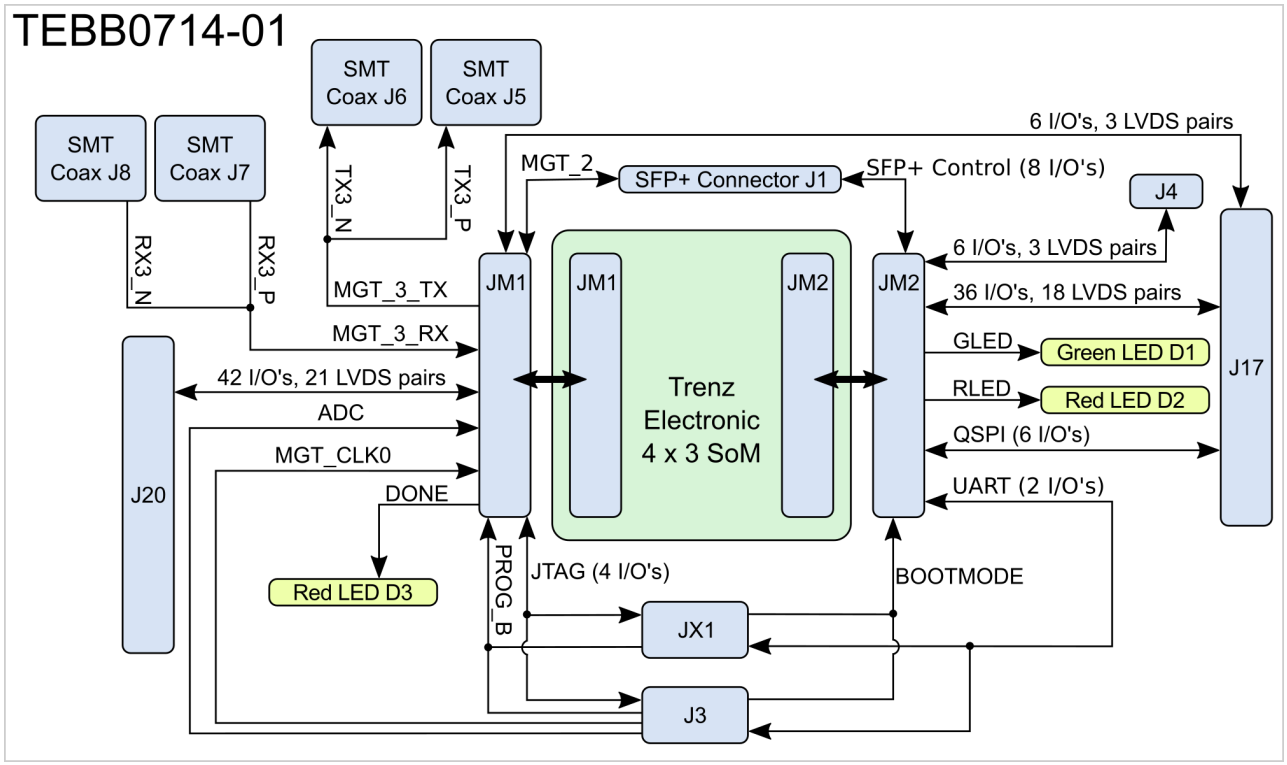

Figure 1: TEBB0714-01 Block Diagram.

Main Components

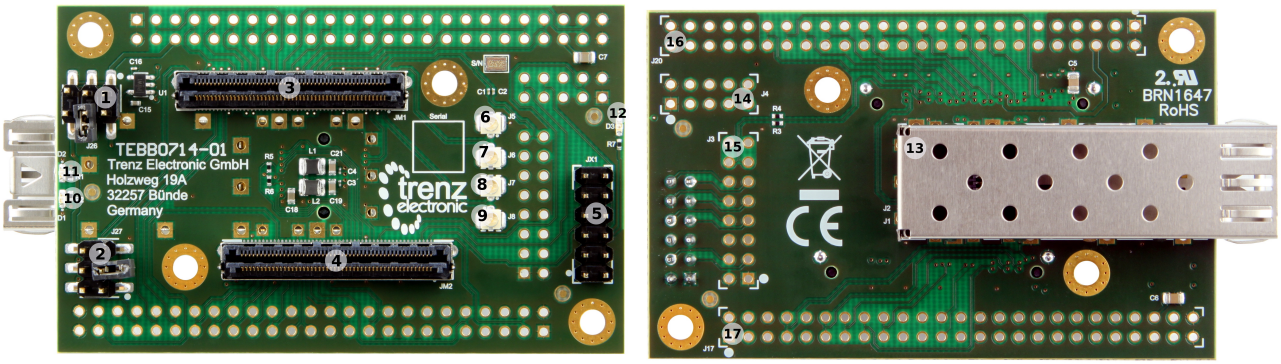

Figure 2: TEBB0714-01 Carrier Board.

1. 6-pin header J26 for selecting PL-bank I/O voltage
2. 6-pin header J27 for selecting XMOD/JTAG VCCIO
3. Samtec Razor Beam™ LSHM-150 B2B connector, JM1
4. Samtec Razor Beam™ LSHM-150 B2B connector, JM2
5. XMOD header, JX1
6. Ultra small SMT coaxial connector, J5
7. Ultra small SMT coaxial connector, J6
8. Ultra small SMT coaxial connector, J7
9. Ultra small SMT coaxial connector, J8
10. User LED D1 (green)
11. User LED D2 (red)
12. LED D3 (red) indicating FPGA's 'Programming DONE'-signal
13. SFP+ Connector, J1
14. 10-pin header solder pads J4 for access to SoM's PL I/O-banks (LVDS pairs possible)
15. 16-pin header solder pads J3, JTAG/UART header with ADC and MGT clock input
16. 50-pin header solder pads J20 for access to SoM's PL I/O-banks (LVDS pairs possible)
17. 50-pin header solder pads J17 for access to SoM's PL I/O-banks (LVDS pairs possible)

Initial Delivery State

Board is shipped in following configuration:

- VCCIO voltage selection jumpers are all set to 1.8 V.
- Pin headers (not soldered to the board, but included in the package as separate component)

Different delivery configurations are available upon request.

Signals, Interfaces and Pins

B2B Connector

With the TEBB0714 Carrier Board's Board-to-Board Connectors (B2B) the MIO- and PL I/O-bank's pins and further interfaces of the mounted SoM can be accessed. A large quantity of these I/O's are also usable as differential pairs. The connectors provide also VCCIO voltages to operate the I/O's properly.

Following table gives a summary of the available I/O's, interfaces and differential pairs of the B2B connectors JB1, JB2 and JB3:

B2B Connector	Interfaces	Count of I/O's	Notes
JM1	User I/O	54 single ended or 27 differential	-
	MGT lanes	4 differential pairs, 2 lanes	-
	MGT reference clock input	1	-
	JTAG	4	-
	SoM control signals	2	'PROG_B', 'DONE'
	ADC interface	1 differential pair	-
JM2	User I/O	36 single ended or 18 differential	-
	SFP+ Interface control signals	8	-
	QSPI interface	6	-
	UART interface	2	-
	User LEDs	2	Red, Green
	SoM control signals	1	'BOOTMODE'

Table 1: General overview of PL I/O signals and SoM's interfaces connected to the B2B connectors.

On-board Pin Header

The TEBB0714 Carrier Board has 4 footprints as soldering pads to mount 2.54mm grid size pin headers to get access the PL I/O-bank's pins and further interfaces of the mounted SoM. With these pin headers, SoM's PL-I/O's are available to the user, a large quantity of these I/O's are also usable as differential pairs.

Following table gives a summary of the pin-assignment, available interfaces and functional I/O's of the pin headers:

On-board Pin Header	Control Signals and Interfaces	Count of I/O's	Notes
J17	User I/O	36 single ended or 18 differential	-
	QSPI interface	6	-
J20	User I/O	42 single ended or 21 differential	-
J3	JTAG	4	-
	UART	2	-
	SoM control signals	2	'BOOTMODE', 'PROG_B'
	ADC	1 differential pair	-
	MGT reference clock input	1 differential pair	AC decoupled on-board (100 nF capacitor)
JX1	JTAG	4	-
	UART	2	-
	SoM control signals	2	'BOOTMODE', 'PROG_B'
J4	User I/O	6 single ended or 3 differential	3.3V, 3.3V_OUT voltage level available on header

Table 2: General overview of PL I/O signals, SoM's interfaces and control signals connected to the on-board connectors.

SFP+ Connector

The TEBB0714 Carrier Board is equipped with one SFP+ connector J1 (board-rev. 01: Molex 74441-0001). The connector is embedded into a SFP cage J2 (board-rev. 01: Molex 74737-0009).

The differential RX/TX data lanes are connected to B2B connector JM1, the control-lines are connected to B2B connector JM2.

Following table describes the pin-assignment of the SFP+ connector in detail:

SFP+ pin	Pin Schematic Name	B2B	FPGA Direction	Description	Note
Transmit Data + (pin 18)	MGT_TX2_P	JM1-14	Output	SFP+ transmit data differential pair	-
Transmit Data - (pin 19)	MGT_TX2_N	JM2-16	Output		-
Receive Data + (pin 13)	MGT_RX2_P	JM1-7	Input	SFP+ receive data differential pair	-
Receive Data - (pin 12)	MGT_RX2_N	JM1-9	Input		-
Receive Fault (pin 2)	SFP0_TX_FAULT	JM2-42	Input	Fault / Normal Operation	High active logic
Receive disable (pin 3)	SFP0_TX_DIS	JM2-44	Output	SFP Enabled / Disabled	Low active logic
MOD-DEF2 (pin 4)	SFP0_SDA	JM2-46	BiDir	2-wire Serial Interface data	3.3V pull-up on-board
MOD-DEF1 (pin 5)	SFP0_SCL	JM2-48	Output	2-wire Serial Interface clock	3.3V pull-up on-board
MOD-DEF0 (pin 6)	SFP0_M-DEF0	JM2-40	Input	Module present / not present	Low active logic
RS0 (pin 7)	SFP0_RS0	JM2-38	Output	Full RX bandwidth	Low active logic
LOS (pin 8)	SFP0_LOS	JM2-34	Input	Loss of receiver signal	High active logic
RS1 (pin 9)	SFP0_RS1	JM2-32	Output	Reduced RX bandwidth	Low active logic

Table 3: SFP+ connector pin-assignment.

Ultra Small SMT Coaxial Connectors

4 HIROSE Ultra Small Surface Mount Coaxial Connectors (up to 6 Gbit/s transmission rate) are present on the Carrier Board available for access to one MGT lane of the SoM. The connectors have the manufacturer designation 'U.FL-R-SMT-1', mating hight: 2.4 mm.

Each conductor of the RX and TX differential pair is routed to one coaxial connector:

Connector Designator	Connected to	B2B Connector
J5	MGT_TX3_P	JM1-8
J6	MGT_TX3_N	JM1-10
J7	MGT_RX3_P	JM1-1
J8	MGT_RX3_N	JM1-3

Table 4: Pin-assignment of the coaxial connectors.

JTAG Interface

JTAG access to the mounted SoM is provided through B2B connector JB2 and is also routed to the XMOD header JX1 and pin header J3. With the TE0790 XMOD USB2.0 to JTAG adapter, the device of the mounted SoM can be programed via USB2.0 interface.

JTAG Signal	B2B Connector Pin	XMOD Header JX1	Pin Header J3	Note
TCK	JM1-90	JX1-4	J3-4	-
TDI	JM1-86	JX1-10	J3-10	-
TDO	JM1-88	JX1-8	J3-8	-
TMS	JM1-92	JX1-12	J3-12	-

Table 5: JTAG interface signals.

XMOD FTDI JTAG-Adapter Header JX1

The JTAG interface of the mounted SoM can be accessed via XMOD header JX1, so in use with the XMOD-FT2232H adapter-board TE0790 the mounted SoM can be programmed via USB2.0 interface. The TE0790 board provides also an UART interface to the SoM's Zynq device which can be accessed by the USB2.0 interface of the adapter-board while the signals between these serial interfaces will be converted.

Following table describes the signals and interfaces of the XMOD header JX1:

Pin Schematic Name	XMOD Header JX1 Pin	B2B	Note
TCK	C (pin 4)	JM1-90	-
TDO	D (pin 8)	JM1-88	-
TDI	F (pin 10)	JM1-86	-
TMS	H (pin 12)	JM1-92	-
B14_L25	A (pin 3)	JM2-97	UART (output from module to XMOD Programmer)
B14_L0	B (pin 7)	JM2-99	UART (input to module from XMOD Programmer)
BOOTMODE	E (pin 9)	JM2-100	-
PROG_B	G (pin 11)	JM1-94	-

Table 6: XMOD header JX1 signals and connections.

When using XMOD FTDI JTAG Adapter TE0790, the adapter-board's VCC and VCCIO will be sourced by the Carrier Board's and module's 3.3V supply voltage. Set the XMOD DIP-switch with the setting:

XMOD DIP-switches	Position
Switch 1	ON
Switch 2	OFF
Switch 3	OFF
Switch 4	OFF

Table 7: XMOD adapter board DIP-switch positions for voltage configuration.

The I/O-voltage of the XMOD adapter board with the schematic name 'V_CFG' and pin-name 'VIO' (pin 6) on XMOD header JX1 can be selected via Jumper J27:

V_CFG Value	Jumper J27 Setting	Note
1.8V	pins 1-2 connected	Module's output voltage.
V_CFG0*	pins 3-4 connected	Internal module VCCIO: 3.3V or 1.8V (Settable by 0-Ohm-Resistor on TE0714 module).
3.3V_OUT	pins 5-6 connected	Module's output voltage.

*Default setting, do not changed, if V_CFG0 Bank power is sourced by module itself.

Table 8: Setting of reference I/O-voltage XMOD header.

Use Xilinx compatible TE0790 adapter board (designation TE-0790-xx with out 'L') to program the Xilinx Zynq devices.

The TE0790 adapter board's CPLD have to be configured with the **Standard** variant of the firmware. Refer to the TE0790 Resources Site for further information and firmware download.

JTAG/UART Header J3

As alternative to the XMOD header JX1, on the Carrier Board pin header J3 is present with 4 additional pins as differential pairs to supply the mounted SoM with an external MGT reference clock signal and to provide differential analog signal input:

Pin Schematic Name	Header J3 Pin	B2B	Note
TCK	4	JM1-90	-
TDO	8	JM1-88	-
TDI	10	JM1-86	-
TMS	12	JM1-92	-
B14_L25	3	JM2-97	UART (output from module)
B14_L0	7	JM2-99	UART (input to module)
BOOTMODE	9	JM2-100	-
PROG_B	11	JM1-94	-

XADC_P	13	JM1-25	Analog input differential pair
XADC_N	14	JM1-27	
CLK0_N	15	JM1-4	AC decoupled on-board (100 nF capacitor)
CLK0_P	16	JM1-2	

Table 9: JTAG/UART header J3 signals and connections.

UART Interface

UART interface is available on B2B connector JM2. With the TE0790 XMOD USB2.0 adapter, the UART signals can be converted to USB2.0 interface signals:

UART Signal Schematic Name	B2B	XMOD Header JX1	Pin Header J3	Note
B14_L0	JM2-99	JX1-7	J3-7	UART (input to module)
B14_L25	JM2-97	JX1-3	J3-3	UART (output from module)

Table 10: UART interface signals.

QSPI Interface

The QSPI interface (if available) of the mounted SoM is routed to the pin header J17. The reference I/O-voltage of the module have to be noticed when using this interface.

SD IO Signal Schematic Name	B2B	Pin Header J17	Note
SPI-DQO	JM2-68	J17-24	QSPI data
SPI-DQ1	JM2-71	J17-27	QSPI data
SPI-DQ2	JM2-73	J17-28	QSPI data
SPI-DQ3	JM2-70	J17-23	QSPI data
SPI-CLK	JM2-67	J17-26	QSPI clock
SPI_CS	JM2-69	J17-25	QSPI chip select

Table 11: QSPI interface signals.

On-board Peripherals

On-board LEDs

The on-board LEDs are available to the user and can be used to indicate system status and activities:

LED Designator	Color	Pin Schematic Name	B2B Connector	Indicating
D1	green	GLED	JM2-26	Available to user.
D2	red	RLED	JM2-24	Available to user.
D3	red	DONE	JM1-96	FPGA module programmed properly.

Figure 12: On-board LEDs

VCCIO Selection Jumper

On the TEBB0714 Carrier Board the PL-bank I/O voltage (schematic name 'VCCIO34') can be selected by the jumper J26.

VCCIO34 Value	Jumper J26 Setting	Note
1.8V	pins 1-2 connected	Module's output voltage.
2.5V	pins 3-4 connected	Voltage generated by on-board LDO U1.
3.3V_OUT	pins 5-6 connected	Module's output voltage.

Table 13: Base-board PL-bank I/O voltage setting.

Take care of the VCCO voltage ranges of the particular PL IO-banks (HR, HP) of the mounted SoM, otherwise damages may occur to the FPGA. Therefore, refer to the TRM of the mounted SoM to get the specific information of the voltage ranges.

It is recommended to set and measure the PL IO-bank supply-voltages before mounting of TE 4 x 3 module to avoid failures and damages to the functionality of the mounted SoM.

Power and Power-On Sequence

Power Consumption

The maximum power consumption of the Carrier Board depends mainly on the mounted SoM's FPGA design running on the Zynq device.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input	Typical Current
3.3V	TBD*

Table 14: Typical power consumption.

* TBD - To Be Determined soon with reference design setup.

Power supply with minimum current capability of 3A for system startup is recommended.

To avoid any damage to the module, check for stabilized on-board voltages and VCCIO's before put voltages on PL I/O-banks and interfaces. All I/Os should be tri-stated during power-on sequence.

Power Supply

Power supply with minimum current capability of 3A at 3.3V for system startup is recommended.

The on-board voltages of the carrier board will be powered up with an external power-supply with nominal voltage of 3.3V.

The external power-supply can be connected to the board by the following pins:

Connector	3.3V pin	GND pin
JX1	JX1-5, JX1-6,	JX1-1, JX1-2
J3	J3-5, J3-6	J3-1, J3-2

J4	J4-5	J4-1, J4-2
J20	J20-5, J20-46	J20-1 , J20-2 , J20-49 , J20-50
J17	J17-5, J17-46	J17-1 , J17-2 , J17-49 , J17-50

Table 15: Connector pins capable for external 3.3V power supply

Power Distribution Dependencies

The PL-bank I/O voltages 1.8V, 2.5V and 3.3V will be available after the mounted SoM's 3.3V voltage level has reached stable state on B2B-connector pins JM1-83 and JM2-54, meaning that all on-module voltages have become stable and module is properly powered up.

Following diagram shows the distribution of the external input voltage of nominal 3.3V to the components:

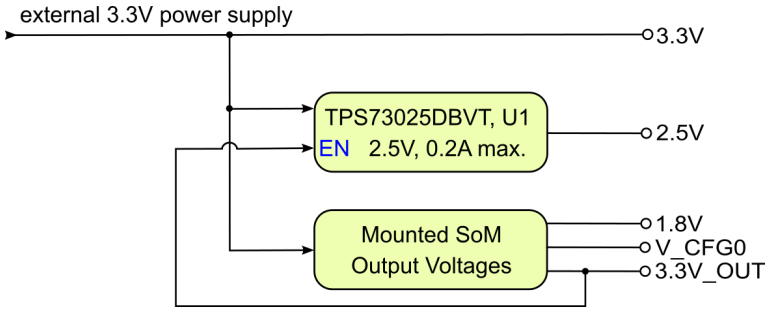

Figure 3: Board power distribution diagram.

Power Rails

The voltage direction of the power rails is from board and on-board connectors' view:

Module Connector (B2B) Designator	VCC / VCCIO	Direction	Pins	Notes
JM1	3.3V	Out	97, 99	3.3V module supply voltage
	3.3V_OUT	In	83	3.3V module output voltage
	VCCIO34	Out	61	PL IO-bank VCCIO
JM2	1.8V	In	18	1.8V module output voltage
	3.3V_OUT	Out	54	3.3V module output voltage
	V_CFG0	In/out	53	Direction depends on solder option of the modul: Internal module VCCIO 3.3V or 1.8V or source from carrier is possible

Table 16: Power pin description of B2B module connector.

On-board Pin Header Designator	VCC / VCCIO	Direction	Pins	Notes
J17	3.3V	In / Out	5, 46	3.3V external supply voltage
	V_CFG	Out / int	6, 45	direction depends on jumper 27 settings and module solder option
J20	3.3V	In / Out	5, 46	3.3V external supply voltage

	VCCIO34	In / Out	6, 45	PL IO-bank VCCIO, depends on Jumper settings

Table 17: Power Pin description of on-board connector.

Jumper / Header Designator	VCC / VCCIO	Direction	Pins	Notes
J26	VCCIO34	In	1, 3, 5	-
	1.8V	Out	2	-
	2.5V	Out	4	-
	3.3V_OUT	Out	6	-
J27	V_CFG	In / Out	1, 3, 5	direction depends on jumper 27 settings and module solder option
	1.8V	Out	2	-
	V_CFG0	Out	4	-
	3.3V_OUT	Out	6	-

Table 18: Power Pin description of VCCIO selection jumper pin header.

JTAG/UART Header Designator	VCC / VCCIO	Direction	Pins	Notes
JX1 (XMOD)	3.3V	Out	5	Connected to 3.3V external supply voltage
	VIO	Out	6	Connected to 'V_CFG', depends on jumper 27 settings
J3	3.3V	Out	5	Connected to 3.3V external supply voltage
	V_CFG	Out	6	direction depends on jumper 27 settings and module solder option

Table 19: Power pin description of XMOD/JTAG Connector.

Board to Board Connector

Board to board connectors are hermaphroditic. Odd pin numbers are connected to even pin numbers on the mating connector and vice versa.

The Trenz Electronic modules use 100-pin REF-189016-02 and 60-pin REF-189017-02 connectors which are compatible with Samtec Razor Beam LSHM type connectors (see table below). When using the same type of connectors on baseboard, mating height will be 8mm. Other mating heights are possible by using connectors with a different height.

Baseboard Connector	Compatible Connector	Number of Pins	Mating height
REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	100 (2 x 50)	6.5 mm
LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	100 (2 x 50)	7.0 mm
REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	100 (2 x 50)	8.0 mm
LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	100 (2 x 50)	10.0mm
REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	60 (2 x 30)	6.5 mm
LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	60 (2 x 30)	7.0 mm
REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	60 (2 x 30)	8.0 mm
LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	60 (2 x 30)	10.0mm

Modules can be manufactured using different type of connectors upon request.

The LSHM connector speed rating depends on the stacking height:

Stacking Height	Speed Rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.9 GHz / 14 Gbps

Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 3 hours 3 axis

Manufacturer Documentation

File	Modified
PDF File hsc-report_lshm-lshm-05mm_web.pdf	11 01, 2017 by Jan Kumann
PDF File lshm_dv.pdf	11 01, 2017 by Jan Kumann
PDF File LSHM-1XX-XX.X-X-DV-A-X-X-TR-FOOTPRINT(1).pdf	11 01, 2017 by Jan Kumann
PDF File LSHM-1XX-XX.X-XX-DV-A-X-X-TR-MKT.pdf	11 01, 2017 by Jan Kumann
PDF File REF-189016-01.pdf	11 01, 2017 by Jan Kumann
PDF File REF-189016-02.pdf	11 01, 2017 by Jan Kumann
PDF File REF-189017-01.pdf	11 01, 2017 by Jan Kumann
PDF File REF-189017-02.pdf	11 01, 2017 by Jan Kumann
PDF File TC0923--2523_report_Rev_2_qua.pdf	11 01, 2017 by Jan Kumann
PDF File tc0929--2611_qua(1).pdf	11 01, 2017 by Jan Kumann

Download All

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Vin supply voltage	3.135	3.465	V	3.3V supply-voltage ± 5%
Storage Temperature	-40	85	°C	WL-SMCW SMD chip LED data sheet

Table 20: Absolute maximum ratings.

Recommended Operating Conditions

Parameter	Min	Max	Units	Notes
Vin supply voltage	3.135	3.465	V	-
Operating temperature	-40	+85	°C	Molex 74441-0001 Product Specification

Table 21: Recommended operating conditions.

Operating Temperature Ranges

Industrial grade: -40°C to +85°C.

The Carrier Board is operable within industrial grade temperature range.

Please check the operating temperature range of the mounted SoM, which determine the relevant operating temperature range of the overall system.

Physical Dimensions

- Board size: PCB 46mm × 75mm. Notice that some parts the are hanging slightly over the edge of the PCB like the the SFP+ connector, which determine the total physical dimensions of the carrier board. Please download the assembly diagram for exact numbers.
- Mating height of the module with standard connectors: 8mm
- PCB thickness: ca. 1.65mm
- Highest part on the PCB is the SFP+ connector, which has an approximately 11.3 mm overall hight. Please download the step model for exact numbers.

The dimensions are given in mm and mil (milli inch).

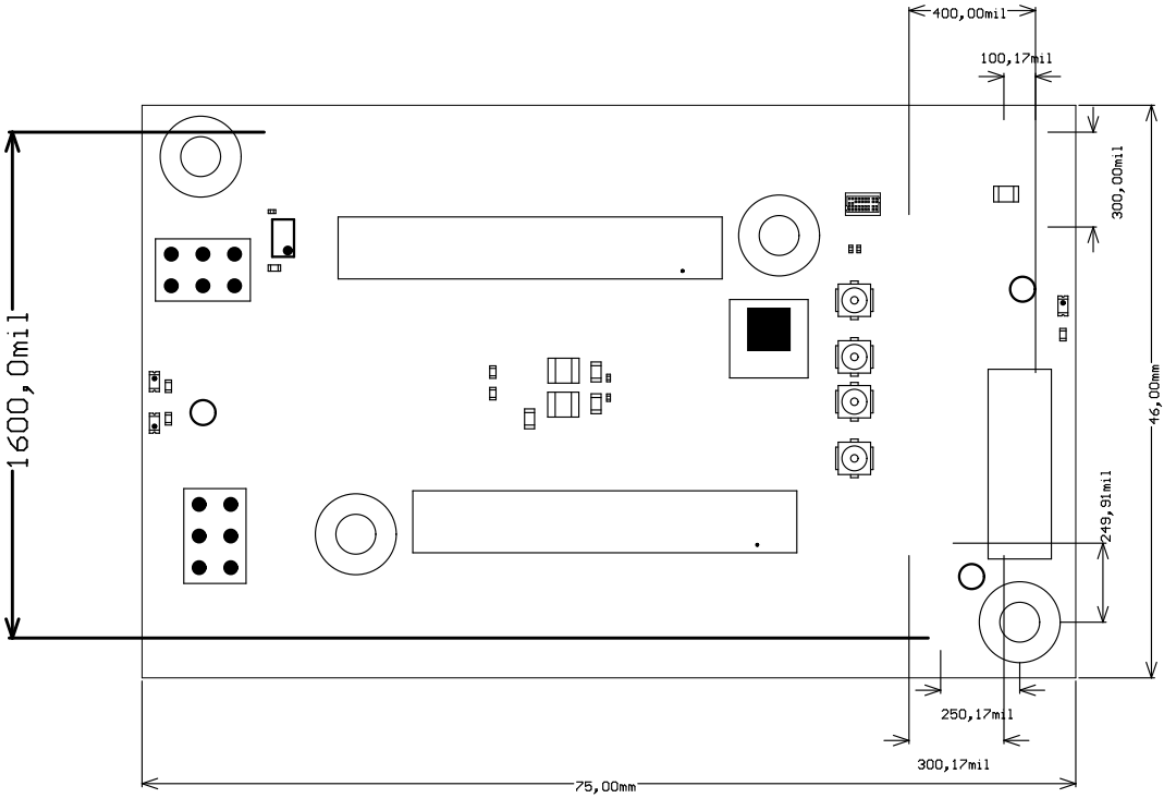

Figure 4: Board physical dimensions drawing.

Revision History

Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
-	01	• First Production Release	-	TEBB0714-01

Table 22: Module hardware revision history.

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

Figure 5: Board hardware revision number.

Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	Unknown macro: 'metadata'	Ali Naseri, Jan Kumann	• First TRM release

Table 23: Document change history.

Disclaimer

Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

02 Sept 2017