TEBF0808 TRM

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Overview

The Trenz Electronic TEBF0808 carrier board is a baseboard for the Xilinx Zynq Ultrascale+ MPSoC modules TE0808 and TE0803, which exposes the module's B2B connector pins to accessible connectors and provides a whole range of on-board components to test and evaluate the Zynq Ultrascale+ SoMs and for developing purposes. The carrier board has a Mini-ITX form factor making it capable to be fitted into a PC enclosure. On the PC enclosure's rear and front panel, MGT interfaces and connectors are accessible, for the front panel elements there are also Intel-PC compatible headers available.

Key Features

- Mini-ITX form factor, PC enclosure compatible
- ATX-24 power supply connector
- Optional 12V standard power plug
- Headers
    - Intel 10-pin HDA Audio
    - Intel 9-pin Power-/Reset-Button, Power-/HD-LED
    - PC-BEEPER
- On-board Power- / Reset-Switches
- 2x Configuration 4-bit DIP-switches
- 2x Optional 4-wire PWM fan connectors
- PCIe Slot - one PCIe lane (16 lane connector)
- CAN FD Transceiver (10 Pin IDC connector and 6-pin header)
- 4x On-board configuration EEPROMs (1x Microchip 24LC128-I/ST, 3x Microchip 24AA025E48T-I/OT)
- Dual SFP+ Connector (2x1 Cage)
- 1x DisplayPort (single lane)
- 1x SATA Connector
- 2x USB3.0 A Connector (Superspeed Host Port (Highspeed at USB2.0))
- 1x USB3.0 on-board connector with two ports
- FMC HPC Slot (FMC_VADJ max. VCCIO)
- FMC Fan
- Gigabit Ethernet RGMII PHY with RJ45 MagJack
- All carrier board peripherals' I²C interfaces muxed to MPSoC's I²C interface
- Quad programmable PLL clock generator SI5338A
- 2x SMA coaxial connectors for clock signals
- MicroSD- / MMC-Card Socket (bootable)
- 32 Gbit (4 GByte) on-board eMMC flash (8 banks a 4 Gbit)
- 2x System Controller CPLDs Lattice MachXO2 1200 HC
- 1x Samtec FireFly (4 GT lanes bidirectional)
- 1x Samtec FireFly connector for reverse loopback
- 2x JTAG/UART header ('XMOD FTDI JTAG Adapter'-compatible) for programming MPSoC and SC CPLDs
- 20-pin ARM JTAG Connector (PS JTAG0)
- 3x PMOD connector (GPIO's and I²C interface to SC CPLDs and MPSoC module)
- On-board DC-DC PowerSoCs

Additional assembly options are available for cost or performance optimization upon request.

Block Diagram

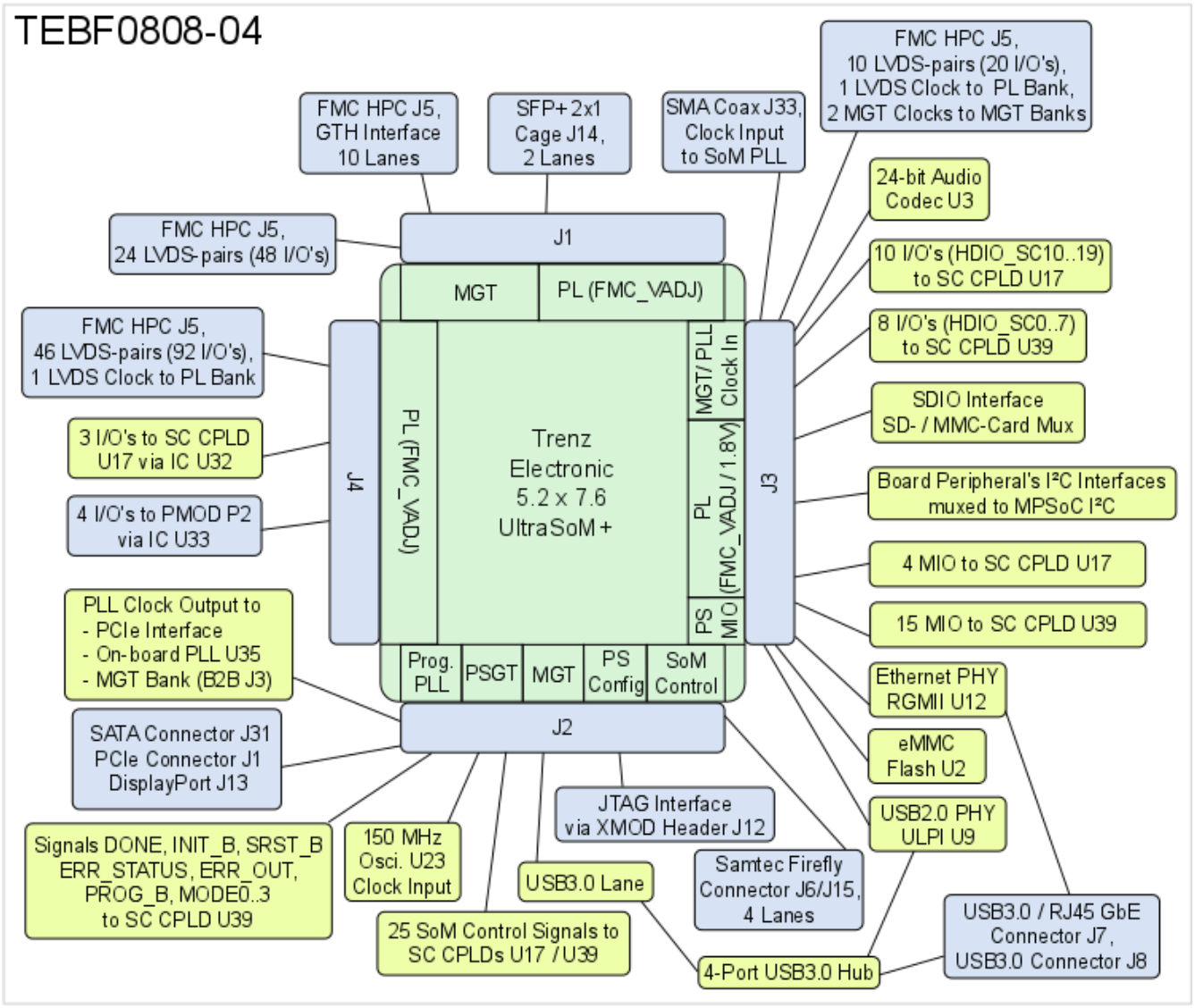

Figure 1: TEBF0808-04 Block Diagram

Block Diagram description of depicted on-board peripherals

On-board Peripheral	B2B	MPSoC Unit / SoM peripheral	Description	TRM Section
FMC HPC J5, 24 LVDS pairs (48 I /O's)	J1	PL Bank (FMC_VADJ)	PL I/O-bank pins, differential pairs	FMC HPC Connector
FMC HPC J5, GTH Interface	J1	MGT Bank	10 MGT Lanes	FMC HPC Connector
SFP+ 2x1 Cage J14	J1	MGT Bank	2 MGT Lanes to dual SFP+ Connector	MGT Interfaces SFP+ and FireFly
SMA Coax J33	J1	On-module PLL	SMA Coaxial Connector to on-module PLL Clock Input pin	Programmable PLL Clock Generator

FMC HPC J5 ▪ 10 LVDS pairs (20 I/O's) ▪ 1 LVDS Clock to PL Bank ▪ 2 MGT Clocks to MGT Banks	J2	PL Bank (FMC_VADJ) MGT Bank	PL I/O-bank pins, differential pairs 1 clock capable PL bank pin-pair 2 MGT clock input pin-pairs	FMC HPC Connector Programmable PLL Clock Generator
24-bit Audio Codec U3	J3	PL Bank (1.8 V)	PL I/O-bank pins to on-board 24-bit Audio Codec	Intel-PC Compatible Headers and FAN Connectors 24-bit Audio Codec
10 I/O's to SC CPLD U17	J3	PL Bank (1.8 V)	PL I/O-bank pins to on-board System Controller CPLD U17	System Controller CPLDs
8 I/O's to SC CPLD U39	J3	PL Bank (1.8 V)	PL I/O-bank pins to on-board System Controller CPLD U39	System Controller CPLDs
SDIO Interface, SD- / MMC-Card Mux	J3	PS MIO	SDIO interface connected to SD- / MMC-Card socket	MIO Bank Interfaces SDIO Port Expander
Board Peripheral's I²C Interfaces muxed to MPSoC I²C	J3	PS MIO	MPSoC I²C interface configured as master connected to on-board slaves	MIO Bank Interfaces 8-Channel I²C Switches
4 MIO to SC CPLD U17	J3	PS MIO	Functionality depending on MPSoC and CPLD firmware	System Controller CPLDs
15 MIO to SC CPLD U39	J3	PS MIO	Functionality depending on MPSoC and CPLD firmware	System Controller CPDLs
Ethernet PHY RGMII	J3	PS MIO	Ethernet PHY U12 connected per RGMII	MIO Bank Interfaces Gigabit Ethernet PHY
eMMC Flash	J3	PS MIO	eMMC Flash memory interface on PS bank	MIO Bank Interfaces eMMC Memory
USB2.0 PHY ULPI	J2	PS MIO	USB2.0 PHY U9 connected per ULPI	MIO Bank Interfaces High-speed USB ULPI PHY
SAMTEC FireFly Connector J6/J15	J2	MGT Bank	MGT Lanes to Samtec FireFly connector	MGT Interfaces SFP+ and FireFly
JTAG Interface via XMOD Header J12	J2	PS Config	MPSoC USB programmable JTAG interface	MIO Bank Interfaces JTAG Interface
USB3.0 Lane	J2	PSGT	USB3.0 PS MGT Lane	MIO Bank Interfaces PS GT Bank Interfaces
4-port USB3.0 Hub	-	-	USB3.0 (2.0 compatible) Hub with 4 ports	MIO Bank Interfaces 4-port USB3.0 Hub
USB3.0 / RJ45 GbE Connector J7, USB3.0 Connector J8	-	-	2-port USB3.0 / RJ45 GbE Connector (stacked)	MIO Bank Interfaces
25 SoM Control Signals to SC CPLDs U17 / U39	J2	On-module DC-DC converter, PLL clock generator	Control Signals, e.g. "Enable"- / "Power Good" - signals of DC-DC-converter and further on-module peripherals	Power-On Sequence Diagram Programmable PLL Clock Generator
150 MHz Osci Clock Input	J2	-	150 MHz SATA interface MGT clock	Oscillators
Signals DONE, INIT_B, SRST_B, ... to SC CPLD U39	J2	PS Config	MPSoC control signal for PS- / PL configuration	System Controller CPLDs
SATA Connector J31 PCIe Connector J1 DisplayPort J13	J2	PSGT	Connectors of the MGT based data interfaces	PS GT Bank Interfaces
PLL Clock Output to ▪ PCIe Interface ▪ On-board PLL U35 ▪ MGT Bank (B2B J3)	J2	On-module PLL clock generator	Reference clock signals of the on-module programmable PLL clock generator	Programmable PLL Clock Generator
4 I/O's to PMOD P2 via IC U33	J4	PL Bank (FMC_VADJ)	PL user I/O's accessible on PMOD connector P2	CAN FD Interface and PMOD Connectors

3 I/O's to SC CPLD U17 via IC U32	J4	PL Bank (FMC_VADJ)	PL user I/O's routed to System Controller CPLD U17	System Controller CPLDs
FMC HPC J5 • 46 LVDS pairs (92 I/O's) • 1 LVDS Clock to PL Bank	J4	PL Bank (FMC_VADJ)	PL I/O-bank pins, differential pairs 1 clock capable PL bank pin-pair	FMC HPC Connector Programmable PLL Clock Generator

Table 1: Description of depicted on-board peripherals

Main Components

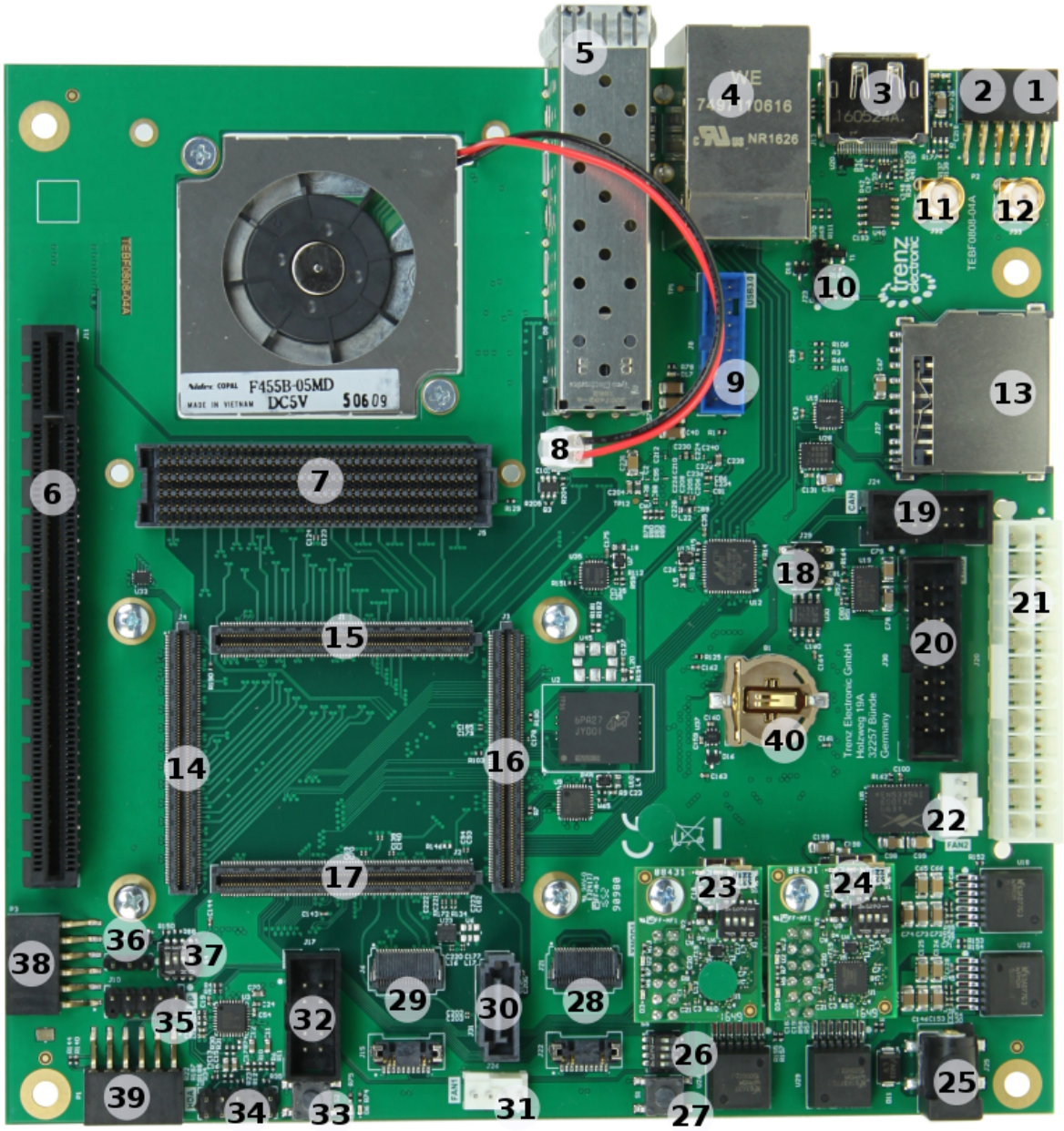

Figure 2: TEBF0808-04 Carrier Board

1. PMOD connector, P2
2. MicroSD Card socket (on bottom side), J16
3. DisplayPort connector, J13
4. USB3.0 A 2x , RJ45 1x (stacked), J7
5. SFP+ 2x1 cage, J14
6. PCIe x16 connector (one PCIe lane connected), J11
7. FMC HPC connector, J5
8. FMC-Fan connector 5V, J19
9. USB3.0 connector, J8
10. PC-BEEPER 4-pin header, J23
11. SMA coaxial connector (SI5338A clock output), J32
12. SMA coaxial connector (clock input to MPSoC module), J33
13. MMC Card socket, J27
14. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J4
15. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J1
16. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J3
17. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J2
18. CAN bus 6-pin header, J29
19. CAN bus 10-pin connector, J24
20. ARM JTAG 20-pin connector, J30
21. ATX-24 power supply connector, J20
22. 4-Wire PWM fan connector, J35
23. JTAG/UART header ('XMOD FTDI JTAG Adapter'-compatible) for access to MPSoC module, J12
24. JTAG/UART header ('XMOD FTDI JTAG Adapter'-compatible) for access to System Controller CPLDs, J28
25. Power Jack 2.1mm 12V, J25
26. 4-bit DIP-switch, S5
27. Power Button, S1
28. Samtec FireFly connector for reverse loopback, J21/J22
29. Samtec FireFly connector (4 GT lanes bidirectional), J6/J15
30. SATA header, J31
31. 4-Wire PWM fan connector, J26
32. I²C interface of programmable on-module PLL (10-pin header), J17
33. Reset Button, S2
34. INTEL HDA 9-pin header, J9
35. Intel front panel (PWR-/RST-Button, HD-/PWR-LED) 9-pin header, J10
36. Samtec FireFly connector J6/J15 I²C interface (3-pin header), J34
37. 4-bit DIP-switch, S4
38. PMOD connector, P3
39. PMOD connector, P1
40. Battery Holder CR1220, B1

Initial Delivery State

Storage device name	Content	Notes
User configuration EEPROMs (1x Microchip 24LC128-I/ST, 3x Microchip 24AA025E48T-I/OT)	Not programmed	-
USB3.0 HUB Configuration EEPROM (Microchip 24LC128-I/ST)	Not programmed	-
Si5338A programmable PLL NVM OTP	Not programmed	-

Table 2: Initial Delivery State of the flash memories

Signals, Interfaces and Pins

FMC HPC Connector

The FMC (FPGA Mezzanine Card) connector J5 with high pin count (HPC) provides as an ANSI/VITA 57.1 standard a modular interface to the MPSoCs FPGA and exposes numerous of its I/O pins for use by other mezzanine modules and expansion cards.

The connector supports single ended (VCCIO: FMC_VADJ) and differential signaling as the I/O's are routed from the FPGA banks as LVDS-pairs to the FMC connector.

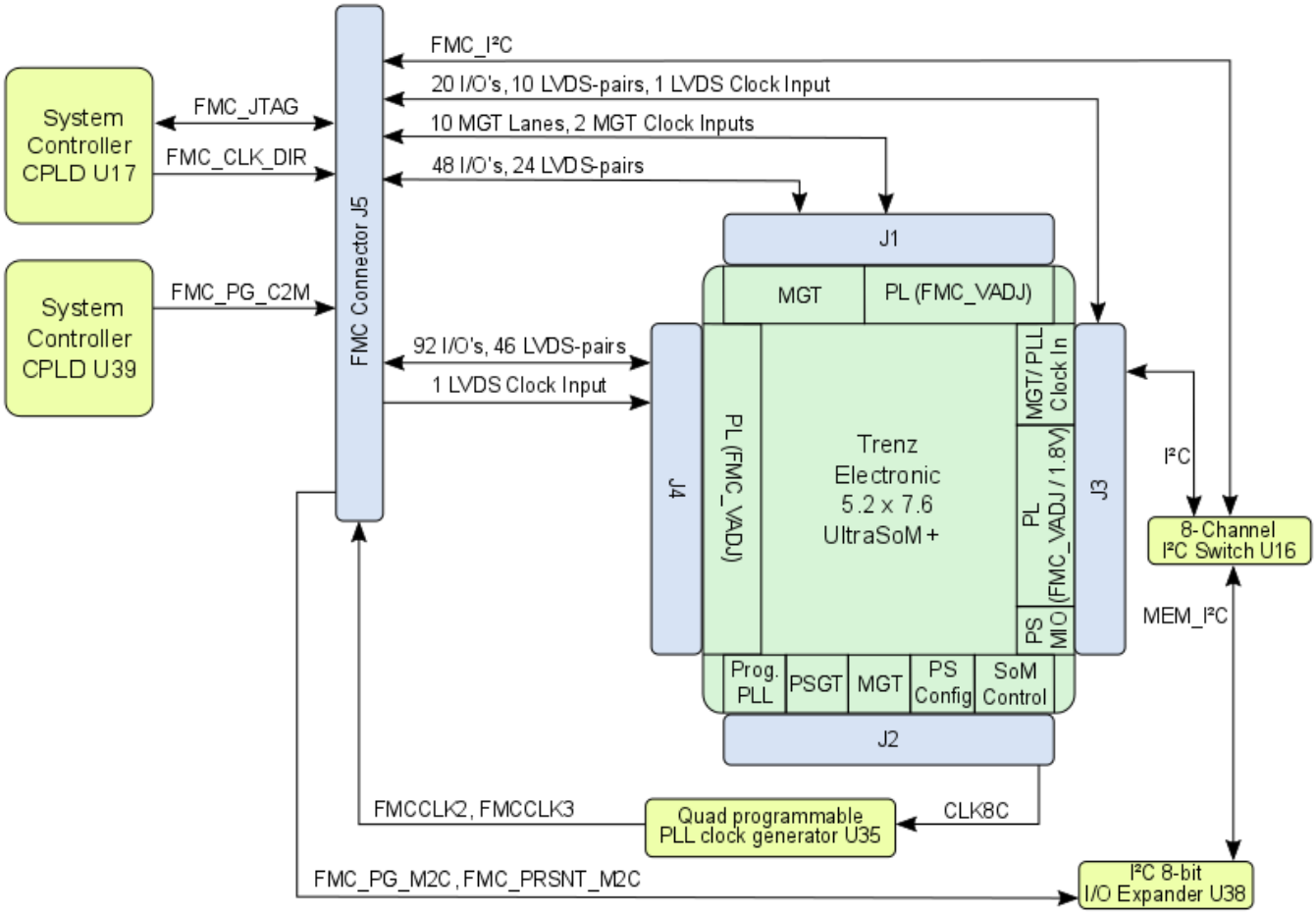

Figure 3: FMC HPC Connector

B2B	I/O Signal Count	LVDS-pairs count	VCCO bank Voltage	Reference Clock Input from FMC Connector	Notes
J1	48	24	FMC_VADJ	-	bank's VREF-pin connected to FMC connector pin J5-H1 (VREF_A_M2C)
J3	20	10	FMC_VADJ	1 LVDS clock from FMC connector J5 (pins J5-G2, J5-G3) to clock capable PL bank pin-pair	-
J4	92	46	FMC_VADJ	1 LVDS clock from FMC connectorJ5 (pins J5-H4, J5-H5) to clock capable PL bank pin-pair	bank's VREF-pin connected to FMC connector pin J5-H1 (VREF_A_M2C)

Table 3: FMC connector pin-outs of available logic banks of the MPSoC

The MGT-banks have also clock input-pins which are exposed to the FMC connector. Following MGT-lanes are available on the FMC connectors J5:

Schematic Names of the MGT Signals	B2B Connector Pins	FMC Connector Pins
B228_RX3_P, B228_RX3_N B228_TX3_P, B228_TX3_N	pins J1-51, J1-53 pins J1-50, J1-52	pins J5-A10, J5-A11 pins J5-A30, J5-A31
B228_RX2_P, B228_RX2_N B228_TX2_P, B228_TX2_N	pins J1-57, J1-59 pins J1-56, J1-58	pins J5-A6, J5-A7 pins J5-A26, J5-A27
B228_RX1_P, B228_RX1_N B228_TX1_P, B228_TX1_N	pins J1-63, J1-65 pins J1-62, J1-64	pins J5-A2, J5-A3 pins J5-A22, J5-A23
B228_RX0_P, B228_RX0_N B228_TX0_P, B228_TX0_N	pins J1-69, J1-71 pins J1-68, J1-70	pins J5-C6, J5-C7 pins J5-C2, J5-C3
B229_RX3_P, B229_RX3_N B229_TX3_P, B229_TX3_N	pins J1-27, J1-29 pins J1-26, J1-28	pins J5-B12, J5-B13 pins J5-B32, J5-B33
B229_RX2_P, B229_RX2_N B229_TX2_P, B229_TX2_N	pins J1-33, J1-35 pins J1-32, J1-34	pins J5-B16, J5-B17 pins J5-B36, J5-B37
B229_RX1_P, B229_RX1_N B229_TX1_P, B229_TX1_N	pins J1-39, J1-41 pins J1-38, J1-40	pins J5-A18, J5-A19 pins J5-A38, J5-A39
B229_RX0_P, B229_RX0_N B229_TX0_P, B229_TX0_N	pins J1-45, J1-47 pins J1-44, J1-46	pins J5-A14, J5-A15 pins J5-A34, J5-A35
B230_RX1_P, B230_RX1_N B230_TX1_P, B230_TX1_N	pins J1-15, J1-17 pins J1-14, J1-16	pins J5-B4, J5-B5 pins J5-B24, J5-B25
B230_RX0_P, B230_RX0_N B230_TX0_P, B230_TX0_N	pins J1-21, J1-23 pins J1-20, J1-22	pins J5-B8, J5-B9 pins J5-B28, J5-B29

Table 4: FMC connector pin-outs of available MGT lanes of the MPSoC

The FMC connector provides pins for reference clock output to the Mezzanine module and clock input to PL banks of the MPSoC:

Clock Signal Schematic Name	FMC Connector Pins	Direction	Clock Source	Notes
B228_CLK0	J5-D4 / J5-D5	in	FMC Connector J5	Extern MGT clock
B229_CLK0	J5-B20 / J5-B21	in	FMC Connector J5	Extern MGT clock
FMCCLK2	J5-K4 / J5-K5	out	Carrier Board PLL SI5338A U35, CLK2	Clock signal to Mezzanine module
FMCCLK3	J5-J2 / J5-J3	out	Carrier Board PLL SI5338A U35, CLK3	Clock signal to Mezzanine module
B64_L14_P / B64_L14_N	J5-H4 / J5-H5	in	FMC Connector J5	Extern LVDS clock to PL bank
B48_L6_P / B48_L6_N	J5-G2 / J5-G3	in	FMC Connector J5	Extern LVDS clock to PL bank

Table 5: FMC connector pin-outs for reference clock output

The FMC connector provides further interfaces like JTAG and I²C interfaces:

Interfaces	I/O Signal Count	Pin schematic Names / FMC Pins	Connected to	Notes
JTAG	5	FMC_TCK, pin J5-D29 FMC_TMS, pin J5-D33 FMC_TDI, pin J5-D30 FMC_TDO, pin J5- D31	SC CPLD U17, bank 1	VCCIO: 3V3SB TRST_L, pin J5-D34 pulled-up to 3V3_PER

I²C	2	FMC_SCL, pin J5-C30 FMC_SDA, pin J5-C31	I²C Switch U16	I²C-lines pulled-up to 3V3_PER
Control Lines	4	FMC_PRSNT_M2C, pin J5-H2	I²C I/O Expander U38	'PG' = 'Power Good'-signal 'C2M' = carrier to (Mezzanine) module 'M2C' = (Mezzanine) module to carrier
		FMC_PG_C2M, pin J5-D1 (3V3_PER pull-up)	SC CPLD U39, bank 0	
		FMC_PG_M2C, pin J5-F1 (3V3_PER pull-up)	I²C I/O Expander U38	
		FMC_CLK_DIR, pin J5-B1 (pulled-down to GND)	SC CPLD U17, bank 1	

Table 6: FMC connector pin-outs of available interfaces to the System Controller CPLD

Several VCCIO voltages are available on the FMC connector to operate the I/O's on different voltage levels:

VCCIO Schematic Name	FMC Connector J5 Pins	Notes
12V	C35/C37	extern 12V power supply
3V3_PER	D32/D36/D38/D40/C39	3.3V peripheral supply voltage
FMC_VADJ	H40/G39/F40/E39	adjustable FMC VCCIO voltage, supplied by DC-DC converter U8

Table 7: Available VCCIO voltages on FMC connector

MIO Bank Interfaces

The TEBF0808 carrier board provides several interfaces, which are configured on the MIO banks 500 .. 503 of the Zynq Ultrascale+ MPSoC.

Following table contains the assignment of the MIO pins to the configured interfaces:

MIO	Configured as	System Controller CPLD	Notes
0..12	Dual QSPI	-	Dual Flash Memory on TE0808 / TE0803 SoM; Bootable
13..23	SD0: eMMC	-	eMMC Memory U2; Bootable
24, 25	-	CPLD (U39) MUXED	-
26..29	-	CPLD (U17 MUXED	Bootable JTAG (PJTAG0)
30	force reboot after FSBL-PLL config for PCIe	CPLD (U39) MUXED	-
31	PCIe reset	CPLD (U39) MUXED	-
32	-	CPLD (U39) MUXED	-
33	-	CPLD (U39) MUXED	-
34..37	-	CPLD (U39) MUXED	-
38, 39	I2C0	-	-
40	forwarded to PWRLED_P / LED_P	CPLD (U39) MUXED	-
41	-	-	-
42, 43	UART0	CPLD (U39) MUXED	-
44	SD_WP to FPGA	CPLD (U39) MUXED	-
45..51	SD1: SD	-	Bootable MikroSD / MMC Card
52..63	USB0	-	-
64..75	GEM3	-	Ethernet RGMII
76, 77	MDC / MDIO	-	Ethernet RGMII

Table 8: MIO Assignment

Following interfaces are provided by the MIO bank of the Zynq Ultrascale+ MPSoC:

- 4x USB3.0 Superspeed ports (downward compatible to USB2.0 Highspeed)
- SDIO port with muxed MikroSD and MMC Card socket
- Gigabit Ethernet interface connected per RGMII
- eMMC interface
- Master I²C interface to on-board peripherals

The block-diagram below visualizes the interfaces of the MIO bank at the Zynq Ultrascale+ MPSoC and their associated on-board peripherals.

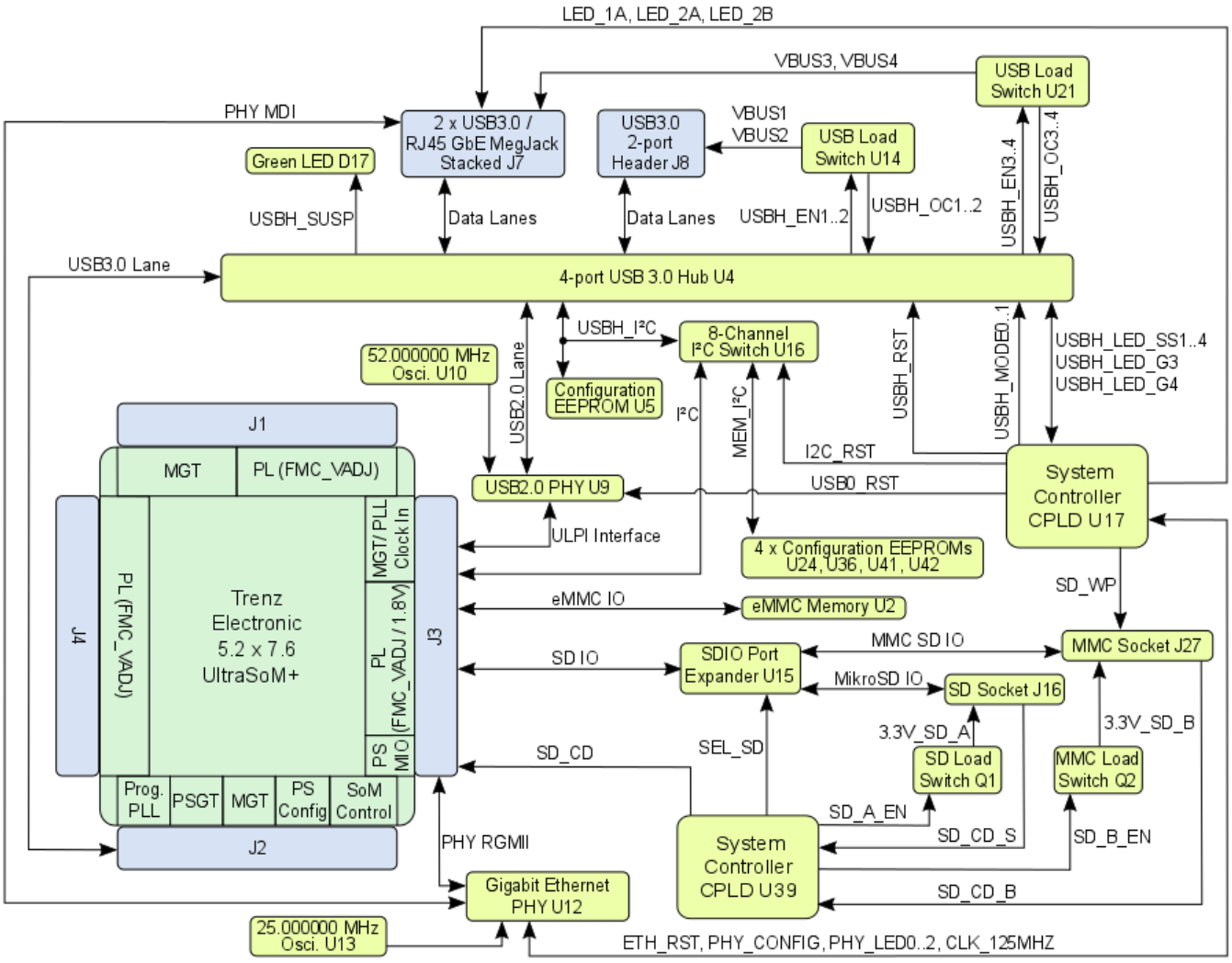

Figure 4: TEBF0808 MIO Interfaces

PS GT Bank Interfaces

The PS GT Bank 505 provides beside the USB3.0 Lane also following interfaces:

- SATA (PS GT bank, MGT2 Lane)

- DisplayPort (PS GT bank, MGT3 Lane, only TX-pair routed)
- PCI Express (PS GT bank, MGT0 Lane)

Function	MGT Lane	Schematic Names / B2B pins	Required Ref Clock	Clock Source	Comment
PCIe	PS 0	PCI_TX_N, pin J2-67 PCI_TX_P, pin J2-69 PCI_RX_N, pin J2-70 PCI_RX_P, pin J2-72	100 MHz	clock signal of SoM's prog. PLL	single lane PCIe connector clock signal routed on carrier board to PCIe connector J1
USB3	PS 1	USB3_TXUP_N, pin J2-61 USB3_TXUP_P, pin J2-63 USB3_RXUP_N, pin J2-64 USB3_RXUP_P, pin J2-66	100 MHz	clock signal of SoM's prog. PLL	clock signal routed on-module, Optional (not equipped) 100 MHz osci. U6 is possible (Configurable on Zynq PS).
SATA	PS 2	SATA_TX_N, pin J2-55 SATA_TX_P, pin J2-57 SATA_RX_N, pin J2-58 SATA_RX_P, pin J2-60	150 MHz	On-board oscillator U23	optional: clock signal of SoM's prog. PLL
DP.0	PS 3	DP0_TX_N, pin J2-49 DP0_TX_P, pin J2-51	27 MHz	clock signal of SoM's prog. PLL	DisplayPort GT SERDES clock signal, routed on-module to MGT bank

Table 9: PS GT Lane Assignment

Following block diagram shows the wiring of the MGT Lanes of the PS GT bank 505 to the particular high speed data interfaces:

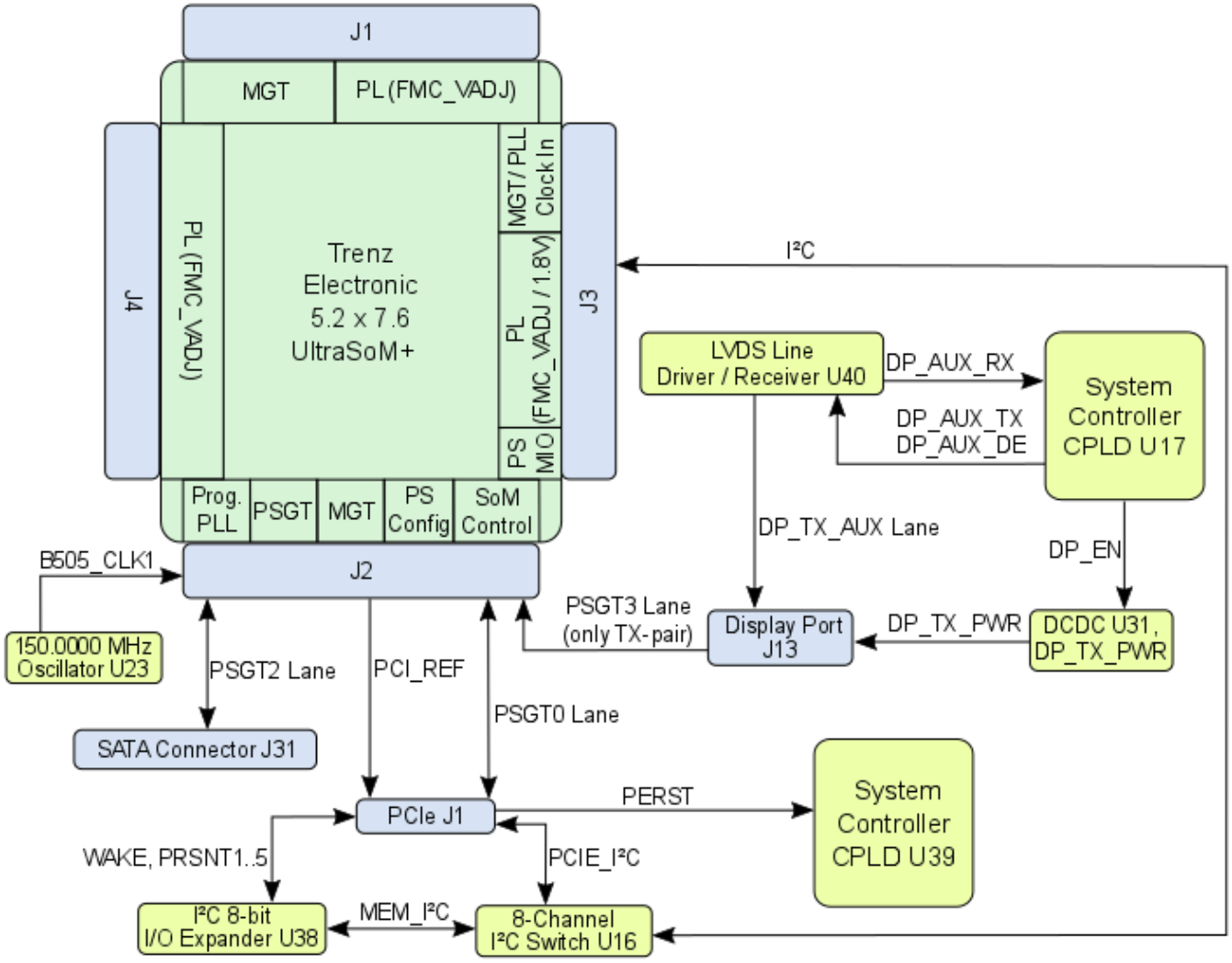

Figure 5: TEBF0808 PS GT Bank 505 Interface

Follwowing table contains a brief description of the control and status signals of PCIe interface:

Signal Schematic Name	FPGA Direction	Description	Logic
WAKE	Input	Link reactivation	Low active
PERST	Input	PCI Express reset input	Low active
PRSNT1	Input	Reference pin for PCIe card lane size	-
PRSNT2	Input	PCI Express ×1 cards	connect to PRSNT1
PRSNT3	Input	PCI Express ×4 cards	connect to PRSNT1
PRSNT4	Input	PCI Express ×8 cards	connect to PRSNT1
PRSNT5	Input	PCI Express ×16 cards	connect to PRSNT1
PCIE_I²C	BiDir	2-wire PCIE System Management Bus	-

Table 10: Description of MGT Connectors Control and Status Signals

MGT Interfaces SFP+ and FireFly

The TEBF0808 carrier board provides the high speed MGT interface connectors "SFP+" (Enhanced small form-factor pluggable) and Samtec "FireFly". This connectors are capable of data transmission rates up to 10 Gbit/s with SFP+ and 28 Gbit/s with FireFly.

Function	MGT Lane	Schematic Names / B2B pins	Required Ref Clock	Clock Source	Comment
FireFly	MGT Lanes 0..3	B128_RX3_N, B128_RX3_P, pins J2-28, J2-30 B128_TX3_N, B128_TX3_P, pins J2-25, J2-27 B128_RX2_N, B128_RX2_P, pins J2-34, J2-36 B128_TX2_N, B128_TX2_P, pins J2-31, J2-33 B128_RX1_N, B128_RX1_P, pins J2-40, J2-42 B128_TX1_N, B128_TX1_P, pins J2-37, J2-39 B128_RX0_N, B128_RX0_P, pins J2-46, J2-48 B128_TX0_N, B128_TX0_P, pins J2-43, J2-45	-	clock signal of SoM's prog. PLL	clock signal on-module routed to MGT bank
SFP	MGT Lane 2	B230_RX2_P, pin J1-9 B230_RX2_N, pin J1-11 B230_TX2_P, pin J1-8 B230_TX2_N, pin J1-10	125 / 156.25 MHz	clock signal of SoM's prog. PLL	clock signal routed on carrier board to MGT bank
SFP	MGT Lane 3	B230_RX3_P, pin J1-3 B230_RX3_N, pin J1-5 B230_TX3_P, pin J1-2 B230_TX3_N, pin J1-4	125 / 156.25 MHz	clock signal of SoM's prog. PLL	clock signal routed on carrier board to MGT bank

Table 11: MGT Lane Assignment

Following block diagram show the wiring of the MGT lanes to the particular interface connectors:

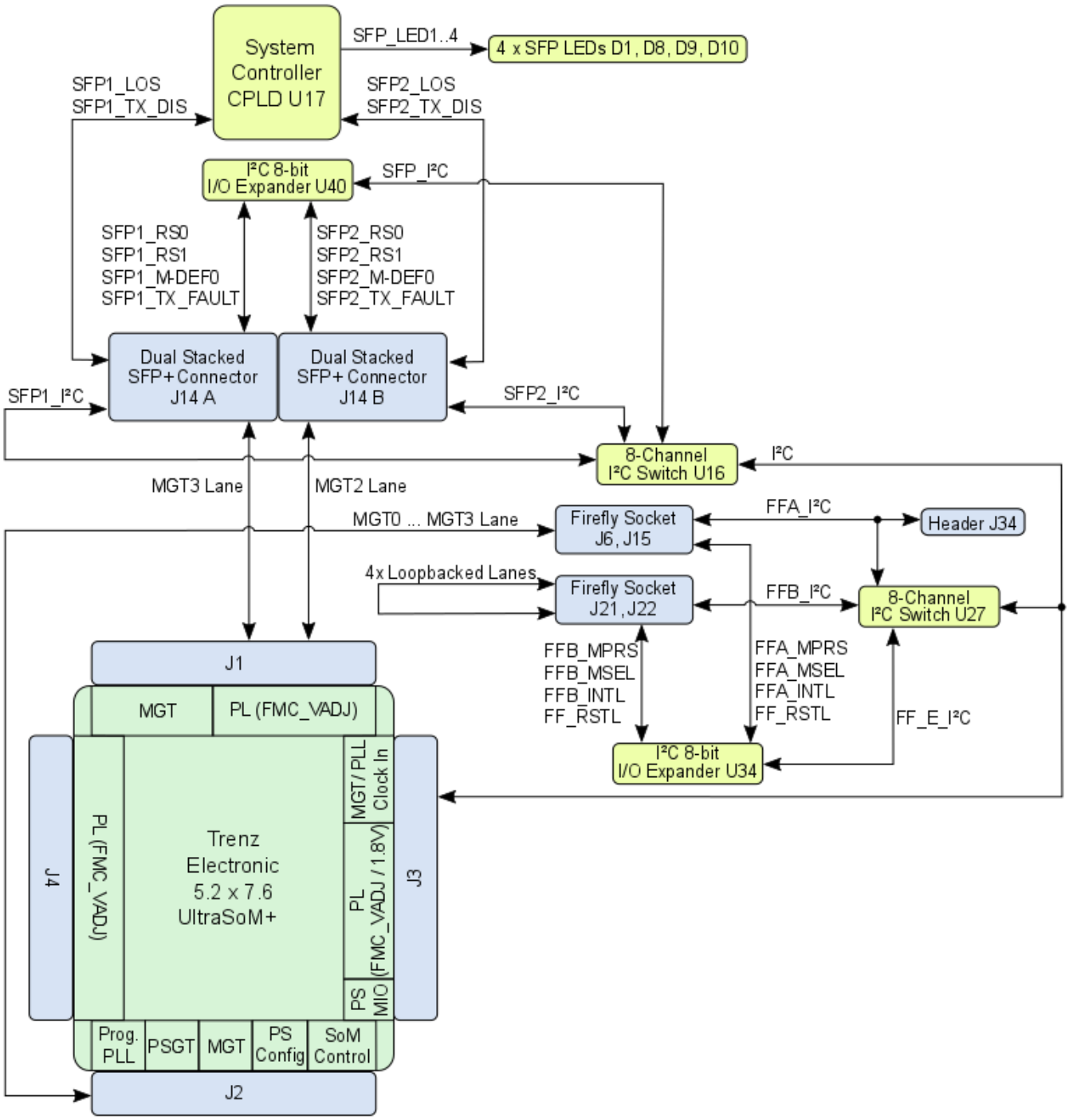

Figure 6: TEBF0808 MGT Interfaces

As shown on the block diagram, the FireFly connector pair J21, J22 provides four reversed looped back MGT lanes. To test any of the on-board MGT lanes or of an extern device, 4 RX/TX differential pairs are bridged on the connector, hence the transmitted data on these MGT lanes flows back to their sources in a loop-back circuit without intentional processing or modification.

Follwowing table contains a brief description of the control and status signals of the MGT lanes incorporating SFP+ and Samtec FireFly connectors:

Signal Schematic Name	Connector Type	FPGA Direction	Description	Logic
SFPx_TX_DISABLE	SFP+	Output	SFP Enabled / Disabled	Low active
SFPx_LOS	SFP+	Input	Loss of receiver signal	High active
SFPx_RS0	SFP+	Output	Full RX bandwidth	Low active
SFPx_RS1	SFP+	Output	Reduced RX bandwidth	Low active
SFPx_M-DEF0	SFP+	Input	Module present / not present	Low active
SFPx_TX_FAULT	SFP+	Input	Fault / Normal Operation	High active
SFPx_I²C	SFP+	BiDir	2-wire Serial Interface	-
FFx_MPRS	FireFly	Output	depending on connected module	-
FFx_MSEL	FireFly	Output	depending on connected module	-
FFx_INTL	FireFly	Input	Module interrupt line	-
FFx_RSTL	FireFly	Output	Module reset line	-
FFx_I²C	FireFly	BiDir	2-wire Serial Interface	-

Table 12: Description of MGT Connectors Control and Status Signals

CAN FD Interface and PMOD Connectors

On the carrier board there is a CAN FD (CAN with Flexible Data-Rate) interface available which is accessible on the CAN headers J24 (10-pin IDC connector) or J29 (6-pin header), which are connected to the CAN FD transceiver U30.

Additionally the carrier board provides PMOD connectors with GPIO and I²C interface:

PMOD	Interface	Connected to	Notes
P1	I²C	8-channel I²C Switch U27	Accessible on MPSoC's I²C interface through I²C switch U27
P2	GPIO	HP Bank of MPSoC (4 I/O's, B65_T0 ... B65_T3), System Controller CPLD U17 (4 I/O's, EX_IO1 ... EX_IO4)	Voltage translation via IC U33 with direction control, only singled-ended signaling possible
P3	I²C	8-channel I²C Switch U27	Accessible on MPSoC's I²C interface through I²C switch U27

Table 13: PMOD Pin Assignment

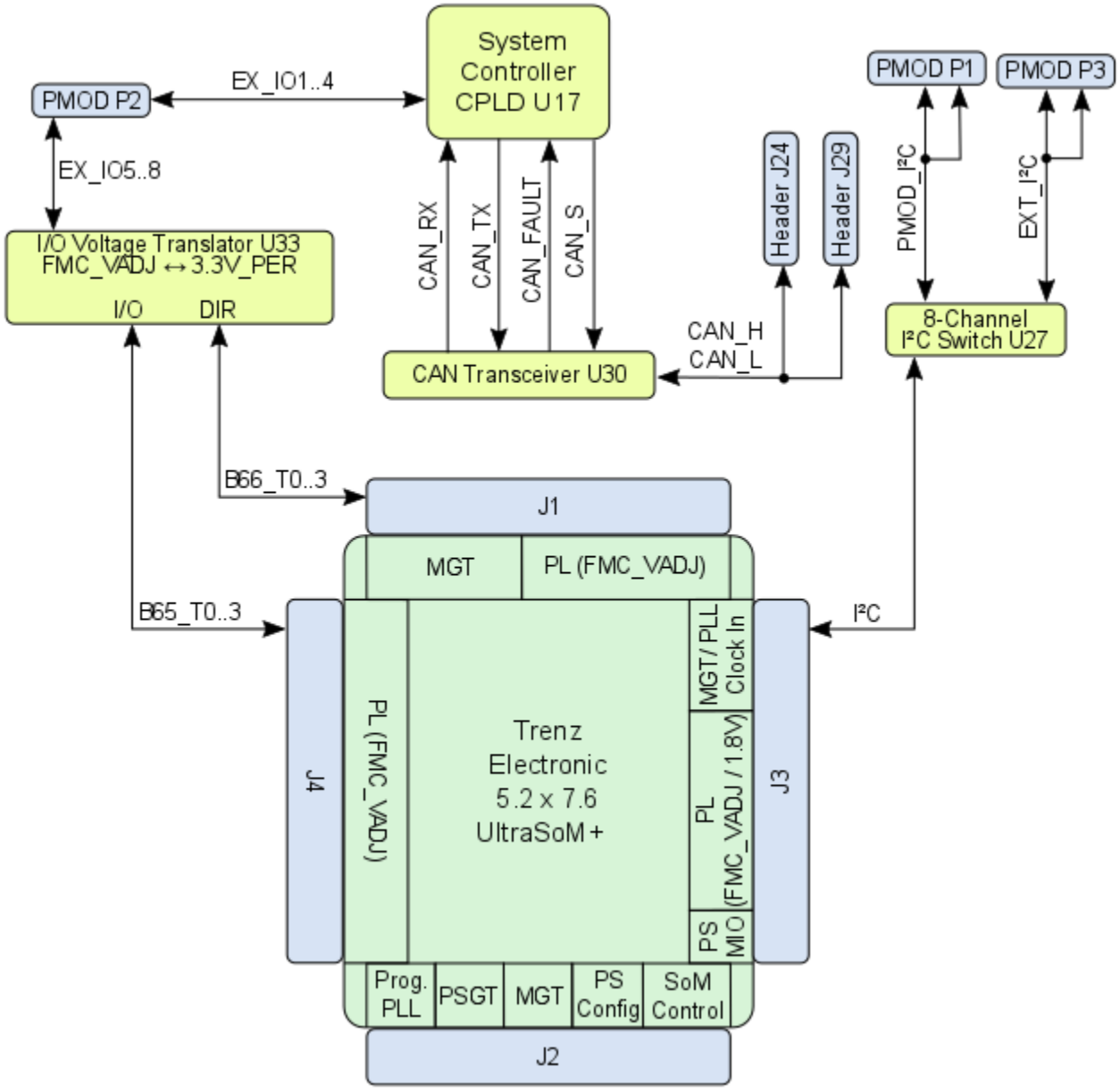

Figure 7: TEBF0808 CAN Interfaces, PMOD

Intel-PC Compatible Headers and FAN Connectors

The TEBF0808 carrier board provides with its Mini-ITX form factor the possibility to encase the boa rd in a PC Enclosure. For this purpose, the board is equipped with several Intel-PC compatible headers to connect them to the PC Enclosure.

Headers are available for following PC front panel elements

- Reset Button
- Power Button
- Power LED

- Hard Disc (HD) LED
- Intel High Definition Audio (HDA) Jacks

Following table gives an overview about the particular headers and a description about their functionalities:

Header	Pin Name	Functionality	Connected to	Notes
J10	Pin 1, HD LED+ Pin 3, HD LED- Pin 2, PWRLED+ Pin 4, PWRLED- Pin 5, GND Pin 7, RSTSW Pin 6, PWRSW Pin 8, GND Pin 9, +5V DC	HD LED Anode HD LED Cathode Power LED Anode Power LED Cathode Ground Reset Switch Power Switch Ground 5V DC Supply	SC CPLD U39	Reset and Power switch-pins are also connected to switch buttons S1 and S2
J9	Pin 1, PORT1L Pin 3, PORT1R Pin 9, PORT2L Pin 5, PORT2R Pin 7, SENS_SEND Pin 2, GND	Microphone Jack Left Microphone Jack Right Audio Out Jack Left Audio Out Jack Right Jack Detect / Mic in Ground	24-bit Audio Codec U3	-
J23	Pin 1, 3V3SB Pin 4, S1	3.3V DC Supply PC compatible Beeper	SC CPLD U39	-
J26	Pin 1, GND Pin 2, 12V Pin 3, F1SENSE Pin 4, F1PWM	Ground 12V DC Supply RPM PWM	SC CPLD U39	4-wire PWM FAN connector
J35	Pin 1, GND Pin 2, 12V Pin 3, F2SENSE Pin 4, F2PWM	Ground 12V DC Supply RPM PWM	SC CPLD U39	4-wire PWM FAN connector optional load switch U48 to turn off/on FAN with pin F2_EN
J19	Pin 1, GND Pin 2, 5V	Ground 5V DC Supply	Load Switch Q3 (5V DC)	2-wire FAN connector Fan off/on switchable by signal 'FAN_FMC_EN' on SC CPLD U39

Table 14: PC compatible Headers

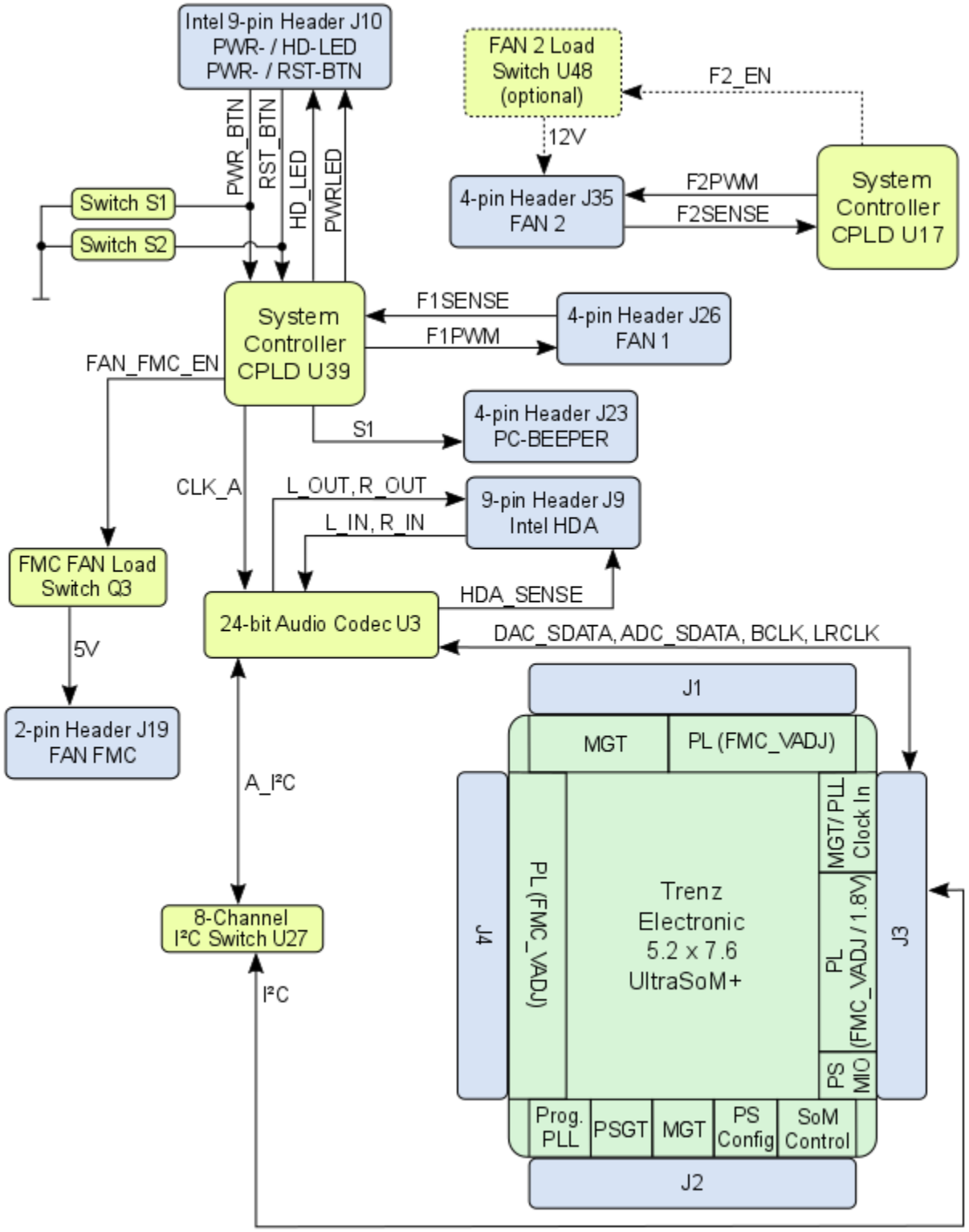
Intel 9-pin Header J10
PWR- / HD-LED
PWR- / RST-BTN
PWR_BTN
RST_BTN
HD_LED
PWRLED
Switch S1
Switch S2
FAN 2 Load Switch U48 (optional)
F2_EN
12V
4-pin Header J35 FAN 2
F2PWM
F2SENSE
System Controller CPLD U17
System Controller CPLD U39
F1SENSE
F1PWM
4-pin Header J26 FAN 1
FAN_FMC_EN
S1
4-pin Header J23 PC-BEEPER
CLK_A
L_OUT, R_OUT
L_IN, R_IN
9-pin Header J9 Intel HDA
FMC FAN Load Switch Q3
HDA_SENSE
24-bit Audio Codec U3
DAC_SDATA, ADC_SDATA, BCLK, LRCLK
5V
2-pin Header J19 FAN FMC
A_I²C
J1
MGT
PL (FMC_VADJ)
J4
PL (FMC_VADJ)
Trenz Electronic 5.2 x 7.6 UltraSoM+
MGT/ PLL Clock In
PL (FMC_VADJ / 1.8V)
PS MIO
J3
Prog. PLL
PSGT
MGT
PS Config
SoM Control
J2
8-Channel I²C Switch U27
I²C

Figure 8: TEBF0808 PC Compatible Headers

JTAG Interface

The TEBF0808 carrier board provides several JTAG interfaces to program both the System Controller CPLDs and the Zynq Ultrascale+ MPSoC.

Therefore, the board is equipped with two JTAG/UART headers, which have 'XMOD FTDI JTAG Adapter'-compatible pin-assignment. So in use with the XMOD-FT2232H adapter-board TE0790 the mounted SoM and the System Controller CPLDs can be programmed via USB interface.

The System Controller CPLDs will be programmed by the XMOD-Header J28 in a cascaded JTAG chain as visualized in Figure 9. To program the System Controller CPLDs, the JTAG interface of these devices have to be activated by DIP-switch S4-3.
The 4 GPIO/UART pins (XMOD1_A/B/E/G) of the XMOD-Header J28 are routed to the System Controller CPLD U17.

XMOD-Header J12 is designated to program the Zynq Ultrascale+ MPSoC via USB interface, the 4 GPIO/UART pins (XMOD2_A/B/E/G) of this header are routed to the System Controller CPLD U39.

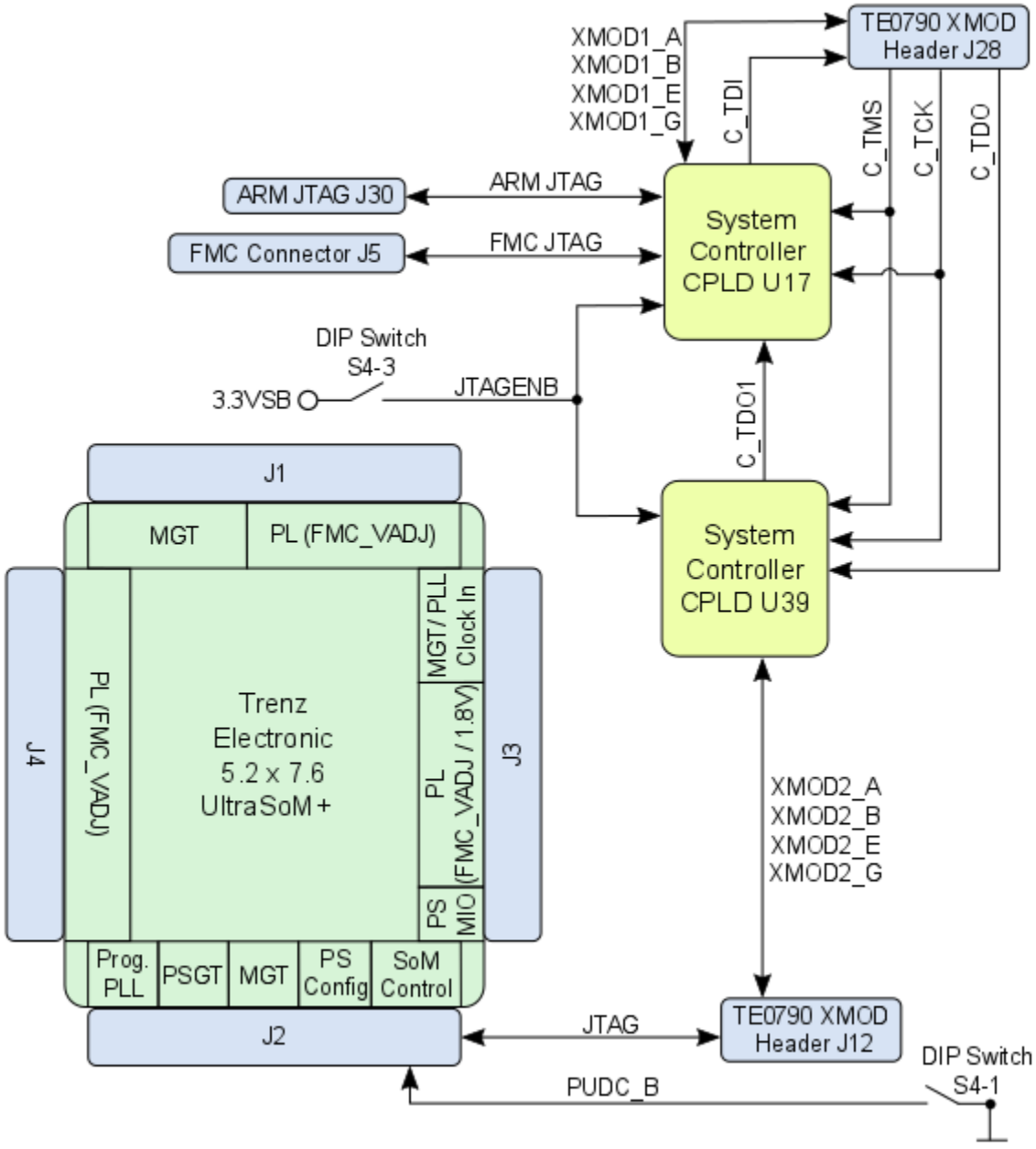

Figure 9: TEBF0808 JTAG interfaces

Further JTAG interfaces of the TEBF0808 carrier board are the ARM JTAG 20-pin IDC connector J30 and on the FMC Connector J5. This JTAG interfaces are connected to the System Controller CPLD U17, hence the logical processing and forwarding of the JTAG signals depend on the SC CPLD firmware. The documentation of the firmware of the SC CPLD U17 contains detailed information on this matter.

On-board Peripherals

System Controller CPLDs

The TEBF0808 is equipped with two System Controller CPLDs - Lattice Semiconductor LCMXO2-1200HC (MachXO2 Product Family) - with the schematic designators U17 and U39.

The SC-CPLD is the central system management unit where essential control signals are logically linked by the implemented logic of the CPLD firmware, which generates output signals to control the system, the on-board peripherals and the interfaces. Interfaces like JTAG and I^2C between the on-board peripherals and to the FPGA-module are by-passed, forwarded and controlled by the System Controller CPLD.

Other tasks of the System Controller CPLD are the monitoring of the power-on sequence and to display the programming state of the FPGA module.

Both System Controller CPLDs are connected to the Zynq Ultrascale+ MPSoC through MIO, PL IO-bank pins and I²C interface. The CPLDs are connected with each other through the IO pins SC_IO0 ... SC_IO8.

The functionalities and configuration of the pins depend on the CPLDs' firmware. The documentations of the firmware of SC CPLD U17 and SC CPLD U39 contains detailed information on this matter.

Following block diagram visualizes the connection of the SC CPLDs with the Zynq Ultrascale+ MPSoC via PS (MIO), PL bank pins and I²C interface.

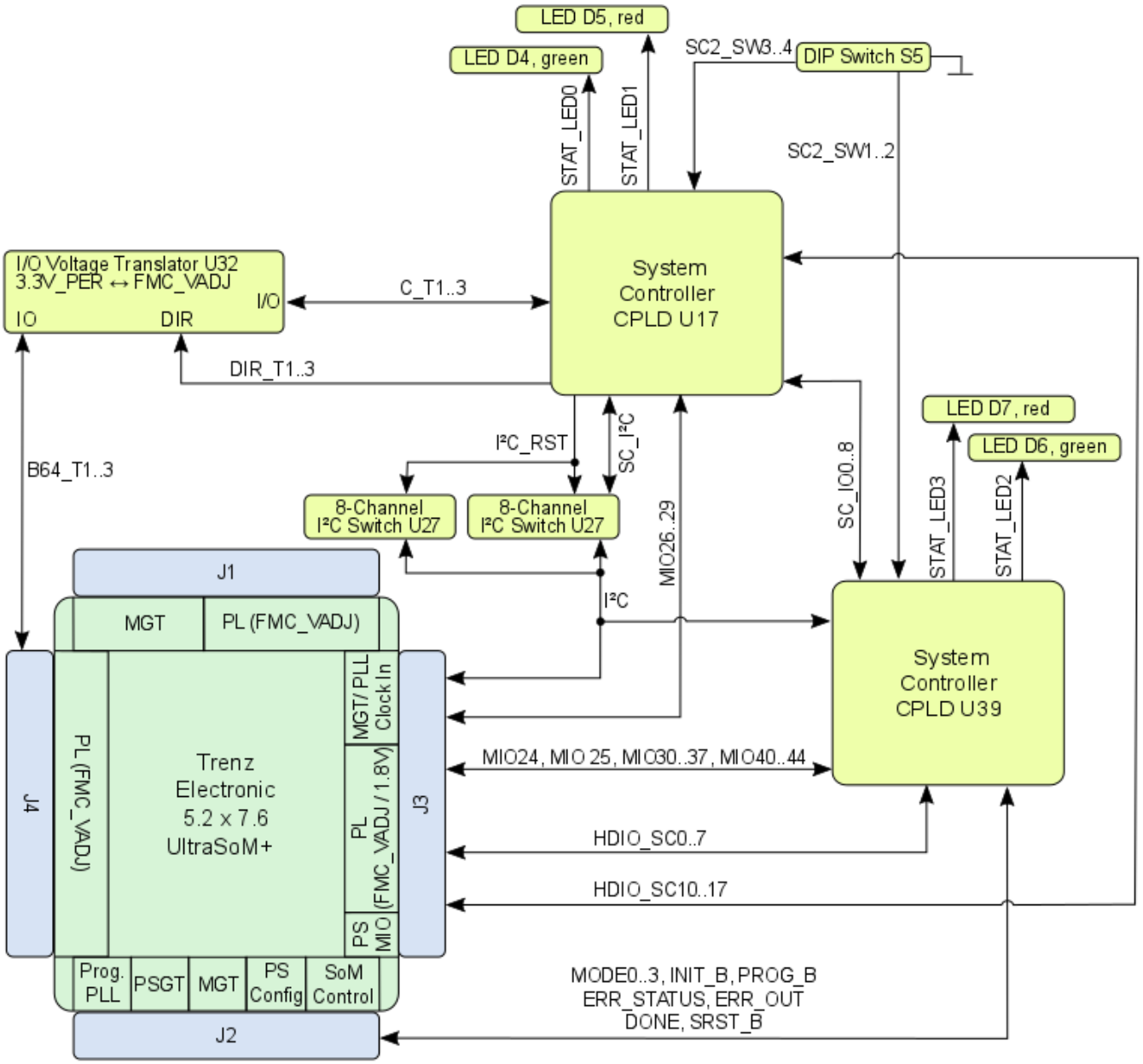

Figure 10: TEBF0808 System Controller CPLDs

Programmable PLL Clock Generator

The TEBF0808 carrier board is equipped with a Silicon Labs I^{2}C programmable quad PLL clock generator Si5338A (U35). It's output frequencies can be programmed by using the I^{2}C bus with address 0x70.

A 25 MHz (U7) oscillator is connected to pin 3 (IN3) and is used to generate the output clocks.

Once running, the frequency and other parameters can be changed by programming the device using the I²C-bus connected through I²C switch U16 between the Zynq module (master) and reference clock signal generator (slave).

Si5338A (U35) Input	Signal Schematic Name	Note
IN1/IN2	CLK8C_P, CLK8C_N	Clock signal of SoM's prog. PLL
IN3	reference clock signal from oscillator SiTime SiT8008BI (U7)	25.000000 MHz fixed frequency.
IN4	pin put to GND	LSB (pin 'IN4') of the default I²C-adress 0x70 not activated.
IN5/IN6	pins not connected / put to GND	not used, differential feedback input
Si5338A (U35) Output	**Signal Schematic Name**	**Note**
CLK0 A/B	SC_CLK0	Clock signal to SC CPLD U17 (single-ended signaling)
CLK1 A/B	SC_CLK1	Clock signal to SC CPLD U17 (single-ended signaling) negative complementary signal 'SC_CLK1_N' put out to SMA Coax J33
CLK2 A/B	FMCCLK2_P, FMCCLK2_N	Clock signal routed to FMC connector J5, pins J5-K4 / J5-K5
CLK3 A/B	FMCCLK3_P, FMCCLK3_N	Clock signal routed to FMC connector J5, pins J5-J2 / J5-J3

Table 15: Pin description of PLL clock generator Si5338A

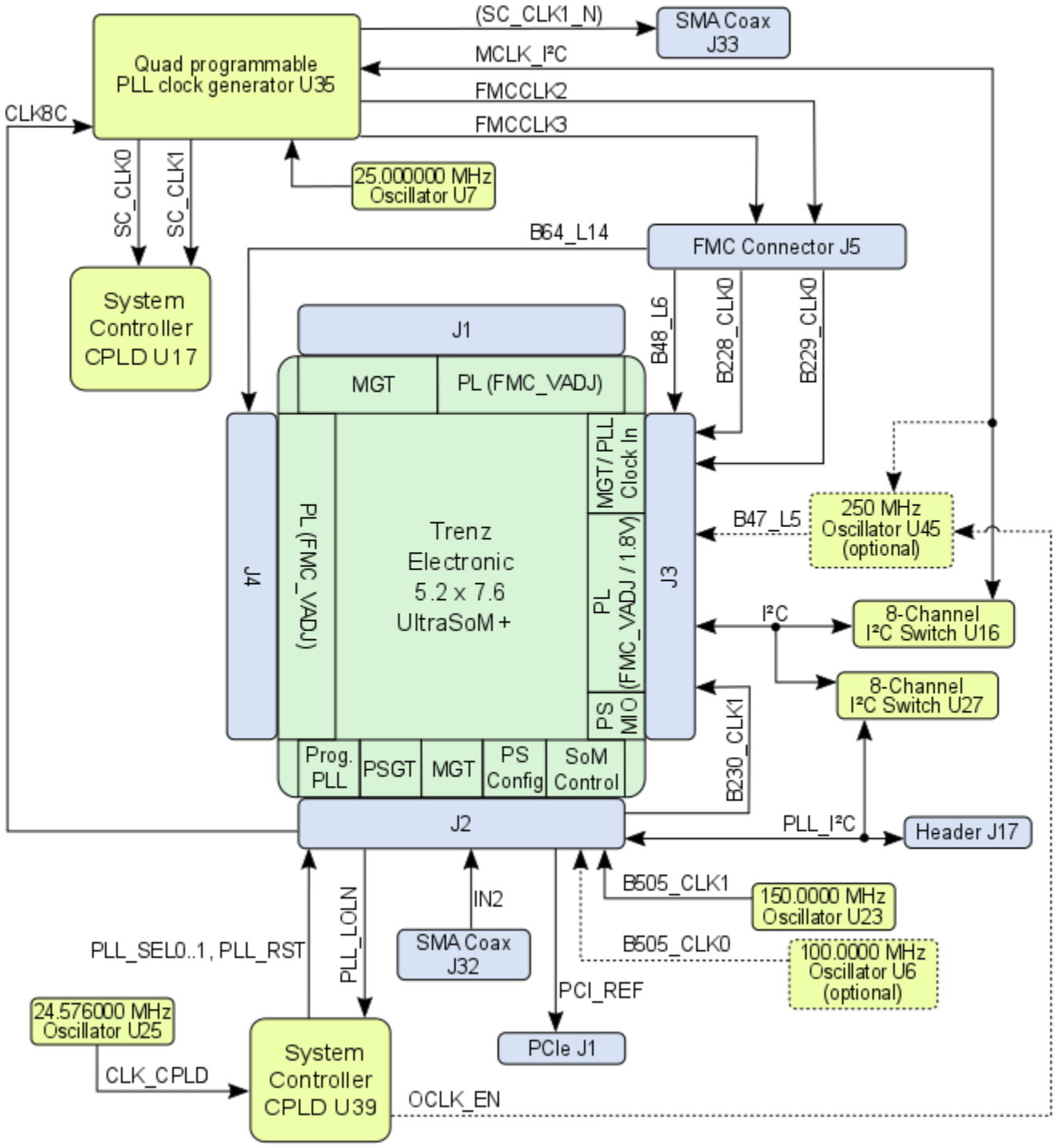

Figure 11: Clocking Configuration of TEBF0808 Carrier Board

⚠ Si5338 OTP ROM is not programmed by default at delivery, so it is customers responsibility to either configure Si5338 during FSBL or then use SiLabs programmer and burn the OTP ROM with customer fixed clock setup.

Si5338 OTP can only be programmed two times, as different user configurations may required different setup, TEBF0808 is normally shipped with blank OTP.
For more information Si5338 at SiLabs.

⚠ Refer to the TE0808 / TE0803 TRM for the configuration and for the internal routing of the on-module multi-channel PLL clock generator signals to the clock input pins of the MGT banks.

Oscillators

The TEBF0808 carrier board is equipped several on-board oscillators to provide the Zynq Ultrascale+ MPSoC's PS and PL banks and the on-board peripherals with reference clock-signals:

Clock Source	Schematic Name	Frequency	Clock Input Destination
SiTime SiT8008BI oscillator, U10	USB0_RCLK	52.000000 MHz	USB 2.0 transceiver PHY U9, pin 26
SiTime SiT8008BI oscillator, U13	ETH_CLK	25.000000 MHz	Gigabit Ethernet PHY U12, pin 34
SiTime SiT8008BI oscillator, U7	-	25.000000 MHz	Quad PLL clock generator U35, pin 3
DSC1123 oscillator, U23	B505_CLK1	150.0000 MHz	PS GT Bank, dedicated for SATA interface
DSC1123 oscillator, U6 **optional, not equipped**	B505_CLK0	100.0000 MHz	PS GT Bank, dedicated for USB interface
Silicon Labs 570FBB000290DG, U45 **optional, not equipped**	B47_L5 (LVDS)	250.MHz	PL Bank clock capable input pins
SiTime SiT8008BI oscillator, U25	CLK_CPLD	24.576000 MHz	System Controller CPLD U35, pin 128

Table 16: Reference clock signal oscillators

High-speed USB ULPI PHY

USB PHY (U9) is provided by USB3320 from Microchip. The ULPI interface is connected to the Zynq Ultrascale+ PS USB0. I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 52.000000 MHz oscillator (U10).

PHY Pin	Connected to	Notes
ULPI	PS bank MIO52 ... MIO63	Zynq Ultrascale+ USB0 MIO pins are connected to the PHY
REFCLK	-	52MHz from on board oscillator (U9)
REFSEL[0..2]	-	All pins set to GND selects the external reference clock frequency (52.000000 MHz)
RESETB	SC CPLD U17	Low active USB PHY Reset (pulled-up to PS_1.8V).
DP, DM	4-port USB3.0 Hub U4	USB2.0 data lane
CPEN	-	External USB power switch active-high enable signal
VBUS	5V	Connected to USB VBUS via a series of resistors, see schematic
ID	-	For an A-device connect to the ground. For a B-device, leave floating

Table 17: USB PHY interface connections

Gigabit Ethernet PHY

On-board Gigabit Ethernet PHY (U12) is provided with Marvell Alaska 88E1512 IC. The Ethernet PHY RGMII interface is connected to the Zynq Ultrascale+ Ethernet0 PS GEM3. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from the on-board 25.000000 MHz oscillator (U13). The 125MHz PHY output clock (PHY_CLK125M) is routed to System Controller CPLD U17, pin 70.

PHY Pin	Connected to	Notes
MDC/MDIO	PS bank MIO76, MIO77	-
PHY LED0..1	SC CPLD U17, pin 67,86	see schematic for details, forwarded to RJ45 GbE MagJack J7
PHY_LED2 / INTn:	SC CPLD U17, pin 85	Active low interrupt line
PHY_CLK125M	SC CPLD U17, pin 70	125 MHz Ethernet PHY clock out
CONFIG	SC CPLD U17, pin 65	Configuration of PHY address LSB and VDDO level
RESETn	SC CPLD U17, pin 62	Active low reset line
RGMII	PS bank MIO64 ... MIO75	Reduced Gigabit Media Independent Interface
SGMII	-	Serial Gigabit Media Independent Interface
MDI	RJ45 GbE MagJack J7	Media Dependent Interface

Table 18: Ethernet PHY interface connections

8-Channel I²C Switches

All on-board and on-module peripherals with accessible I²C interface are muxed to the I²C interface of the Zynq Ultrascale+ MPSoC as master.

For this purpose, the TEBF0808 carrier board is equipped with two 8-channel I²C switches provided by TCA9548A from Texas Instruments, together creating up to 16 switched I²C channels.

Refer to the data sheet of the TCA9548A chip how to address and and transmit data to the I²C slave devices through this switches.

The I^2C bus works internally on-module with reference voltage 1.8V, it is connected to the MPSoC I^2C interface via PS MIO bank (pins MIO38, MIO39) configured as master.

MIO	Signal Schematic Name	Notes
38	I2C_SCL	1.8V reference voltage
39	I2C_SDA	1.8V reference voltage

Table 19: MIO-pin assignment of the module's I^2C interface

I^2C addresses for on-board slave devices are listed in the table below:

I²C Slave Devices connected to MPSoC I²C Interface	I²C Switch Position	I²C Slave Address	Schematic Names of I²C Bus Lines
8-channel I²C switch U16	-	0x73	I2C_SDA / I2C_SCL
8-channel I²C switch U27	-	0x77	I2C_SDA / I2C_SCL
SC CPLD U39, bank 2, pins 52 (SDA), 50 (SCL)	-	User programmable	I2C_SDA / I2C_SCL

I²C Slave Devices connected to 8-channel I²C Switch U16	I²C Switch Position	I²C Slave Address	Schematic Names of I²C Bus Lines
On-board Quad programmable PLL clock generator U35 Si5338	0	0x70	MCLK_SDA / MCLK_SCL
8-bit I²C IO Expander U44	1	0x26	SFP_SDA / SFP_SCL
PCIe Connector J1	2	module dependent	PCIE_SDA / PCIE_SCL
SFP+ Connector J14A	3	module dependent	SFP1_SDA / SFP1_SCL
SFP+ Connector J14B	4	module dependent	SFP2_SDA / SFP2_SCL
Configuration EEPROM U42	5	0x54	MEM_SDA / MEM_SCL
Configuration EEPROM U36	5	0x52	MEM_SDA / MEM_SCL
Configuration EEPROM U41	5	0x51	MEM_SDA / MEM_SCL
Configuration EEPROM U22	5	0x50	MEM_SDA / MEM_SCL
8-bit I²C IO Expander U38	5	0x27	MEM_SDA / MEM_SCL
FMC Connector J5	6	module dependent	FMC_SDA / FMC_SCL
USB3.0 Hub configuration EEPROM U5	7	0x51	USBH_SDA / USBH_SCL
USB3.0 Hub	7	0x60	USBH_SDA / USBH_SCL
I²C Slave Devices connected to 8-channel I²C Switch U27	**I²C Switch Position**	**I²C Slave Address**	**Schematic Names of I²C Bus Lines**
PMOD Connector P1	0	module dependent	PMOD_SDA / PMOD_SCL
24-bit Audio Codec U3	1	0x38	A_I2C_SDA / A_I2C_SCL
FireFly Connector J15	2	module dependent	FFA_SDA / FFA_SCL
FireFly Connector J22	3	module dependent	FFB_SDA / FFB_SCL
On-module Quad programmable PLL clock generator Si5345 (TE0808)	4	0x69	PLL_SDA / PLL_SCL
SC CPLD U17, bank 3, pins 13 (SDA), 14 (SCL)	5	User programmable	SC_SDA / SC_SCL
8-bit I²C IO Expander U34	6	0x24	FF_E_SDA / FF_E_SCL
PMOD Connector P3	7	module dependent	EXT_SDA / EXT_SCL

Table 20: On-board peripherals' I²C-interfaces device slave addresses

Configuration EEPROMs

The TEBF0808 carrier board contains several EEPROMs for configuration and general user purposes. The EEPROMs are provided by Microchip and all have I²C interfaces:

EEPROM Modell	Schematic Designator	Memory Density	Purpose
24LC128-I/ST	U30	128 Kbit	user
24AA025E48T-I/OT	U36	2 Kbit	user
24AA025E48T-I/OT	U41	2 Kbit	user
24AA025E48T-I/OT	U42	2 Kbit	user
24LC128-I/ST	U5	128 Kbit	USB3.0 Hub U4 configuration memory

Table 21: On-board configuration EEPROMs overview

4-port USB3.0 Hub

On the carrier board there are up to 4 USB3.0 Super Speed ports available, which are also downward compatible to USB2.0 High Speed ports. The USB3.0 ports are provided by Cypress Semiconductor CYUSB3324 4-port USB3.0 Hub controller U4. The pin-strap configuration option of the USB3.0 Hub is disabled, so this controller gets the configuration data and parameter from the configuration EEPROM U5. The I²C interface of the EEPROM and the controller is also accessible by the Zynq Ultrascale+ MPSoC through I²C switch U16.

On the Upstream-side, this controller is connected to the MGT1 lane of MPSoC's PS GT bank to establish the USB3.0 data lane. For the USB2.0 interface, the controller is connected to the on-board USB2.0 PHY U9. The USB2.0 PHY is connected per ULPI interface (MIO pins 52..63) to MPSoC's MIO bank.

The USB3.0 Hub controller has also an ARM Cortex-M0 controller integrated, refer to the data sheet for further features and programmable options.

CAN FD Transceiver

On-board CAN FD (Flexible Data Rate) transceiver is provided by Texas Instruments TCAN337. This controller is the physical layer of the CAN interface and is specified for data rates up to 1 Mbps. The controller has many protection features included to ensure CAN network robustness and to eliminate the need for additional protection circuits. Refer to the data sheet of this transceiver for more details and specifications.

The transceiver is connected to System Controller CPLD U17, means it works on this interface with 3.3V VCCIO. The logical signal processing of the CAN interface depends on the current firmware ot the SC CPLD U17.

eMMC Memory

The TEBF0808 carrier board is equipped with embedded MMC memory connected to the PS MIO bank (MIO13 ... MIO23) of the Zynq Ultrascale+ MPSoC. The memory is provided by MTFC4GACAJCN-4M from Micron Technology. It has a memory density of 32 Gbit (4 GByte) and is sectored into 8 banks a 4 Gbit.

24-bit Audio Codec

For high resolution digital audio signal processing, the TEBF0808 carrier board is equipped with the Analog Devices 24-bit Audio Codec chip ADAU1761 with the schematic designator U3. The Audio Codec chip is connected to the Intel High Defintion Audio (Intel HDA) compatible 9-pin header J9 with single-ended signaling for analog stereo audio signal input and output. It supports also MIC / Jack detect. Its I²C control interface is accessible by the Zynq Ultrascale+ MPSoC through I²C switch U27.

The 24-bit Audio Codec provides numerous features and is also fully programmable with its dedicated graphical tool from the manufacturer. Refer to the data sheet of this chip for more detail information and specifications.

SDIO Port Expander

Due to the different signaling voltage levels of the MicroSD and MMC Card interfaces (3.3V) and the PS MIO bank of the Zynq Ultrascale+ MPSoC (1.8V), there is voltage-translation necessary, which is fullfilled by the SDIO port expander Texas Instruments TXS02612, U15. This IC also muxes the MikroSD and the MMC Card sockets to the SDIO port of the MPSoC, which is controlled by the signal 'SEL_SD' of the System Controller CPLD U39. The SC CPLD U39 also controls the load switches to enable the card sockets J16 and J27 and to report the card detect signal both of the sockets to the MPSoC (see schematic).

DIP-Switches

There are two 4-bit DIP-witches present on the TEBF0808 carrier board to configure options and set parameters. The following section describes the functionalities of the particular switches.

DIP-switch S4

Table below describes the functionalities of the switches of DIP-switch S4 at their single positions:

DIP-switch S4	Position ON	Position OFF	Notes

S4-1	PUDC_B is Low	PUDC_B is HIGH	Internal pull-up resistors during configuration are enabled at ON-position, means I/O's are 3-stated until configuration of the FPGA completes.
S4-2	x	x	not connected
S4-3	SC CPLDs' JTAG enabled	SC CPLDs' JTAG disabled	JTAG interface is enabled on both SC CPLDs, as this CPLDs are configured in a casdaced JTAG chain.
S4-4	DC-DC converter U18 (5V) enabled	DC-DC converter U18 (5V) not manually enabled	In OFF-position, the DC-DC-converter will be still enabled by the Enable-signal ('5V_EN') of SC CDPD U39 (wired-OR circuit).

Table 22: DIP-switch S4 functionality description

DIP-switch S5

DIP-switch S5 located close to PWR push-button is connected to the two System Controller CPLDs, its functionalities depend on the current firmware of the CPLDs.

The DIP-switch is connected to SC CPLD U17 and U39 as fellows:

DIP-switch S5	Signal Schematic Name	Connected to	Functionality	CPLD Documentation
S5-1	SC_SW1	SC CPLD U39, pin 133	set 2-bit code for boot mode selection	TEBF0808 Slave CPLD
S5-2	SC_SW2	SC CPLD U39, pin 138		Section: Boot Mode
S5-3	SC_SW3	SC CPLD U17, pin 6	user defined	TEBF0808 Master CPLD
S5-4	SC_SW4	SC CPLD U17, pin 5	set FMC_VADJ: 1.8V at ON-position, 1.2V at OFF-position	

Table 23: DIP-switch S5 connection to SC CPLDs

The boot mode of the mounted Ultrascale+ Zynq MPSoC module will be set in current SC CPLD U39 firmware version as described in the table below:

S5-1	S5-2	Description
ON	ON	Default, boot from SD/microSD or SPI Flash if no SD is detected
OFF	ON	Boot from eMMC
ON	OFF	Boot mode PJTAG0
OFF	OFF	Boot mode main JTAG

Table 23: DIP-switch S5 boot mode selection

On-board LEDs

The TEBF0808 carrier board is equipped with several LED to signal current states and activities. The functionality of the LEDs D4 ... D7 depends on the current firmware of the SC CPLDs U17 and U39.

LED	Color	Description and Notes
D4	green	Status LED, connected to SC CPLD U17
D5	red	Status LED, connected to SC CPLD U17
D6	green	Status LED, connected to SC CPLD U39
D7	red	Status LED, connected to SC CPLD U39
D1	red	SFP+ interface status LED, connected to SC CPLD U17

D8	green	SFP+ interface status LED, connected to SC CPLD U17
D9	red	SFP+ interface status LED, connected to SC CPLD U17
D10	green	SFP+ interface status LED, connected to SC CPLD U17
D17	green	LED is on if all USB3.0 and USB 2.0 ports are in the suspend state and is off when either of the ports comes out of the suspend state.

Table 24: On-board LEDs functionality description

Power and Power-On Sequence

Power Consumption

The maximum power consumption of a module mainly depends on the design which is running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Distribution Dependencies

All on-board voltages of the TEBF0808 are generated out of the extern applied 12V power supply.

There are following dependencies how the initial 12V power supply is distributed to the on-board DC-DC converters, which power up further DCDC converters and the particular on-board voltages:

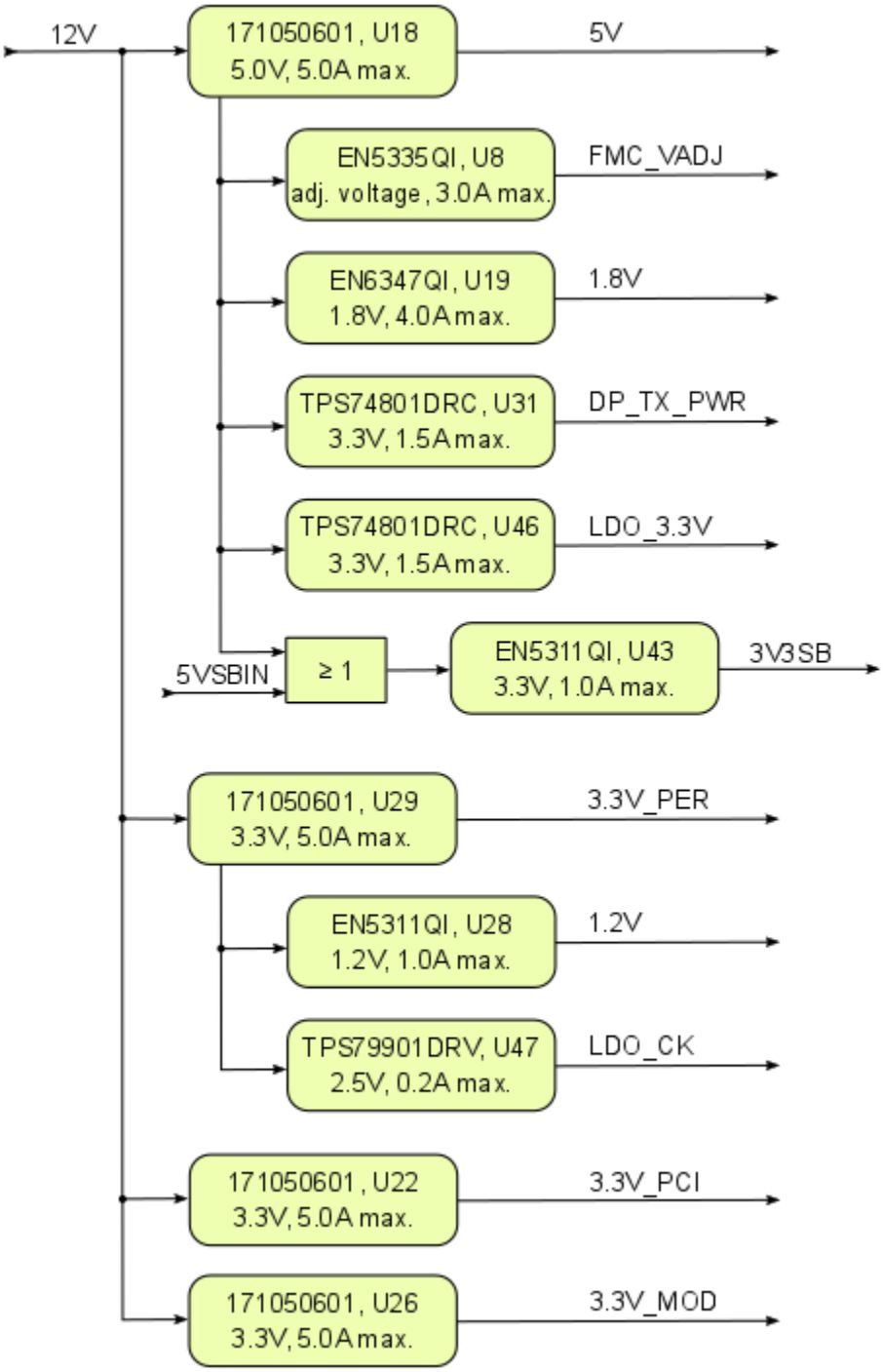

Figure 12: Power Distribution Diagram

⚠ Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

Power-On Sequence Diagram

The power-on sequence of the on-board DC-DC converters depens on the current firmware of the System Controller CPLD U39.

Following diagram visualizes the connection of the DC-DC converter control signals ('Enable', 'Power-Good') with System Controller CPLD U39, which enables the particular on-board voltages.

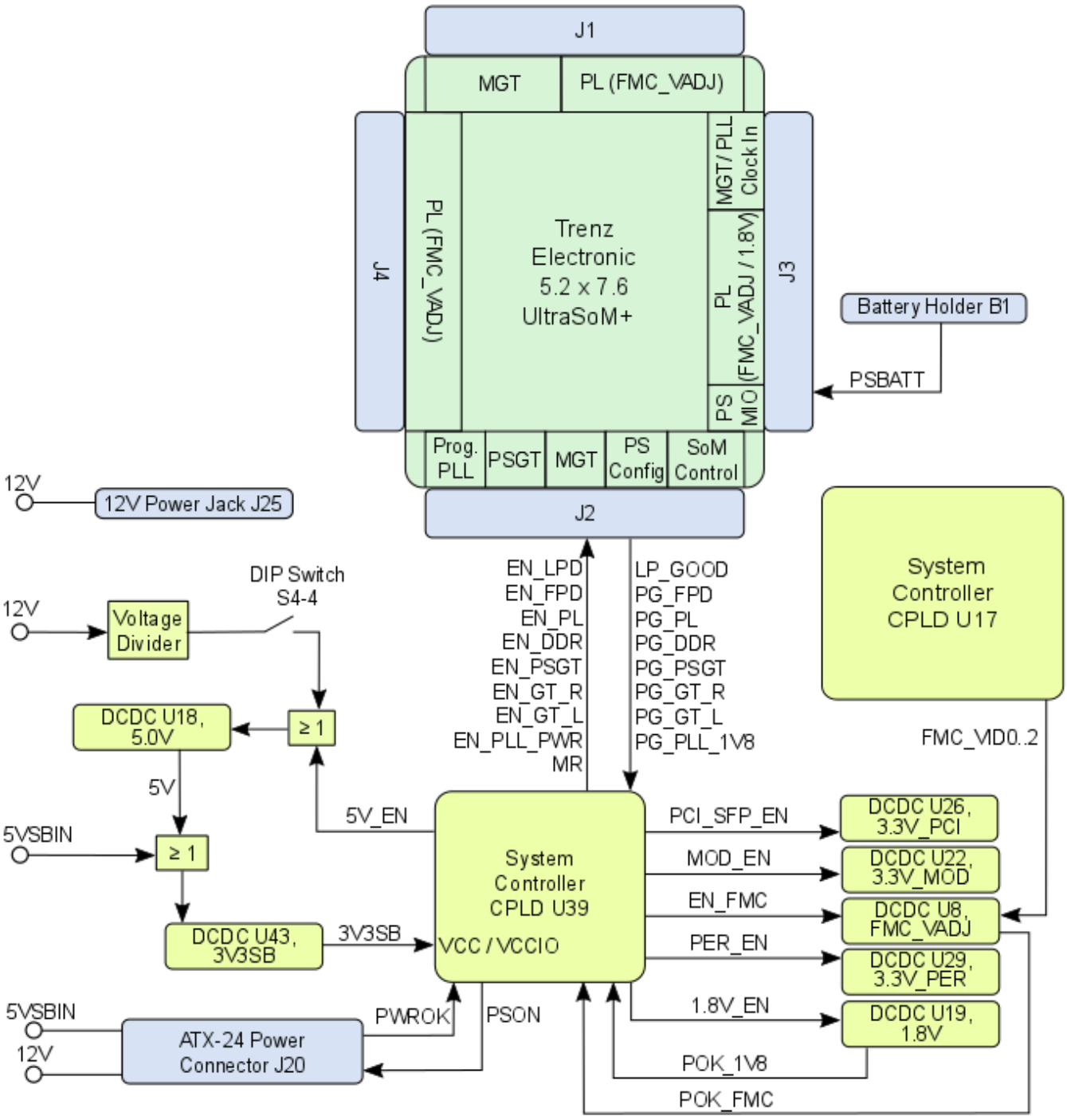

Figure 13: Power-On Sequence Utilizing DCDC Converter Control Signals

As shown in Figure 13, the DIP switch S4-4 has to be closed if using only 12V single power supply through 12V power jack J25, otherwise the 5V voltage level will not be enabled to generate the 3V3SB voltage to power up the SC CPLD U39 and starting the power-on sequence.
By using an ATX-24 power connector on J20, there is usually also a 5V supply voltage provided, hence the DIP switch S4-4 is not relevant in this case of power supply.

The TEBF0808 carrier board manages both the power-on sequence of the mounted TE0808 / TE0803 SoM and the on-board DC-DC converters via System Controller CPLD U39.

The power-on sequence of the TE0808 / TE0803 SoM is managed by utilizing the SoM's DC-DC converter control signals ('Enable', 'Power-Good'), so the DC-DC converters of the SoM dedicated to the particular Power Domains of the Zynq Ultrascale+ MPSoC will be powerer-up in a specific sequence to meet the recommended criteria to power up the Xilinx Zynq Ultrascale+ MPSoC properly.

To avoid any damages to the MPSoC module, check for stabilized on-board voltages in steady state before powering up the MPSoC's I/O bank voltages VCCOx. All I/O's should be tri-stated during power-on sequence.

Core voltages and main supply voltages of the Zynq Ultrascale+ MPSoC have to reach stable state and the "Power Good"-signals of the SoM have to be asserted before other voltages like bank's I/O voltages (VCCOx) can be powered up.

It is important that all PS and PL I/Os are tri-stated at power-on until the "Power Good"-signals are logically high, meaning that all on-module voltages have become stable and module is properly powered up.

Adjustable PL Bank VCCO Voltage FMC_VADJ

The carrier board VCCO voltage 'FMC_VADJ' supplying the PL IO-banks of the MPSoC is provided by DC-DC converter U8 and selectable by the pins 'FMC_VID0' ... 'FMC_VID2' of the System Controller CPLD U17.

FMC_VID2	FMC_VID1	FMC_VID0	FMC_VADJ Value
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V

Table 25: Bit patterns for fixed values of the FMC_VADJ voltage

Note: These pins of the DC-DC converter U8 are hard-wired to initialiy fix the voltage to 1.8V (see schematic).

Power Rails

Module Connector (B2B) Designator	VCC / VCCIO	Direction	Pins	Notes
J1	3.3V_MOD,	Out	Pin 151, 153, 155, 157, 159	-
	FMC_VADJ	Out	Pin 90, 120	-
	PL_1V8	In	Pin 91, 121	not connected
J2	3.3V_MOD	Out	Pin 138, 140, 142, 144, 153, 154, 155, 156, 157, 158, 159, 160	-
	PS_BATT	Out	Pin 125	-
	DDR_1V2	In	Pin 135	not connected
	PS_1V8	In	Pin 99	not connected
J3	3.3V_MOD	Out	Pin 157, 158, 159, 160	-
	FMC_VADJ	Out	Pin 15, 16	-
	1.8V	Out	Pin 43, 44	-

	PLL_3V3	Out	Pin 152	-
	SI_PLL_1V8	In	Pin 151	connected to testpoint
	PS_1V8	In	Pin 147, 148	not connected
J4	3.3V_MOD	Out	Pin 58, 59, 105, 106	-

Table 26: Power pin description of B2B Module Connector.

FAN Designator	VCC / VCCIO	Direction	Pins	Notes
J35	12V	Out	Pin 2	FAN2 Header
J26	12V	Out	Pin 2	FAN1 Header
J19	FAN_FMC	Out	Pin 2	FMC FAN Header

Table 27: Power pin description of FAN Connector

FMC Designator	VCC / VCCIO	Direction	Pins	Notes
J5	12V	Out	Pin C35, G37	-
	3.3V_PER	Out	Pin D32, D36, D38, D40, C39	-
	FMC_VADJ	Out	Pin E39, G39, H40, F40	adjustable FMC VCCIO

Table 28: Power pin description of FMC Connector

Main Power ATX + LED/RST Designator	VCC / VCCIO	Direction	Pins	Notes
J20	12V	In	Pin 10, 11	ATX-24 Connector
	5VSBIN	In	Pin 9	-
J25	12V	In	Pin 1	12V Power Jack **Attention**: optional, use only if ATX-24 Connector is not connected
J10	5V	Out	Pin 9	Power-/HD-LED/Reset Header

Table 29: Power pin description of ATX-24 Connector and Power-/HD-LED/Reset Header

PMOD Designator	VCC / VCCIO	Direction	Pins	Notes
P1	3.3V_PER	Out	Pin 6, 12	-
P2	3.3V_PER	Out	Pin 6, 12	-
P3	3.3V_PER	Out	Pin 6, 12	-

Table 30: Power pin description of PMOD Connector

XMOD / JTAG Designator	VCC / VCCIO	Direction	Pins	Notes
J12	3.3VSB	Out	Pin 5	XMOD Header

	1.8V	Out	Pin 6	-
J28	3.3VSB	Out	Pin 5, 6	XMOD Header
J30	3.3VSB	Out	Pin 1	ARM JTAG Header

Table 31: Power pin description of XMOD/JTAG Connector

Peripheral Designator	VCC / VCCIO	Direction	Pins	Notes
J23	3.3VSB	Out	Pin 1	PC Compatible BEEPER
J11	12V	Out	Pin A2, A3, B1, B2, B3	PCIe Connector
	3.3V_PCI	Out	Pin A9, A10, B8, B10	-
J29	5V	Out	Pin 5	CAN-Bus Header
J13	DP_TX_PWR	Out	Pin 20	Display-Port Connector
J14A	3.3V_PCI	Out	Pin T15, T16	SFP+ 2x1 Connector
J14B	3.3V_PCI	Out	Pin L15, L16	SFP+ 2x1 Connector
J15	3.3V_PER	Out	Pin 1, 10	FireFly Connector
J22	3.3V_PER	Out	Pin 1, 10	FireFly Connector
J7A	VBUS4	Out	Pin U1	USB3.0 Connector
J7B	VBUS3	Out	Pin U10	USB3.0 Connector
J8	VBUS1	Out	Pin 19	USB3.0 Header
	VBUS2	Out	Pin 1	-
J16	3.3V_SD_A	Out	Pin 4	MicroSD Card Socket
J27	3.3V_SD_B	Out	Pin 4	MMC Card Socket
B1	VBATT	In	Pin +	Battery Holder

Table 32: Power pin description of Peripherals' Connector

B2B connectors

5.2 x 7.6 cm UltraSoM+ modules use four Samtec Razor Beam LP Terminal Strip (ST5) on the bottom side.

- 4x REF-192552-02 (160-pins)
  - ST5 Mates with SS5

5.2 x 7.6 cm UltraSoM+ carrier use four Samtec Razor Beam LP Socket Strip (SS5) on the top side.

- 4x REF192552-01 (160-pins)
  - SS5 Mates with ST5

Features

- Board-to-Board Connector 160-pins, 80 contacts per row
- Ultrafine .0197" (0.50 mm) pitch
- Narrow body design saves space on board
- Lead style -03.5
- Samtec 28+ Gbps Solution
- Mates with: ST5
- Insulator Material: Liquid Crystal Polymer, schwarz
- Operating Temperature Range: -55°C bis +125°C
- Lead-Free Solderable: Yes

- RoHS Konform: Yes

Connector Stacking height

When using the standard type on baseboard and module, the mating height is 5 mm.

Other mating heights are possible by using connectors with a different height:

Order number	REF number	Samtec Number	Type	Contribution to stacking height	Comment
27219	REF192552-01	SS5-80-3.50-L-D-K-TR	Baseboard connector	3.5mm	Standard connector used on carrier
27018	REF-189545-02	SS5-80-3.00-L-D-K-TR	Baseboard connector	3 mm	Assembly option on request
27220	REF-192552-02	ST5-80-1.50-L-D-P-TR	Module connector	1.5 mm	Standard connector used on modules
27017	REF-189545-01	ST5-80-1.00-L-D-P-TR	Module connector	1 mm	Assembly option on request

Connectors.

The module can be manufactured using other connectors upon request.

Current Rating

Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

Connector Speed Ratings

The connector speed rating depends on the stacking height:

Stacking height	Speed rating
4 mm, Single-Ended	13GHz/26Gbps
4 mm, Differential	13.5GHz/27Gbps
5 mm, Single-Ended	13.5GHz/27Gbps
5 mm, Differential	20GHz/40 Gbps

Speed rating.

The SS5/ST5 series board-to-board spacing is currently available in 4mm (0.157"), 4.5mm (0.177") and 5mm (0.197") stack heights.

The data in the reports is applicable only to the 4mm and 5mm board-to-board mated connector stack height.

Manufacturer Documentation

File	Modified
PDF File hsc-report-sma_st5-ss5-04mm_web.pdf	30 05, 2017 by Susanne Kunath
PDF File hsc-report-sma_st5-ss5-05mm_web.pdf	30 05, 2017 by Susanne Kunath
PDF File REF-192552-01.pdf	13 11, 2017 by John Hartfiel
PDF File REF-192552-02.pdf	13 11, 2017 by John Hartfiel
PDF File ss5.pdf	13 11, 2017 by John Hartfiel

	PDF File ss5-st5.pdf	13 11, 2017 by John Hartfiel
	PDF File ss5-xx-x.xx-x-d-k-tr-mkt.pdf	13 11, 2017 by John Hartfiel
	PDF File st5.pdf	13 11, 2017 by John Hartfiel
	PDF File st5-xx-x.xx-x-d-p-tr-mkt.pdf	13 11, 2017 by John Hartfiel

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Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes / Reference Document
Power supply voltage (12V nominal)	11.4	12.6	V	ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) standard
Battery Voltage VBATT	-0.5	2	V	Xilinx DS925 data sheet
Voltage on pins of PMOD P2	-0.5	3.75	V	MachXO2 Family Data Sheet
Storage temperature (ambient)	-55	85	°C	Marvell 88E1512 datasheet

Table 33: Board absolute maximum ratings.

⚠ Assembly variants for higher storage temperature range are available on request.

Recommended Operating Conditions

Parameter	Min	Max	Unit	Notes / Reference Document
Power supply voltage (12V nominal)	11.4	12.6	V	ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) standard
Battery Voltage VBATT	1.2	1.5	V	Xilinx DS925 data sheet
Voltage on pins PMOD P2	3.135	3.6	V	MachXO2 Family Data Sheet

Table 34: Board recommended operating conditions.

⚠ Please check TRM TE0808 / TE0803 and Xilinx datasheet DS925 for complete list of absolute maximum and recommended operating ratings for the mounted UltraSoM+.

Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial grade: -40°C to +85°C.

Extended grade: 0°C to +85°C.

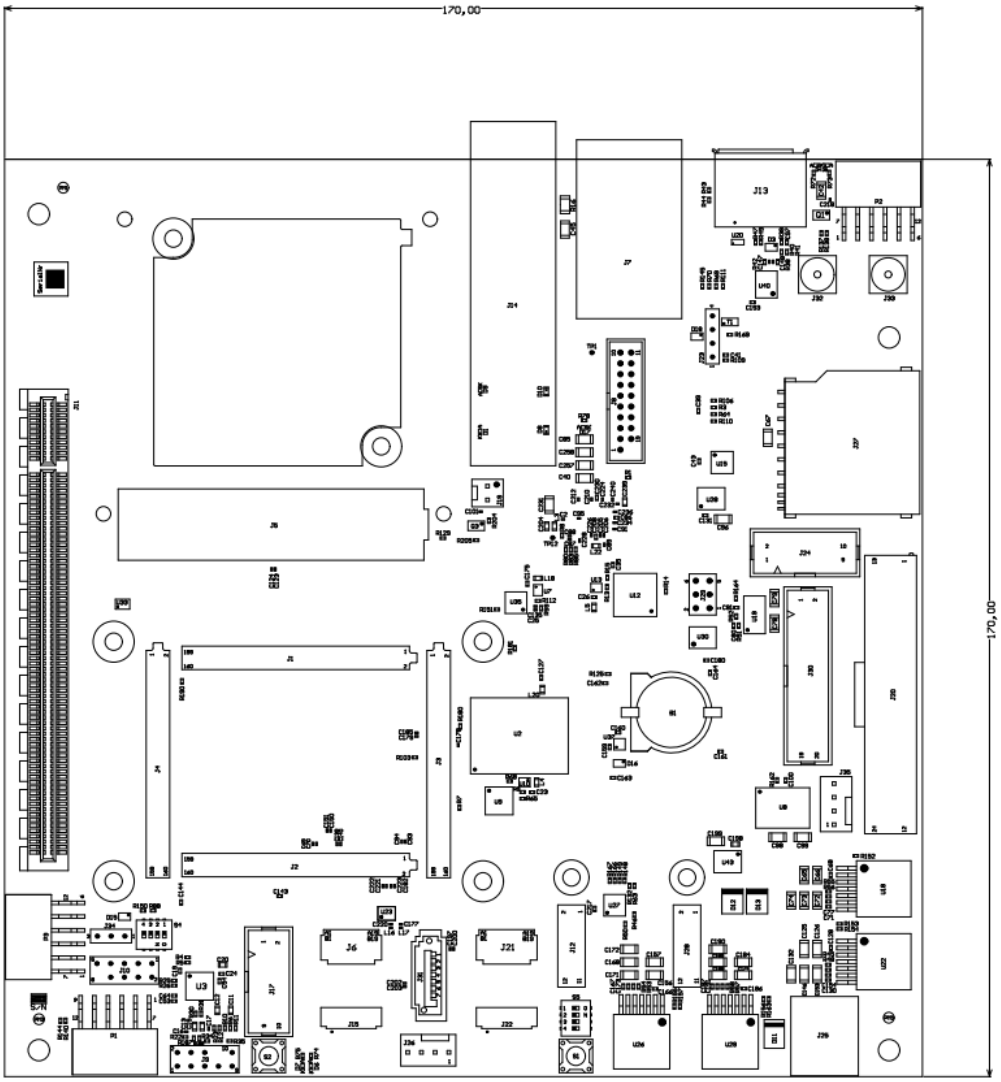
The carrier board itself is capable to be operated at industrial grade temperature range.

Please check the operating temperature range of the mounted UltraSOM+ modules, which determine the relevant operating temperature range of the overall system.

Physical Dimensions

- Module size: 170 mm × 170 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 5 mm
- PCB thickness: 1.844 mm ± 10%
- Highest part on PCB: approx. 32 mm. Please download the step model for exact numbers

All dimensions are given in millimeters.



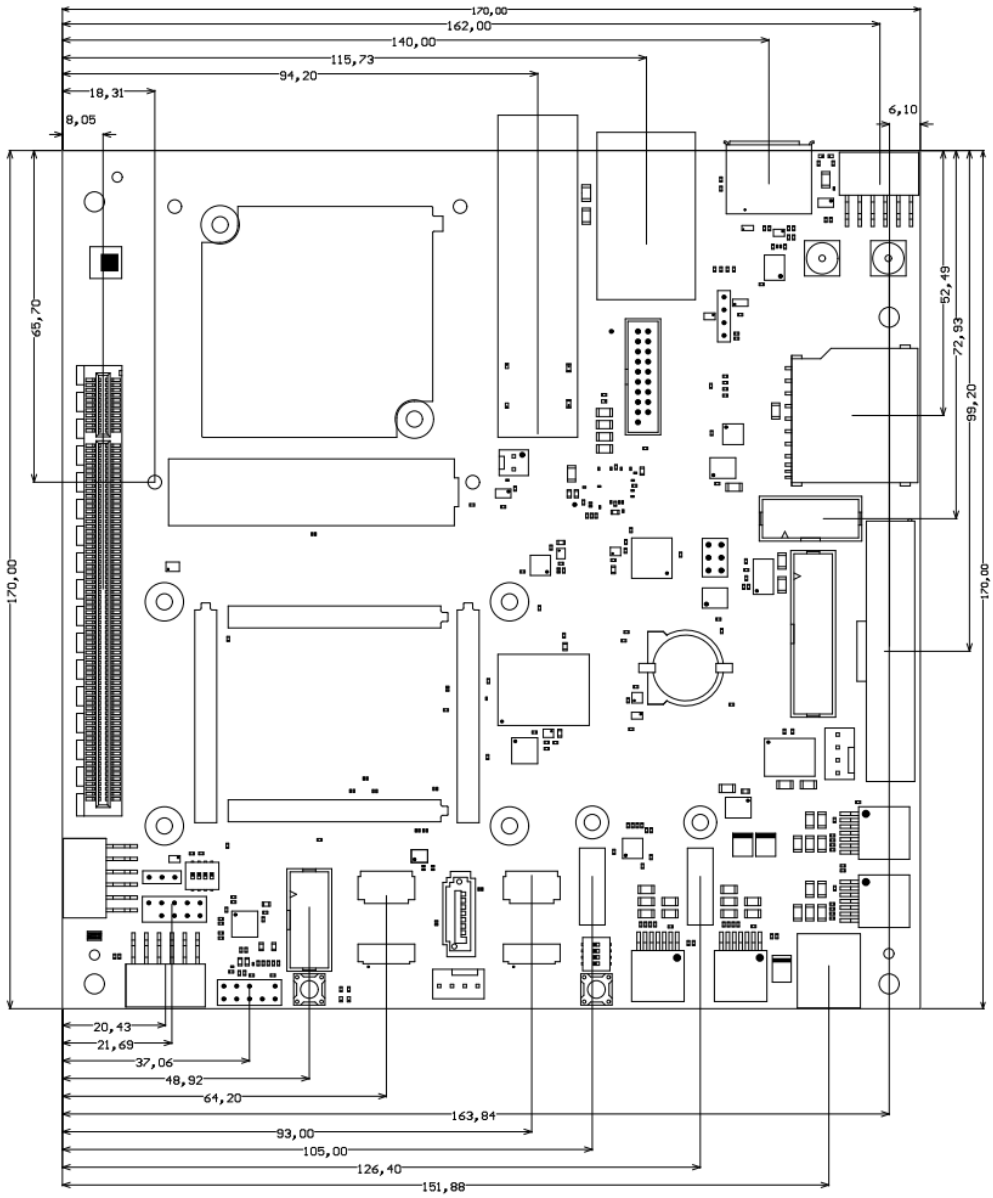


Figure 14: Board physical dimensions drawing.

Revision History

Hardware Revision History

Date	Revision	Notes	Link to PCN	Documentation Link
-	04	Current available board revision	-	TEBF0808-04
-	03	Second production release	-	TEBF0808-03

-	02	First production release	-	TEBF0808-02
-	01	Prototype	-	-

Table 35: Board hardware revision history.

Hardware revision number is written on the PCB board together with the module model number separated by the dash.

Figure 15: Board hardware revision number.

Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• System Controller links fixed
2019-09-03	v.96	Thomas Steffens	• correction EEPROM Designator • correction typ U25 CLK
2018-07-02	v.89	Martin Rohrmüller	• Typo
2018-05-31	v.88	John Hartfiel	• Typo correction Table 13 • Typo correction Table 9

2017-11-15	v.86	Ali Naseri	• DIP-switches section revised and updated
2017-11-13	v.82	Ali Naseri	• updated B2B connector max. current rating per pin
2017-11-13	v.80	John Hartfiel	• rework B2B section
2017-10-19	v.79	Ali Naseri	• added additionally MGT lanes information
2017-10-18	v.75	Ali Naseri	• added Power Rails section
2017-08-29	v.70	John Hartfiel	• update document change history • published
2017-08-28	v.69	Ali Naseri	• Initial document

--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• --

Table 36: Document change history.

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