TE0841 TRM

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Overview

The Trenz Electronic TE0841-02 is an industrial-grade 4 x 5 cm SoM integrating Xilinx Kintex UltraScale FPGA, 2 GByte of DDR4 SDRAM, 64 MByte QSPI Flash for configuration and operation and powerful switch-mode power supplies for all on-board voltages. Numerous configurable I/Os are provided via rugged high-speed strips. All this on a tiny footprint, smaller than a credit card size at very competitive price. All Trenz Electronic 4 x 5 cm SoMs are mechanically compatible.

Key Features

- Xilinx Kintex UltraScale FPGA (XCKU035 or XCKU040)
- 2 banks of 1024 MByte DDR4 SDRAM, 32bit wide memory interface(each DDR 16bit separate)
- 512 Mbit (64 MByte) QSPI Flash
- 3 x Samtec Razor Beam LSHM B2B, 260 terminals total
  - 60 x HR I/Os
  - 84 x HP I/Os
  - 8 x GTH transceiver lanes (TX/RX)
  - 2 x MGT external clock inputs
- Clocking
  - Si5338 - 4 output PLLs, GT and PL clocks
  - 200 MHz LVDS oscillator
- All power supplies on-board, single power source operation
- Evenly spread supply pins for optimized signal integrity
- Size: 40 x 50 mm
- 3 mm mounting holes for skyline heat spreader
- Rugged for industrial applications

Additional assembly options are available for cost or performance optimization upon request.

Block Diagram

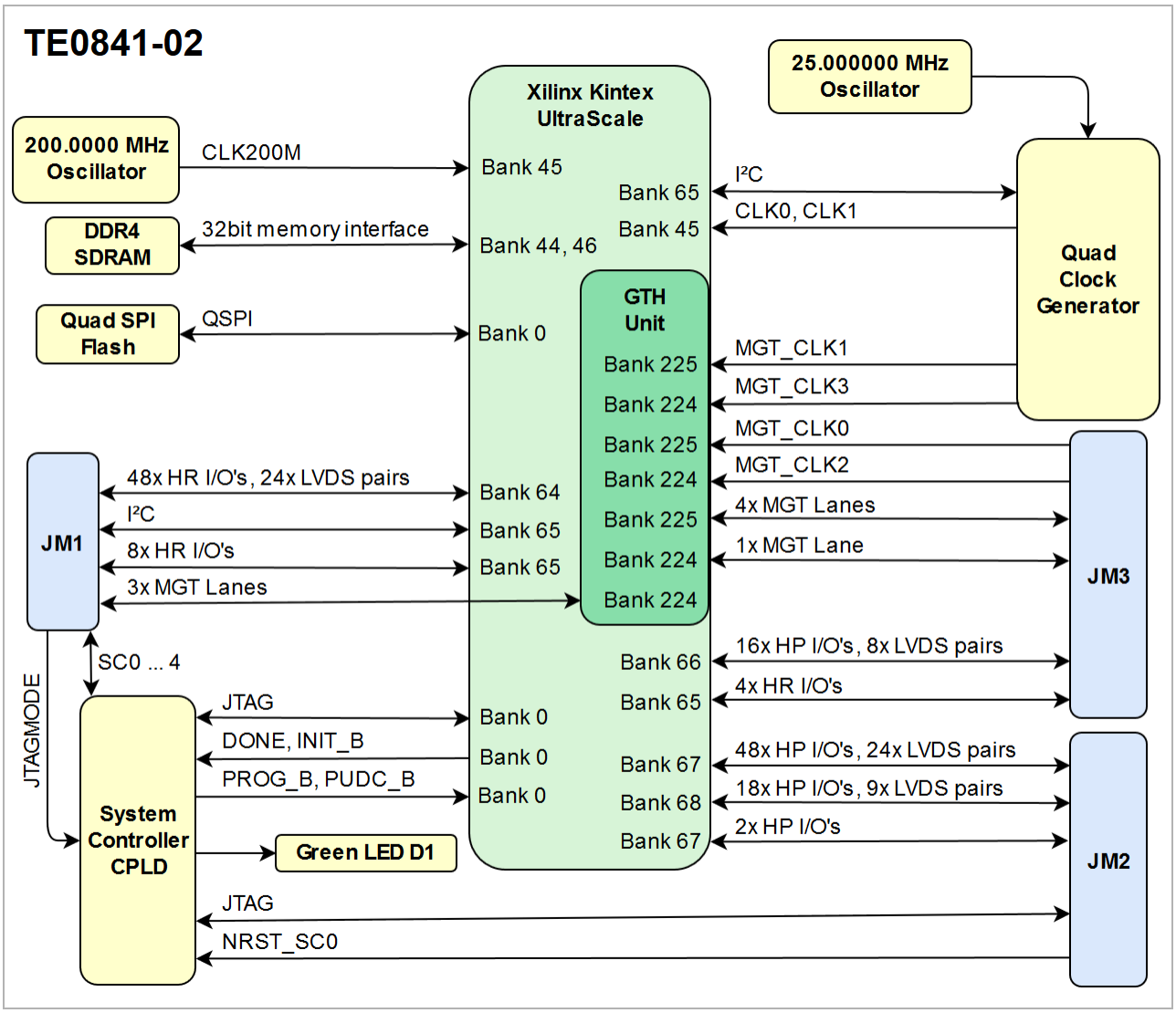


Figure 1: TE0841-02 block diagram

Main Components

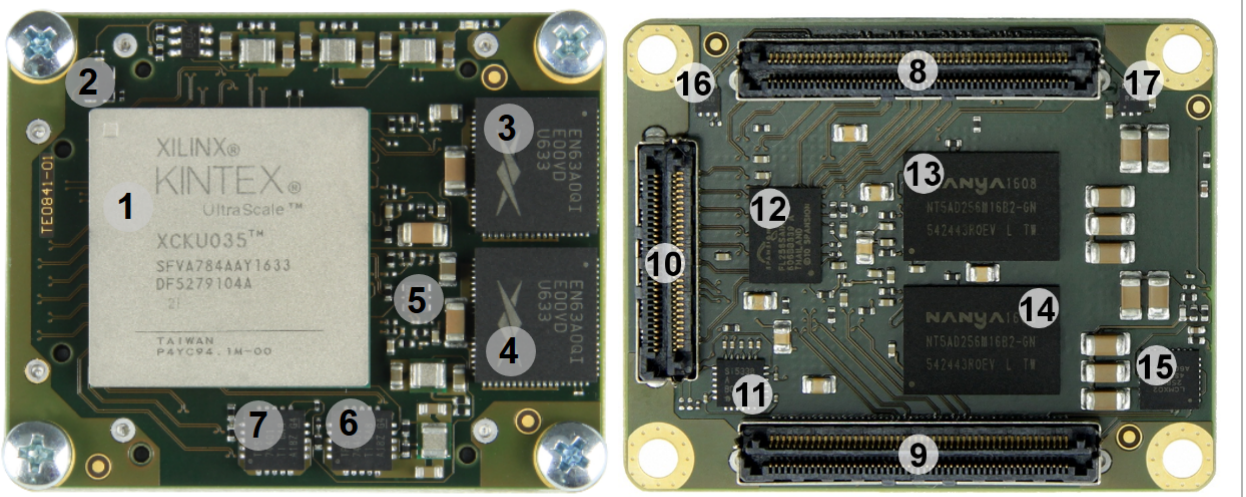


Figure 2: TE0841-02 main components

1. Xilinx Kintex UltraScale FPGA, U1
2. Ultra performance oscillator @25.000000 MHz, U3
3. 12A PowerSoC DC-DC converter (0.95V), U14
4. 12A PowerSoC DC-DC converter (0.95V), U7
5. Low-jitter precision LVDS oscillator @200.0000 MHz, U11
6. Low-dropout (LDO) linear regulator (MGTAVTT 1.20V), U8
7. Low-dropout (LDO) linear regulator (MGTAVCC 1.02V), U12
8. Samtec Razor Beam™ LSHM-150 B2B connector, JM1
9. Samtec Razor Beam™ LSHM-150 B2B connector, JM2
10. Samtec Razor Beam™ LSHM-130 B2B connector, JM3
11. Programmable quad clock generator, U2
12. 64 MByte QSPI Flash, U6
13. 8 Gbit DDR4 SDRAM, U4
14. 8 Gbit DDR4 SDRAM, U5
15. System Controller CPLD, U18**Programmable Clock Generator**
16. Low-dropout (LDO) linear regulator (MGTAUX), U9
17. Ultra-low power low-dropout (LDO) regulator (VBATT), U19

Initial Delivery State

Storage device name	Content	Notes
System Controller CPLD	Default firmware	-
OTP Flash area	Empty	Not programmed
Quad clock generator OTP area	programmed	on PCB REV02 and newer

Table 1: TE0841-02 module initial delivery state of programmable on-board devices

Boot Process

By default the configuration mode pins M[2:0] of the FPGA are set to QSPI mode (Master SPI), hence the FPGA is configured from serial NOR flash at system start-up. The JTAG interface of the module is provided for storing the initial FPGA configuration data to the QSPI flash memory.

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

I/O signals connected to the SoCs I/O bank and B2B connector:

FPGA Bank	Type	B2B Connector	I/O Signal Count	Bank VCCO Voltage	Notes
64	HR	JM1	48 IO's, 24 LVDS pairs	B64_VCCO	Supplied by the carrier board
65	HR	JM1	8 IO's	3.3V	On-module power supply
65	HR	JM3	4 IO's	3.3V	On-module power supply
66	HP	JM3	16 IO's, 8 LVDS pairs	B66_VCCO	Supplied by the carrier board
67	HP	JM2	48 IO's, 24 LVDS pairs	B67_VCCO	Supplied by the carrier board
67	HP	JM2	2 IO's	B67_VCCO	Supplied by the carrier board
68	HP	JM2	18 IO's, 9 LVDS pairs	B68_VCCO	Supplied by the carrier board

Table 2: General overview of FPGA's PL I/O signals connected to the B2B connectors

For detailed information about the pin out, please refer to the Pin-out Tables.

MGT Lanes

MGT (Multi Gigabit Transceiver) lane consists of one transmit and one receive (TX/RX) differential pairs, two signals each or four signals total per one MGT lane. Following table lists lane number, MGT bank number, transceiver type, signal schematic name, board-to-board pin connection and FPGA pins connection:

Lane	Bank	Type	Signal Name	B2B Pin	FPGA Pin
0	225	GTH	• MGT_RX0_P • MGT_RX0_N • MGT_TX0_P • MGT_TX0_N	• JM3-8 • JM3-10 • JM3-7 • JM3-9	• MGTHRXP0_225, Y2 • MGTHRXN0_225, Y1 • MGTHTXP0_225, AA4 • MGTHTXN0_225, AA3
1	225	GTH	• MGT_RX1_P • MGT_RX1_N • MGT_TX1_P • MGT_TX1_N	• JM3-14 • JM3-16 • JM3-13 • JM3-15	• MGTHRXP1_225, V2 • MGTHRXN1_225, V1 • MGTHTXP1_225, W4 • MGTHTXN1_225, W3
2	225	GTH	• MGT_RX2_P • MGT_RX2_N • MGT_TX2_P • MGT_TX2_N	• JM3-20 • JM3-22 • JM3-19 • JM3-21	• MGTHRXP2_225, T2 • MGTHRXN2_225, T1 • MGTHTXP2_225, U4 • MGTHTXN2_225, U3
3	225	GTH	• MGT_RX3_P • MGT_RX3_N • MGT_TX3_P • MGT_TX3_N	• JM3-26 • JM3-28 • JM3-25 • JM3-27	• MGTHRXP3_225, P2 • MGTHRXN3_225, P1 • MGTHTXP3_225, R4 • MGTHTXN3_225, R3

4	224	GTH	• MGT_RX4_P • MGT_RX4_N • MGT_TX4_P • MGT_TX4_N	• JM1-12 • JM1-10 • JM1-6 • JM1-4	• MGTHRXP0_224, AH2 • MGTHRXN0_224, AH1 • MGTHTXP0_224, AG4 • MGTHTXN0_224, AG3
5	224	GTH	• MGT_RX5_P • MGT_RX5_N • MGT_TX5_P • MGT_TX5_N	• JM1-24 • JM1-22 • JM1-18 • JM1-16	• MGTHRXP1_224, AF2 • MGTHRXN1_224, AF1 • MGTHTXP1_224, AF6 • MGTHTXN1_224, AF5
6	224	GTH	• MGT_RX6_P • MGT_RX6_N • MGT_TX6_P • MGT_TX6_N	• JM1-27 • JM1-25 • JM1-19 • JM1-17	• MGTHRXP2_224, AD2 • MGTHRXN2_224, AD1 • MGTHTXP2_224, AE4 • MGTHTXN2_224, AE3
7	224	GTH	• MGT_RX7_P • MGT_RX7_N • MGT_TX7_P • MGT_TX7_N	• JM3-2 • JM3-4 • JM3-1 • JM3-3	• MGTHRXP3_224, AB2 • MGTHRXN3_224, AB1 • MGTHTXP3_224, AC4 • MGTHTXN3_224, AC3

Table 3: FPGA to B2B connectors routed MGT lanes overview

Below are listed MGT banks reference clock sources:

Clock signal	Bank	Source	FPGA Pin	Notes
MGT_CLK0_P	225	B2B, JM3-33	MGTREFCLK0P_225, Y6	Supplied by the carrier board.
MGT_CLK0_N		B2B, JM3-31	MGTREFCLK0N_225, Y5	
MGT_CLK1_P	225	U2, CLK1B	MGTREFCLK1P_225, V6	On-board Si5338A.
MGT_CLK1_N		U2, CLK1A	MGTREFCLK1N_225, V5	
MGT_CLK2_P	224	B2B, JM3-34	MGTREFCLK2P_224, AD6	Supplied by the carrier board.
MGT_CLK2_N		B2B, JM3-32	MGTREFCLK2N_224, AD5	
MGT_CLK3_P	224	U2, CLK2B	MGTREFCLK3P_224, AB6	On-board Si5338A.
MGT_CLK3_N		U2, CLK2B	MGTREFCLK3N_224, AB5	

Table 4: MGT reference clock sources

JTAG Interface

JTAG access to the Xilinx Kintex UltraScale FPGA is available through B2B connector JM2.

JTAG Signal	B2B Connector Pin
TMS	JM2-93
TDI	JM2-95
TDO	JM2-97
TCK	JM2-99

Table 5: JTAG interface signals

⚠ JTAGMODE pin 89 in B2B connector JM1 should be set low or grounded for normal operation. Set this pin high for SC CPLD update via JTAG interface.

System Controller CPLD I/O Pins

Special purpose pins are connected to the System Controller CPLD and have following default configuration:

Pin Name	SC CPLD Direction	Function	Default Configuration
JTAGMODE	Input	JTAG select	Low for normal operation.
nRST_SC0	Input	Reset	Low active board reset input
SC1	-	-	not currently used ('BOOTMODE' in default B2B pin out')
SC2	Input / Output	-	Power good signal ('PGOOD' in default B2B pin out)
SC3	Input	-	Power enable pin ('EN1' in default B2B pin out)
SC4	-	-	not currently used ('NOSEQ' in default B2B pin out')
F_TCK	Output	JTAG signals between SC CPLD and FPGA	B2B JTAG signals are forwarded to the FPGA through SC CPLD.
F_TMS	Output		
F_TDI	Output		
F_TDO	Input		
TCK	Input	JTAG signals between SC CPLD and B2B connector	Program FPGA or SC CPLD depending on pin JTAGMODE.
TMS	Input		
TDI	Input		
TDO	Output		
PROG_B	Output	FPGA configuration	PL configuration reset signal.
DONE	Input	FPGA configuration done	PL configuration completed.
PUDC_B	Output	Pull up during configuration	PL I/O's are 3-stated until configuration of the FPGA completes.
INIT_B	Input	Initialization done	Low active FPGA initialization pin or configuration error signal.
EN_PL	Input	Enable PL Power DC-DC converters	Set to contant logical high.
CPLD_IO	Output	user I/O	Connected to FPGA Bank 45, pin P28.

Table 6: System Controller CPLD I/O pins

For detailed function of the pins and signals, the internal signal assignment and the implemented logic, look to the Wiki reference page of the module's SC CPLD or into its bitstream file.

Quad SPI Interface

Quad SPI interface is connected to the FPGA configuration bank 0.

Signal Name	QSPI Flash Memory U6 Pin	FPGA Pin
SPI_CS	C2	RDWR_FCS_B_0, AH7
SPI_D0	D3	D00_MOSI_0, AA7
SPI_D1	D2	D01_DIN_0, Y7

SPI_D2	C4	D02_0, U7
SPI_D3	D4	D03_0, V7
SPI_CLK	B2	CCLK_0, V11

Table 7: Quad SPI interface signals and connections

I2C Interface

On-module I²C interface is routed from PL bank 65 I/O pins (PLL_SCL and PLL_SDA) to the I²C interface of Si5338 PLL quad clock generator U2, also two further pins of bank 65 can be used as external I²C interface of the modue:

I²C Interface	Schematic net names	Connected to	I²C Address	Notes
PL bank 65 I/O	'PLL_SCL', pin AB20 'PLL_SDA' pin AB19	Si5338 U2, pin 12 Si5338 U2, pin 19	0x70	default address
PL bank 65 I/O	'B65_SCL', pin Y19 'B65_SDA', pin AA19	B2B JM1, pin 95 B2B JM1, pin 93	-	

Table 8: I^2C slave device addresses

On-board Peripherals

System Controller CPLD

The System Controller CPLD (U2) is provided by Lattice Semiconductor LCMXO2-256HC (MachXO2 Product Family). The SC-CPLD is the central system management unit where essential control signals are logically linked by the implemented logic in CPLD firmware, which generates output signals to control the system, the on-board peripherals and the interfaces. Interfaces like JTAG and I^2C between the on-board peripherals and to the FPGA module are by-passed, forwarded and controlled by the System Controller CPLD.

Other tasks of the System Controller CPLD are the monitoring of the power-on sequence and to display the programming state of the FPGA module.

For detailed information, refer to the reference page of the SC CPLD firmware of this module.

DDR Memory

By default TE0841 module has two K4A8G165WB-BIRC DDR4 SDRAM chips arranged into 32-bit wide memory bus providing total of 2 GBytes of on-module RAM. Different memory sizes are available optionally.

Quad SPI Flash Memory

On-module QSPI flash memory (U6) on the TE0841-01 is provided by Micron Serial NOR Flash Memory N25Q512A11G1240E with 512-Mbit (64 MByte) storage capacity. This non volatile memory is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.

SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash during power-on. By default this bit is set to high at the manufacturing plant.

Programmable Clock Generator

There is a Silicon Labs I^{2}C programmable quad PLL clock generator on-board (Si5338A, U2) to generate various reference clocks for the module.

Si5338A Pin	Signal Name / Description	Connected to	Direction	Note
IN1	-	not connected	Input	not used
IN2	-	GND	Input	not used
IN3	Reference input clock	U3, pin 3	Input	25.000000 MHz oscillator, Si8208AI
IN4	-	GND	Input	I^{2}C slave device address LSB.
IN5	-	not connected	Input	not used
IN6	-	GND	Input	not used
CLK0A	CLK1_P	U1, R23	Output	FPGA bank 45, default 100MHz*
CLK0B	CLK1_N	U1, P23		
CLK1A	MGT_CLK1_N	U1, V5	Output	FPGA MGT bank 225 reference clock, default 125MHz*
CLK1B	MGT_CLK1_P	U1, V6		
CLK2A	MGT_CLK3_N	U1, AB5	Output	FPGA MGT bank 224 reference clock, default 156,25MHz*
CLK2B	MGT_CLK3_P	U1, AB6		
CLK3A	CLK0_P	U1, pin T24	Output	FPGA bank 45, default 156,25MHz*
CLK3B	CLK0_N	U1, pin T25		

Table 9: Programmable quad PLL clock generator inputs and outputs, *PCB REV01 is not programmed

Oscillators

The FPGA module has following reference clocking signals provided by external baseboard sources and on-board oscillators:

Clock Source	Frequency	Signal Name	Clock Destination	Notes
U3, SiT8208AI	25.000000 MHz	CLK	Si5338A PLL U2, pin 3 (IN3)	-
U11, DSC1123DL5	200.0000 MHz	CLK200M_P	FPGA bank 45, pin R25	Enable by FPGA bank 65, pin AF24
		CLK200M_N	FPGA bank 45, pin R26	Signal: 'ENOSC'

Table 10: Reference clock signals

On-board LEDs

LED	Color	Connected to	Description and Notes
D1	Green	System Controller CPLD, bank 3	Exact function is defined by SC CPLD firmware.

Table 11: On-board LEDs

Power and Power-On Sequence

Power Consumption

The maximum power consumption of a module mainly depends on the design running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input	Typical Current
VIN	TBD*
3.3VIN	TBD*

Table 12: Typical power consumption

* TBD - To Be Determined soon with reference design setup.

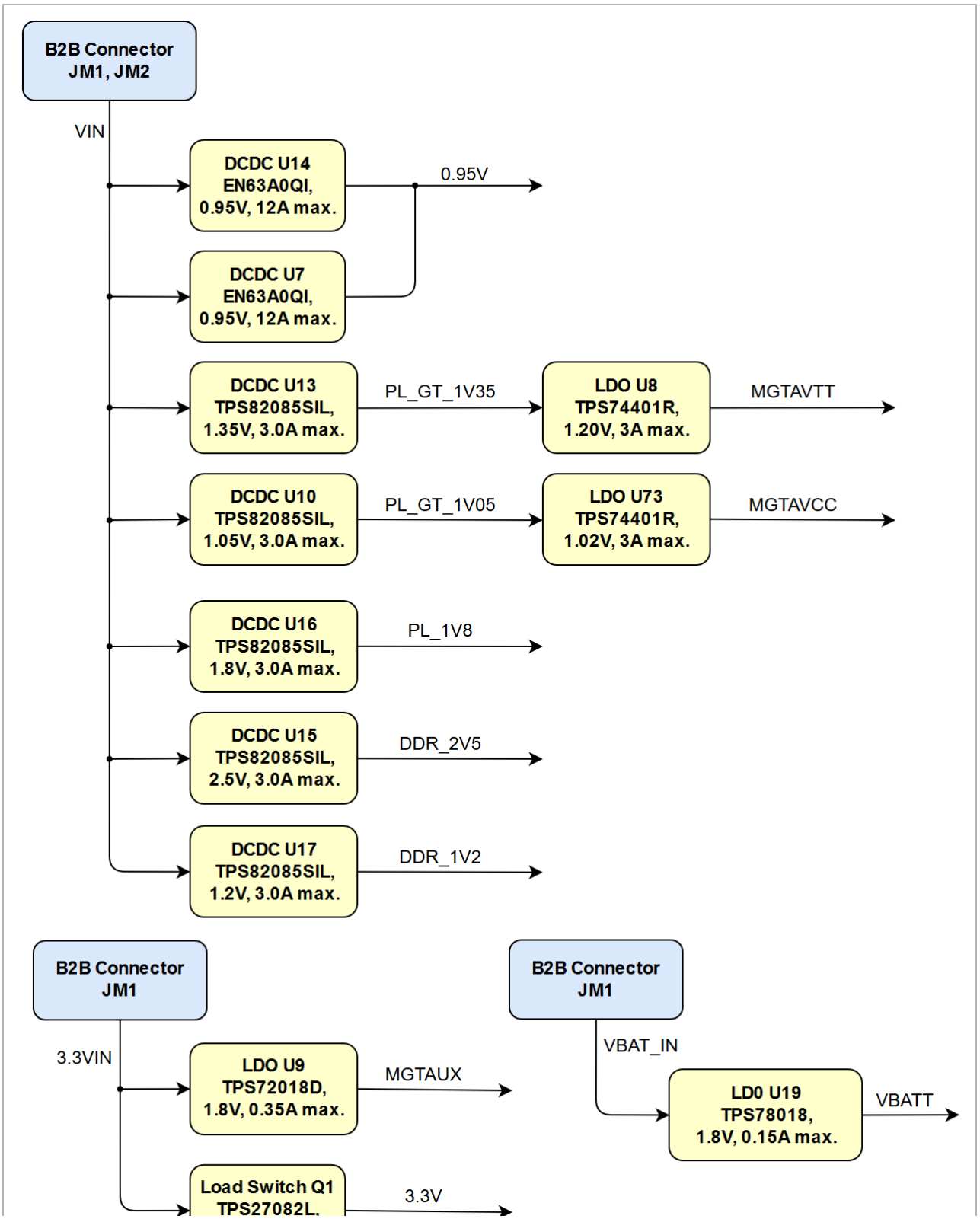
Single 3.3V power supply with minimum current capability of 4A for system startup is recommended.

For the lowest power consumption and highest efficiency of the on-board DC-DC regulators it is recommended to power the module from one single 3.3V supply. All input power supplies should have a nominal value of 3.3V. Although the input power supplies can be powered up in any order, it is recommended to power them up simultaneously.



To avoid any damage to the module, check for stabilized on-board voltages should be carried out (i.e. power good and enable signals) before powering up any FPGA's I/O bank voltages VCCO_x. All I/Os should be tri-stated during power-on sequence.

Power Distribution Dependencies


B2B Connector
JM1, JM2
VIN
DCDC U14
EN63A0QI,
0.95V, 12A max.
0.95V
DCDC U7
EN63A0QI,
0.95V, 12A max.
DCDC U13
TPS82085SIL,
1.35V, 3.0A max.
PL_GT_1V35
LDO U8
TPS74401R,
1.20V, 3A max.
MGTAVTT
DCDC U10
TPS82085SIL,
1.05V, 3.0A max.
PL_GT_1V05
LDO U73
TPS74401R,
1.02V, 3A max.
MGTAVCC
DCDC U16
TPS82085SIL,
1.8V, 3.0A max.
PL_1V8
DCDC U15
TPS82085SIL,
2.5V, 3.0A max.
DDR_2V5
DCDC U17
TPS82085SIL,
1.2V, 3.0A max.
DDR_1V2
B2B Connector
JM1
3.3VIN
LDO U9
TPS72018D,
1.8V, 0.35A max.
MGTAUX
Load Switch Q1
TPS27082L,
3.3V
B2B Connector
JM1
VBAT_IN
LD0 U19
TPS78018,
1.8V, 0.15A max.
VBATT

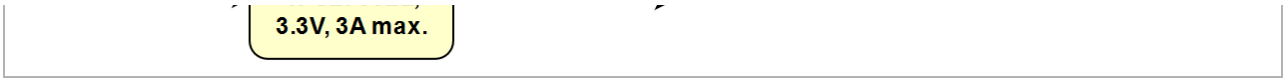


Figure 3: TE0841-02 Power Distribution Diagram

See also Xilinx datasheet DS892 for additional information. User should also check related base board documentation when intending base board design for TE0841 module.

Power-On Sequence

The TE0841 SoM meets the recommended criteria to power up the Xilinx FPGA properly by keeping a specific sequence of enabling the on-board DC-DC converters dedicated to the particular functional units of the FPGA chip and powering up the on-board voltages.

Following diagram clarifies the sequence of enabling the particular on-board voltages, which will power-up in descending order as listed in the blocks of the diagram:

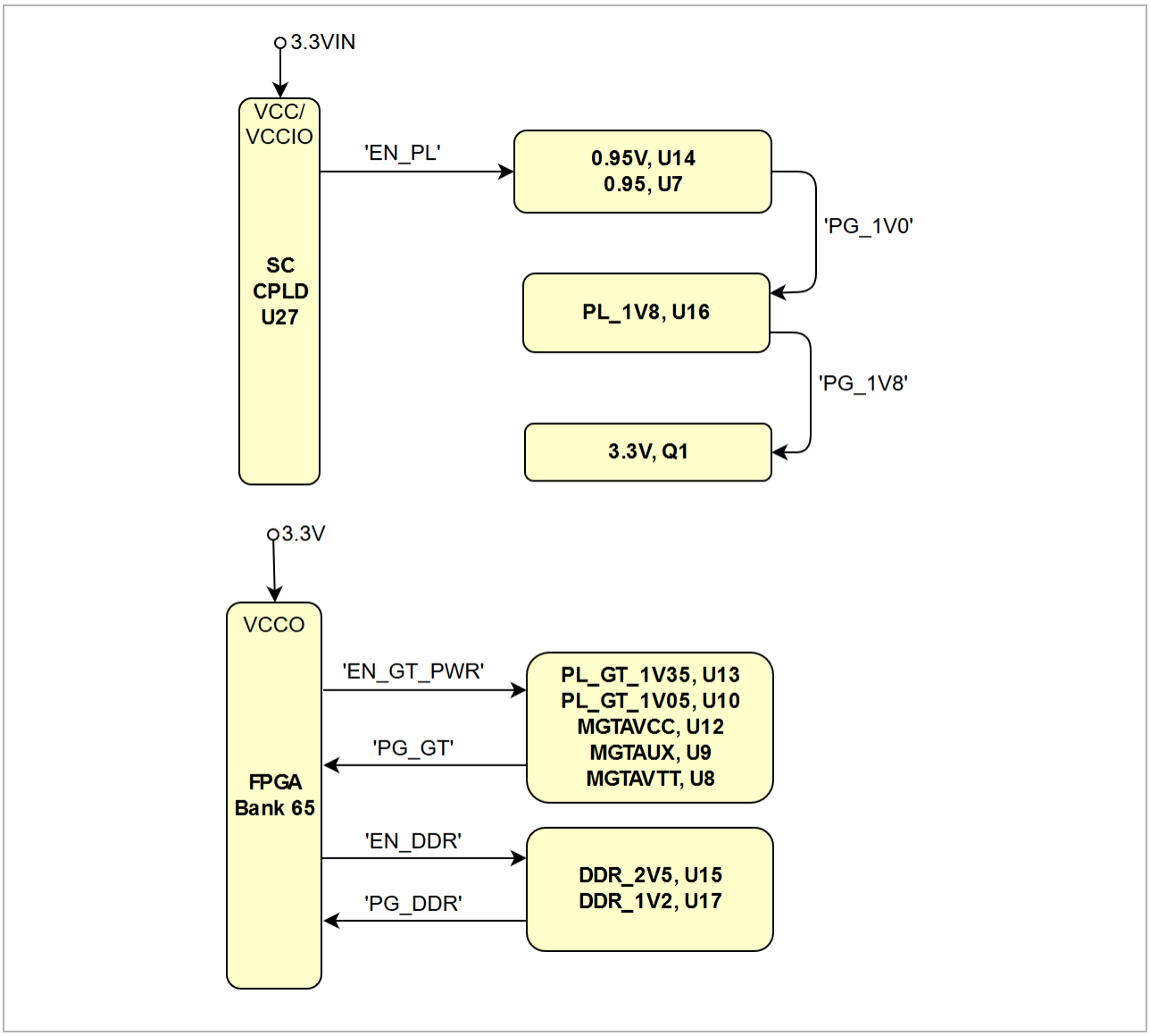


Figure 4: TE0841-02 Power-On Sequence Diagram

Power Rails

Power Rail Name	B2B JM1 Pins	B2B JM2 Pins	Input/Output	Notes
VIN	1, 3, 5	2, 4, 6, 8	Input	Supply voltage.
3.3VIN	13, 15	-	Input	Supply voltage.
B64_VCO	9, 11	-	Input	HR (High Range) bank voltage.
B66_VCO	-	1, 3	Input	HP (High Performance) bank voltage.
B67_VCO	-	7, 9	Input	HP (High Performance) bank voltage.

B68_VCO	-	5	Input	HP (High Performance) bank voltage.
VBAT_IN	79	-	Input	RTC battery supply voltage.
3.3V	-	10, 12, 91	Output	Module on-board 3.3V voltage level.

Table 13: Module power rails

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

Bank Voltages

Bank	Schematic Name	Voltage	Voltage Range
0 (config)	PL_1.8V	1.8V	-
44 HP	DDR_1V2	1.2V	HP: 1.2V to 1.8V
45 HP	PL_1.8V	1.8V	HP: 1.2V to 1.8V
46 HP	DDR_1V2	1.2V	HP: 1.2V to 1.8V
64 HR	B64_VCO	user	HR: 1.2V to 3.3V
65 HR	3.3V	3.3V	HR: 1.2V to 3.3V
66 HP	B66_VCO	user	HP: 1.2V to 1.8V
67 HP	B67_VCO	user	HP: 1.2V to 1.8V
68 HP	B68_VCO	user	HP: 1.2V to 1.8V

Table 14: Module PL I/O bank voltages

Board to Board Connector



These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three Samtec Razor Beam LSHM connectors on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm

24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

Connectors.

The module can be manufactured using other connectors upon request.

Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

Speed rating.

Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

Manufacturer Documentation

File	Modified
PDF File hsc-report_lshm-lshm-05mm_web.pdf High speed test report	07 04, 2016 by Thorsten Trenz
PDF File lshm_dv.pdf LSHM catalog page	07 04, 2016 by Thorsten Trenz
PDF File LSHM-1XX-XX.X-X-DV-A-X-X-TR-FOOTPRINT(1).pdf Recommended layout and stencil drawing	07 04, 2016 by Thorsten Trenz
PDF File LSHM-1XX-XX.X-XX-DV-A-X-X-TR-MKT.pdf Technical drawing	07 04, 2016 by Thorsten Trenz
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PDF File REF-189017-02.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File TC0923--2523_report_Rev_2_qua.pdf Design qualification test report	07 04, 2016 by Thorsten Trenz
PDF File tc0929--2611_qua(1).pdf Shock and vibration report	07 04, 2016 by Thorsten Trenz

Download All

Variants Currently In Production

See also the current available variants on the Trenz Electronic shop page

Trenz shop TE0841 overview page	
English page	German page

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	-0.3	6.0	V	EN63A0QI, TPS74401RGW datasheets
3.3VIN supply voltage	-0.1	3.4	V	Xilinx datasheet DS892 (HR Bank VCCO)
VBAT_IN	-0.3	6.0	V	TPS780xx datasheet
Supply voltage for HR I/O banks (VCCO)	-0.500	3.400	V	Xilinx datasheet DS892
Supply voltage for HP I/O banks (VCCO)	-0.500	2.000	V	Xilinx datasheet DS892
I/O input voltage for HR I/O banks	-0.400	VCCO + 0.550	V	Xilinx datasheet DS892
I/O input voltage for HP I/O banks	-0.550	VCCO + 0.550	V	Xilinx datasheet DS892
I/O input voltage for SC CPLD U18	-0.5	3.75	V	LCMXO2-256HC datasheet
GTH and GTY transceiver reference clocks absolute input voltage (MGT_CLK0, MGT_CLK2)	-0.500	1.320	V	Xilinx datasheet DS892
GTH and GTY transceiver receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	-0.500	1.260	V	Xilinx datasheet DS892
Storage temperature	-40	+100	°C	SML-P11 LED datasheet

Table 16: Module absolute maximum ratings

⚠ Assembly variants for higher storage temperature range are available on request.

Recommended Operating Conditions

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	3.3	5.5	V	TPS82085SIL, TPS74401RGW datasheet
3.3VIN supply voltage	3.3	3.4	V	Xilinx datasheet DS892 (HR Bank VCCO)

VBAT_IN	2.2	5.5	V	TPS780xx datasheet
Supply voltage for HR I/O banks (VCCO)	1.140	3.400	V	Xilinx datasheet DS892
Supply voltage for HP I/O banks (VCCO)	0.950	1.890	V	Xilinx datasheet DS892
I/O input voltage for HR I/O banks	–0.200	VCCO + 0.20	V	Xilinx datasheet DS892
I/O input voltage for HP I/O banks	–0.200	VCCO + 0.20	V	Xilinx datasheet DS892
I/O input voltage for SC CPLD U18	-0.3	3.6	V	LCMXO2-256HC datasheet
Industrial Module Operating Temperature Range	-40	85	°C	Xilinx datasheet DS892
Commercial Module Operating Temperature Range	0	85	°C	Xilinx DS892, Silicon Labs Si5338 datasheet

Table 17: Module recommended operating conditions

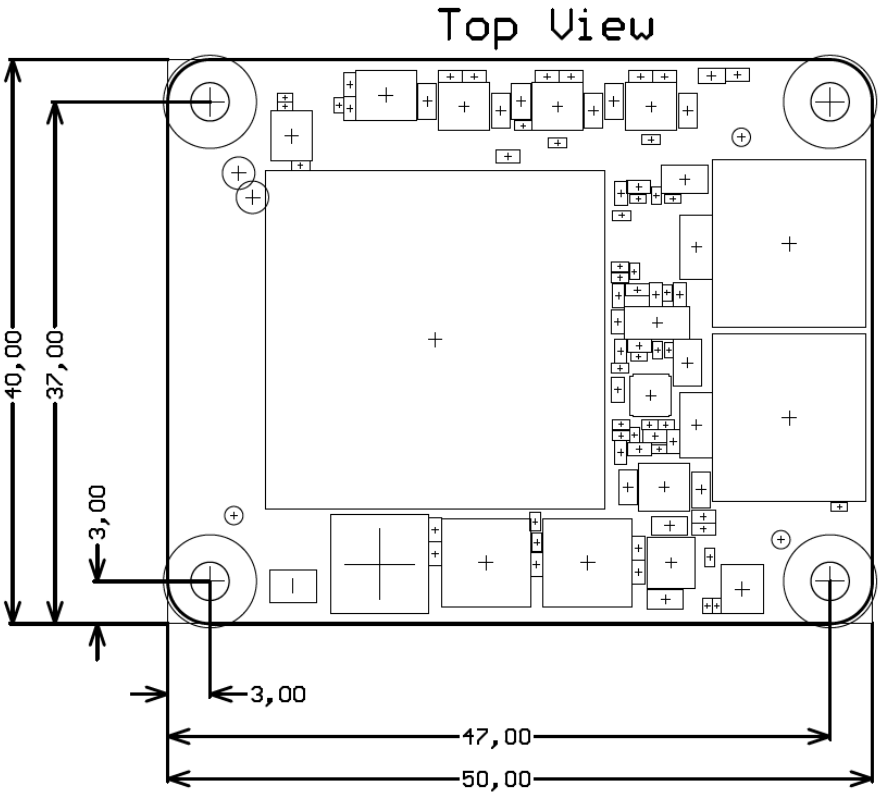
Module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

⚠ Please check also Xilinx datasheet DS892 for complete list of absolute maximum and recommended operating ratings.

Physical Dimensions

- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8 mm.
- PCB thickness: 1.65 mm.
- Highest part on PCB: approximately 3 mm. Please download the step model for exact numbers.

All dimensions are given in millimeters.


Top View
40,00
37,00
3,00
3,00
47,00
50,00

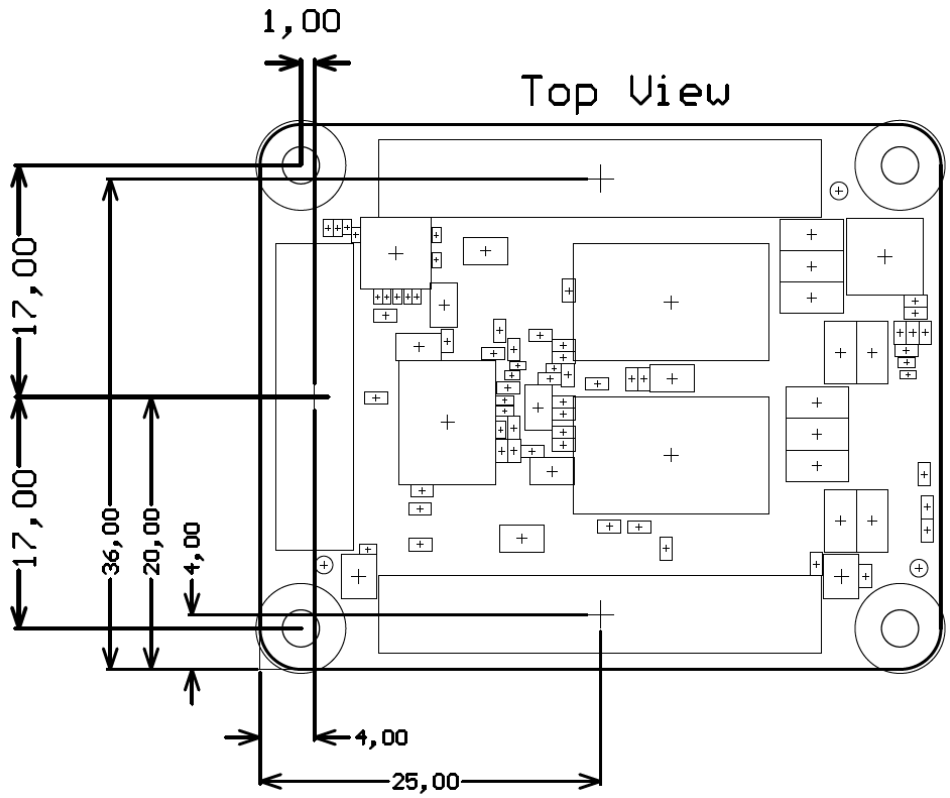


Figure 5: Module physical dimensions drawing

Revision History

Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
2018-05-11	02	current available board revision	PCN-20180511	TE0841-02
2015-12-09	01	First production release	-	TE0841-01

Table 18: Module hardware revision history

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

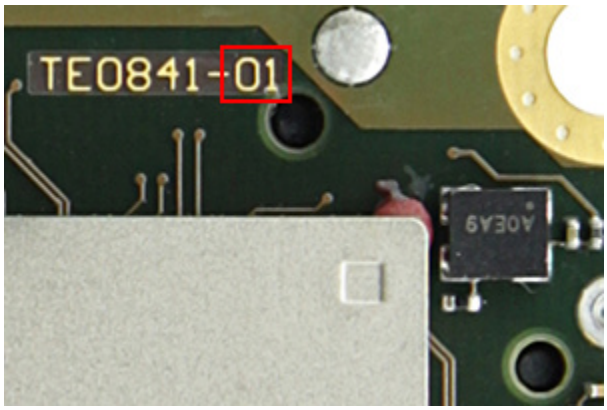


Figure 6: Module hardware revision number

Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• correction delivery section • update key features, document history
2018-08-07	v.69	Ali Naseri	• updated pictures main components
2018-07-13	v.68	Ali Naseri	• PCB REV02
2018-07-10	v.58	John Hartfiel	• update links
2018-03-13	v.57	Jan Kumann, Ali Naseri	• Initial document.

--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• --

Table 18: Document change history

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

02 Sept 2017