SC0911 CPLD

Table of contents

Overview

Firmware for PCB CPLD with designator U27. CPLD Device in Chain: LCMX02-7000HC

Feature Summary

- Power Management
- Reset Management
- Boot Mode
- FAN Control
- LED Control
- FMC JTAG
- CAN
- PJTAG

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	Schematic Sheet	PCB < REV03
3V3SB		B16	3.3V	CPLD Programm Pin connected with pullup	SC1	
3V3SB		B20	3.3V	CPLD initn Pin connected with pullup	SC1	
3V3SB		C29	3.3V	CPLD Done Pin connected with pullup	SC1	
A_LA06_SC_N		C22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA06_SC_P		B22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA07_SC_N		F20	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA07_SC_P		E22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA08_SC_N		E21	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA08_SC_P		D22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA09_SC_N		G22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA09_SC_P		G21	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA10_SC_N		G17	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA10_SC_P		H16	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA11_SC_N		K22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA11_SC_P		K21	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA12_SC_N		H20	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA12_SC_P		H21	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA13_SC_N		L22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA13_SC_P		L21	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA14_SC_N		G16	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA14_SC_P		F18	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA15_SC_N		D19	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA15_SC_P		C21	FMC_AF_1.8V	/ currently_not_used	SC2	

A_LA16_SC_N		M21	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA16_SC_P		M22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA17_SC_N		N21	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA17_SC_P		N22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA18_SC_N		G19	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA18_SC_P		F19	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA19_SC_N		E19	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA19_SC_P		D20	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA20_SC_N		E20	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA20_SC_P		D21	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA21_SC_N		J17	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA21_SC_P		J16	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA22_SC_N		J19	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA22_SC_P		J18	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA23_SC_N		G18	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA23_SC_P		H17	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA24_SC_N		R22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA24_SC_P		P20	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA25_SC_N		K16	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA25_SC_P		K17	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA26_SC_N		K18	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA26_SC_P		L20	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA27_SC_N		K20	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA27_SC_P		J21	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA28_SC_N		U22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA28_SC_P		T20	FMC_AF_1.8V	/ currently_not_used	SC2	

A_LA29_SC_N		T22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA29_SC_P		T21	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA30_SC_N		W22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA30_SC_P		V21	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA31_SC_N		V22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA31_SC_P		U20	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA32_SC_N		Y20	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA32_SC_P		Y21	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA33_SC_N		AA22	FMC_AF_1.8V	/ currently_not_used	SC2	
A_LA33_SC_P		Y22	FMC_AF_1.8V	/ currently_not_used	SC2	
B64_T1	out	D3	1.8V	reserved for RGPIO / currently_not_implemented	SC2	
B64_T2	in	C3	1.8V	reserved for RGPIO / currently_not_implemented	SC2	
B64_T3	in	B1	1.8V	reserved for RGPIO / currently_not_implemented	SC2	
B65_T1	in	C2	1.8V	CAN_S (with pulldown)	SC2	
B65_T2	out	E4	1.8V	CAN_FAULT	SC2	
B65_T3		C1	1.8V	/ currently_not_used	SC2	
B66_T1	in	D1	1.8V	FPGA / dp_aux_data_out	SC2	
B66_T2	in	F4	1.8V	FPGA / dp_aux_data_oe_n	SC2	
B66_T3	out	F3	1.8V	FPGA / dp_aux_data_	SC2	
B67_T1	out	F1	1.8V	FPGA / dp_hot_plug_detect	SC2	
B67_T2	in	G3	1.8V	FPGA / LED	SC2	
B67_T3	in	H4	1.8V	FPGA / LED	SC2	
C_TCK	in	A8	3.3V	JTAG CPLD XMOD	SC1	
C_TDI	in	C7	3.3V	JTAG CPLD XMOD	SC1	
C_TDO	out	A6	3.3V	JTAG CPLD XMOD	SC1	
C_TMS	int	C9	3.3V	JTAG CPLD XMOD	SC1	
CAN_FAULT	in	D15	3.3V	CAN / B65_T2	SC1	
CAN_RX	in	B15	3.3V	CAN / MIO34	SC1	
CAN_S	out	C15	3.3V	CAN / B65_T1	SC1	
CAN_TX	out	C16	3.3V	CAN / MIO35	SC1	
CLK_SC	in	AA9	3.3V	external User CLK 25MHz (oscillator is assembly option)	SC1	
DDR_EN	out	C6	3.3V	Power 7A	SC1	
DDR_PG	in	B8	3.3V	Power 7A	SC1	
DONE	in	G4	1.8V	PS Config	SC2	

DP_AUX_DE	out	AB13	3.3V	DP	SC1	
DP_AUX_RX	in	AB12	3.3V	DP	SC1	
DP_AUX_TX	out	AA14	3.3V	DP	SC1	
DP_EN	out	M4	1.8V	Power 8	SC2	
DP_TX_HPD	in	AA15	3.3V	DP	SC1	
EN_12V	out	C10	3.3V	Power 1	SC1	
EN_3.3V / EN_3P3V	out	Y8	3.3V	Power 2	SC1	
EN_A_3V3	out	Y18	3.3V	Power 8 FMC	SC1	
EN_AF_1V8	out	W19	3.3V	Power 8 FMC	SC1	
EN_B_3V3	out	G11	3.3V	Power 8 FMC	SC1	
EN_BC_1V8	out	A3	3.3V	Power 8 FMC	SC1	
EN_C_3V3	out	E11	3.3V	Power 8 FMC	SC1	
EN_D_3V3	out	F8	3.3V	Power 8 FMC	SC1	
EN_DE_1V8	out	C5	3.3V	Power 8 FMC	SC1	
EN_E_3V3	out	E8	3.3V	Power 8 FMC	SC1	
EN_F_3V3	out	Y10	3.3V	Power 8 FMC	SC1	
EN_GT_L	out	A7	3.3V	Power 4B,C	SC1	
EN_GT_R	out	B7	3.3V	Power 4B,C	SC1	
EN_SFP_SSD	out	W8	3.3V	Power 8	SC1	
EN_VCCINT	out	B9	3.3V	Power 1	SC1	
ERR_OUT	in	H1	1.8V	PS Config	SC2	
ERR_STATUS	in	J2	1.8V	PS Config	SC2	
ETH_RST	out	L6	1.8V	Reset	SC2	
F_LA06_SC_N		M19	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA06_SC_P		M18	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA07_SC_N		P21	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA07_SC_P		N20	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA08_SC_N		N18	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA08_SC_P		M20	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA09_SC_N		R18	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA09_SC_P		R19	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA10_SC_N		R20	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA10_SC_P		R21	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA11_SC_N		U19	FMC_AF_1.8V	/ currently_not_used	SC2	

F_LA11_SC_P		T19	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA12_SC_N		P18	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA12_SC_P		P19	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA13_SC_N		U17	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA13_SC_P		U18	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA14_SC_N		R17	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA14_SC_P		T18	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA15_SC_N		R16	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA15_SC_P		T17	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA16_SC_N		V19	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA16_SC_P		W20	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA17_SC_N		N16	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA17_SC_P		N17	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA18_SC_N		L16	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA18_SC_P		L17	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA19_SC_N		M16	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA19_SC_P		M17	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA20_SC_N		N6	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA20_SC_P		N7	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA21_SC_N		T6	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA21_SC_P		R7	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA22_SC_N		T5	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA22_SC_P		R6	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA23_SC_N		P6	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA23_SC_P		P7	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA24_SC_N		W3	FMC_AF_1.8V	/ currently_not_used	SC2	

F_LA24_SC_P		V4	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA25_SC_N		Y2	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA25_SC_P		W4	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA26_SC_N		U4	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA26_SC_P		T4	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA27_SC_N		U5	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA27_SC_P		T7	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA28_SC_N		V2	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA28_SC_P		W1	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA29_SC_N		AA1	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA29_SC_P		Y1	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA30_SC_N		V1	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA30_SC_P		U3	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA31_SC_N		V3	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA31_SC_P		W2	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA32_SC_N		M3	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA32_SC_P		N5	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA33_SC_N		R2	FMC_AF_1.8V	/ currently_not_used	SC2	
F_LA33_SC_P		R3	FMC_AF_1.8V	/ currently_not_used	SC2	
F1_EN	out	C8	3.3V	FAN	SC1	
F1PWM	out	E10	3.3V	FAN	SC1	
F1SENSE	in	D11	3.3V	FAN	SC1	
F2_EN	out	B4	3.3V	FAN	SC1	
F2PWM	out	D9	3.3V	FAN	SC1	
F2SENSE	in	G12	3.3V	FAN	SC1	
F3_EN	out	A12	3.3V	FAN	SC1	
F3PWM	out	B13	3.3V	FAN	SC1	
F3SENSE	in	A13	3.3V	FAN	SC1	
FAN_A_EN	out	Y19	3.3V	FAN	SC1	
FAN_B_EN	out	A2	3.3V	FAN	SC1	

FAN_C_EN	out	B3	3.3V	FAN	SC1	
FAN_D_EN	out	D7	3.3V	FAN	SC1	
FAN_E_EN	out	D6	3.3V	FAN	SC1	
FAN_F_EN	out	W18	3.3V	FAN	SC1	
FMC12V_EN	out	AA8	3.3V	Power 8 FMC	SC1	
FMCA_PG_C2M	inout	E16	3.3V	Power 8 FMC	SC1	
FMCA_PG_M2C	in	F17	3.3V	Power 8 FMC	SC1	
FMCA_PRSNT	in	F16	3.3V	Power 8 FMC	SC1	
FMCA_TCK	out	T16	3.3V	JTAG	SC1	
FMCA_TDI	out	U15	3.3V	JTAG	SC1	
FMCA_TDO	in	U16	3.3V	JTAG	SC1	
FMCA_TMS	out	V17	3.3V	JTAG	SC1	
FMCAF_12V_PG	in	W9	3.3V	Power 8 FMC	SC1	
FMCB_PG_C2M	inout	C4	3.3V	Power 8 FMC	SC1	
FMCB_PG_M2C	in	D5	3.3V	Power 8 FMC	SC1	
FMCB_PRSNT	in	D4	3.3V	Power 8 FMC	SC1	
FMCB_TCK	out	E6	3.3V	JTAG	SC1	
FMCB_TDI	out	D8	3.3V	JTAG	SC1	
FMCB_TDO	in	E9	3.3V	JTAG	SC1	
FMCB_TMS	out	F10	3.3V	JTAG	SC1	
FMCC_PG_C2M	inout	U6	3.3V	Power 8 FMC	SC1	
FMCC_PG_M2C	in	V6	3.3V	Power 8 FMC	SC1	
FMCC_PRSNT	in	W5	3.3V	Power 8 FMC	SC1	
FMCC_TCK	out	W6	3.3V	JTAG	SC1	
FMCC_TDI	out	Y4	3.3V	JTAG	SC1	
FMCC_TDO	in	Y5	3.3V	JTAG	SC1	
FMCC_TMS	out	AA3	3.3V	JTAG	SC1	
FMCD_PG_C2M	inout	G8	3.3V	Power 8 FMC	SC1	
FMCD_PG_M2C	in	G10	3.3V	Power 8 FMC	SC1	
FMCD_PRSNT	in	AA4	3.3V	Power 8 FMC	SC1	
FMCD_TCK	out	T12	3.3V	JTAG	SC1	
FMCD_TDI	out	U8	3.3V	JTAG	SC1	
FMCD_TDO	in	V9	3.3V	JTAG	SC1	
FMCD_TMS	out	U10	3.3V	JTAG	SC1	
FMCE_PG_C2M	inout	AB3	3.3V	Power 8 FMC	SC1	
FMCE_PG_M2C	in	AB2	3.3V	Power 8 FMC	SC1	
FMCE_PRSNT	in	AB5	3.3V	Power 8 FMC	SC1	
FMCE_TCK	out	Y6	3.3V	JTAG	SC1	
FMCE_TDI	out	AB6	3.3V	JTAG	SC1	
FMCE_TDO	in	AA7	3.3V	JTAG	SC1	

FMCE_TMS	out	AB7	3.3V	JTAG	SC1	
FMCF_PG_C2M	inout	AB20	3.3V	Power 8 FMC	SC1	
FMCF_PG_M2C	in	AB21	3.3V	Power 8 FMC	SC1	
FMCF_PRSNT	in	AA19	3.3V	Power 8 FMC	SC1	
FMCF_TCK	out	W11	3.3V	JTAG	SC1	
FMCF_TDI	out	V11	3.3V	JTAG	SC1	
FMCF_TDO	in	AB10	3.3V	JTAG	SC1	
FMCF_TMS	out	AA10	3.3V	JTAG	SC1	
I2C_RST	out	L2	1.8V	Reset	SC2	
INIT_B	in	J3	1.8V	PS Config	SC2	
JTAGENB	in	A16	3.3V	JTAG / Enable to get access to CPLD over JTAG. Pin is not accessible on CPLD. Is set by DIP-Switch S3-2	SC1	
LED_1A	out	Y12	3.3V	ETH LED yellow (right connector LED)	SC1	
LED_2A	out	Y13	3.3V	ETH LED green (left connector LED) (LED_2A high LED_2B low)	SC1	
LED_2B	out	Y14	3.3V	ETH LED orange (left connector LED) (LED_2B high LED_2A low)	SC1	
LED1	out	U12	3.3V	USR (D13 green)	SC1	
LED2	out	V12	3.3V	USR (D14 green)	SC1	
LED3	out	W12	3.3V	USR (D15 green)	SC1	
LED4	out	V13	3.3V	USR (D16 red)	SC1	
MEM_SCL	in	W16	3.3V	I2C	SC1	
MEM_SDA	inout	V16	3.3V	I2C	SC1	
MIO24		F5	1.8V	MIO / currently_not_used	SC2	
MIO25		G5	1.8V	MIO / currently_not_used	SC2	
MIO26	out	G15	3.3V	MIO / PJTAG TCK	SC1	
MIO27	out	E12	3.3V	MIO / PJTAG TDI	SC1	
MIO28	in	E15	3.3V	MIO / PJTAG TDO	SC1	
MIO29	out	C11	3.3V	MIO / PJTAG TMS	SC1	
MIO30	out	C13	3.3V	MIO / Status LED	SC1	
MIO31	in	B12	3.3V	MIO / currently_not_used	SC1	
MIO32		B11	3.3V	MIO / currently_not_used	SC1	
MIO33	in	U7	3.3V	MIO / PCIe Reset	SC1	
MIO34	out	D12	3.3V	MIO / CAN	SC1	
MIO35	in	F15	3.3V	MIO / CAN	SC1	
MIO36		G7	3.3V	MIO / currently_not_used	SC1	
MIO37		D14	3.3V	MIO / currently_not_used	SC1	
MIO40		F12	3.3V	MIO / currently_not_used	SC1	
MIO41		T8	3.3V	MIO / currently_not_used	SC1	
MIO42	out	B14	3.3V	MIO / UART RX	SC1	
MIO43	in	E7	3.3V	MIO / UART TX	SC1	
MIO44	out	E14	3.3V	MIO / SD-WP	SC1	
MIO45	out	A20	3.3V	MIO / SD-CP	SC1	

MIO6	in	F6	1.8V	MIO / QSPI FB CLK from ZynqMP	SC2	
MODE0	out	H3	1.8V	PS Config Boot Mode	SC2	
MODE1	out	H2	1.8V	PS Config Boot Mode	SC2	
MODE2	out	G2	1.8V	PS Config Boot Mode	SC2	
MODE3	out	G1	1.8V	PS Config Boot Mode	SC2	
MR	out	L7	1.8V	PS Config (PS_POR_B) Reset	SC2	
NC	out	AA20	3.3V	used as dummi output pin / Not connected	SC1	
NC		T15	3.3V	Not connected	SC1	
NC		V15	3.3V	Not connected	SC1	
NC		W15	3.3V	Not connected	SC1	
NC		V14	3.3V	Not connected	SC1	
NC		W14	3.3V	Not connected	SC1	
NC		U13	3.3V	Not connected	SC1	
NC		T13	3.3V	Not connected	SC1	
NC		AB16	3.3V	Not connected	SC1	
NC		Y3	3.3V	Not connected	SC1	
NC		A21	3.3V	Not connected	SC1	
NC		G6	1.8V	Not connected	SC2	
NC		N1	1.8V	Not connected	SC2	
NC		N2	1.8V	Not connected	SC2	
NC		M1	1.8V	Not connected	SC2	
NC		N3	1.8V	Not connected	SC2	
NC		P2	1.8V	Not connected	SC2	
NC		M7	1.8V	Not connected	SC2	
NC		M6	1.8V	Not connected	SC2	
NC		P3	1.8V	Not connected	SC2	
NC		R1	1.8V	Not connected	SC2	
NC		M5	1.8V	Not connected	SC2	
NC		H5	1.8V	Not connected	SC2	
NC		J5	1.8V	Not connected	SC2	
NC		J4	1.8V	Not connected	SC2	
NC		K5	1.8V	Not connected	SC2	
NC		L3	1.8V	Not connected	SC2	
PG_12V	in	A11	3.3V	Power 1	SC1	
PG_FPD	in	A10	3.3V	Power 2	SC1	
PG_GT_L	in	K3	1.8V	Power 5BC	SC2	
PG_GT_R	in	F11	3.3V	Power 5BC	SC1	
PG_PSGT	in	A5	3.3V	Power 6A	SC1	
PHY_CLK125M	in	K2	1.8V	CLK	SC2	
PHY_LED0	in	L5	1.8V	PHY LED	SC2	

PHY_LED1	in	L1	1.8V	PHY LED	SC2	
PHY_LED2	in	K1	1.8V	/ currently_not_used	SC2	
PLL_RST	out	L4	1.8V	Reset	SC2	
PROG_B	out	E2	1.8V	PS Config (opt. PL Reset)	SC2	
PSGT_EN	out	B10	3.3V	Power 4A	SC1	
SC_SW1	in	E17	3.3V	USR S3-3 / Set Boot Mode	SC1	
SC_SW2	in	D16	3.3V	USR S3-4 / Set Boot Mode	SC1	
SD_CD	in	T11	3.3V	SD CD	SC1	
SD_EN	out	U11	3.3V	Power 8	SC1	
SD_WP	in	T10	3.3V	SD WP	SC1	
SFP_LED1		AB17	3.3V	/ currently_not_used	SC1	
SFP_LED2		AB18	3.3V	/ currently_not_used	SC1	
SFP_LED3		AA16	3.3V	/ currently_not_used	SC1	
SFP_LED4		AB15	3.3V	/ currently_not_used	SC1	
SFP0_LOS		V8	3.3V	/ currently_not_used	SC1	
SFP0_TX_DIS	out	Y7	3.3V	SFP	SC1	
SFP1_LOS		W7	3.3V	/ currently_not_used	SC1	
SFP1_TX_DIS		V7	3.3V	SFP	SC1	
SI5345_CLK		E1	1.8V	/ currently_not_used	SC2	
SSD1_LED		AA13	3.3V	/ currently_not_used	SC1	
SSD1_PERSTN	out	AA11	3.3V	SSD Reset	SC1	
SSD1_SLEEP		AA12	3.3V	/ currently_not_used	SC1	
SSD1_WAKE	out	AB11	3.3V	SSD	SC1	
U_SW1	in	D18	3.3V	USR (S4-1) / currently_not_used	SC1	
U_SW2	in	D17	3.3V	USR (S4-2) / currently_not_used	SC1	
U_SW3	in	C19	3.3V	USR (S4-3)/ currently_not_used	SC1	
U_SW4	in	C18	3.3V	USR (S4-4) / currently_not_used	SC1	
USB0_RST	out	M2	1.8V	Reset	SC2	
USBH_MODE0	out	Y17	3.3V	USB	SC1	
USBH_MODE1	out	Y16	3.3V	USB	SC1	
USBH_RST	out	Y15	3.3V	Reset	SC1	
USR_BUT1	in	F13	3.3V	USR (S1)	SC1	
USR_BUT2	in	G13	3.3V	USR (S2) / Power Reset	SC1	
USR_BUT3	in	W17	3.3V	USR (S3) / optional Power Reset	SC1	N.C. on PCB REV02,REV03
XMOD1_A		B19	3.3V	XMOD J35 / currently_not_used	SC1	
XMOD1_B	out	A17	3.3V	XMOD J35 LED / Attention this is connected to XMOD1_E	SC1	
XMOD1_E		C17	3.3V	XMOD J35 / Attention this is connected to XMOD1_B / currently_not_used	SC1	
XMOD1_G	in	A18	3.3V	XMOD J35 Button	SC1	
XMOD2_A	out	K7	1.8V	UART RXD (XMOD J24)	SC2	
XMOD2_B	in	K6	1.8V	UART TX (XMOD J24)	SC2	

XMOD2_E	out	H7	1.8V	XMOD J24 LED / Boot Mode	SC2	
XMOD2_G	in	H6	1.8V	XMOD J24 Button / PS Reset	SC2	

Functional Description

JTAG

JTAG access over CPLD XMOD J35.

Set DIP-Switch S3-2 to ON to get CPLD into JTAG Chain. This is only needed for CPLD update. Otherwise JTAG is routed thought FMCs or to PJTAG dependign on boot mode. JTAG is connected into cascade from FMC A to F, if module is detected, otherwise corresponding connector is left out.

Boot Mode	Description
PJTAG0	PJTAG MIOs are connected to JTAG chain
all other	FMC IOs are connected to JTAG chain

Note: FPGA/SoC JTAG access is available directly over second XMOD.

Power

Power is controlled by different state machines and can be restart over S2 Button or S3 Button (PCB REV04 only). Main Power sequence must be finished successfully before other power management units starts. Power Management can be checked over status LEDs, see LED section.

Main Power:

State	Conditions for next state	Description
1:IDLE	PG_12V is ready	Start with this state on power up or Power Reset • EN12V is enabled, EN_VCCINT, EN_3P3V, DDR_EN are disabled
2:PER1_EN	PG_FPD is ready	• EN12V, EN_VCCINT, EN_3P3V are enabled, DDR_EN is is disabled
3:PER2_EN	DDR_PG is ready	• EN12V, EN_VCCINT, EN_3P3V DDR_EN are enabled
4:RDY	DDR_PG or PG_FPD or PG_12V failed	Normal state if power sequence was ok.
5:ERROR	---	Only set, if a error occurs after successfully power up. Manually reset is needed.

MGT Power:

State	Conditions for next state	Description
1:IDLE	Main Power sequence is done	Start with this state if main power is stared. • PSGT_EN, EN_GT_L, EN_GT_R are disabled
2:PER1_EN	PG_PSGT, PG_GT_L, PG_GT_R are ready	• SGT_EN, EN_GT_L, EN_GT_R are enabled

3:RDY	PG_PSGT or PG_GT_L or PG_GT_R failed	Normal state if power sequence was ok.
4:ERROR	---	Only set if a error occurs after successfully power up. Manually reset is needed.

Periphery Power:

State	Conditions for next state	Description
1:IDLE	Main Power sequence is done	Start with this state if main power is stared. • DP_EN, EN_SFP_SSD, SD_EN are disabled
2:PER1_EN	No check possible, next state is RDY	• DP_EN, EN_SFP_SSD, SD_EN are enabled
3:RDY	No check possible	Normal state if power sequence was ok.
4:ERROR	---	This state should never occurs.

FMC A and F Power:

State	Conditions for next state	Description
1:IDLE	Main Power sequence is done	Start with this state if main power is stared. • FMC12V_EN, EN_AF_1V8, EN_A_3V3, EN_F_3V3, FMCF_PG_C2M, FMCA_PG_C2M are disabled
2: PER1_EN	FMCAF_12V_PG, FMCF_PG_C2M, FMCA_PG_C2M are ready	• FMC12V_EN, EN_AF_1V8, EN_A_3V3, EN_F_3V3, FMCF_PG_C2M, FMCA_PG_C2M are enabled
3:RDY	FMCAF_12V_PG or FMCF_PG_C2M or FMCA_PG_C2M failed	Normal state if power sequence was ok.
4: ERROR	---	Only set if a error occurs after successfully power up. Manually reset is needed.

* FMCF_PG_C2M, FMCA_PG_C2M are bidirectional. External Pull up is used to check power fails.

FMC B,C,D,E Power:

State	Conditions for next state	Description
1:IDLE	Main Power sequence is done	Start with this state if main power is stared. • EN_BC_1V8, EN_DE_1V8, EN_B_3V3, EN_C_3V3, EN_D_3V3, EN_E_3V3, FMCB_PG_C2M, FMCC_PG_C2M, FMCD_PG_C2M, FMCE_PG_C2M are disabled
2: PER1_EN	FMCB_PG_C2M, FMCC_PG_C2M, FMCD_PG_C2M, FMCE_PG_C2M are ready	• EN_BC_1V8, EN_DE_1V8, EN_B_3V3, EN_C_3V3, EN_D_3V3, EN_E_3V3, FMCB_PG_C2M, FMCC_PG_C2M, FMCD_PG_C2M, FMCE_PG_C2M are enabled
3:RDY	FMCB_PG_C2M or FMCC_PG_C2M or FMCD_PG_C2M or FMCE_PG_C2M failed	Normal state if power sequence was ok.

4: ERROR	---	Only set if a error occurs after successfully power up. Manually reset is needed.

FMCF_PB_C2M, FMCC_PG_C2M, FMCD_PG_C2M, FMCE_PG_C2M are bidirectional. External Pull up is used to check power fails. 12V is sourced and controlled by main power.

Reset

Button	Description
S2	Main Power Reset Button. Restart power management.
FPGA XMOD	PS MR Reset Button. Restart PS (PS_POR_B)

- Buttons are debounced.

For all other resets, see component sections.

Boot Mode

S3-3 (SC_SW1)	S3-4 (SC_SW2)	Description
OFF	OFF	SD1 Boot Mode (SD-Card on J11), if SD is insered
OFF	OFF	eMMC Boot Mode, if SD is **not** insered
OFF	ON	PJTAG0
ON	OFF	QSPI32
ON	ON	JTAG

Display Port

Output	Input
DP_AUX_TX	B66_T1
DP_AUX_DE	not B66_T2
B66_T3	DP_AUX_RX
B67_T1	DP_TX_HPD

CAN

- CAN_S soured by B65_T1
- CAN_FAULT is connected to B65_T2
- CAN_RX is connected to MIO34
- CAN_TX sourced by MIO35

SD

- SD_EN is controlled by power management.

- SD_CD is connected to MIO45.
- SD_WP is connected to MIO44.

SFP

- Transmit for all SFP is enabled.

USB

- USB Mode pins constant "11" (default boot mode).
- USB0_RST is controlled by power management.
- USBH_RST is controlled by power management.

SSD

- SSD1_WAKE is "0".
- SSD1_PERSTn is controlled by power management and MIO33.

I2C

- I2C_RST is controlled by power management.

FAN

FAN1 to FAN3 speed can be controlled via I2C Bus. FMC FANs can be disabled over I2C Bus and only run, if FMCx_PRESNT is available.

I2C Baseaddress: 0x74. I2C with 8Bit Register Address with 8Bit Data. I2C CLK currently 100 MHz supported.

Write Access:

Register Address	Name	Description
0	FAN CTRL	Enable FAN, Bit 0-2 Fan1 to Fan2, Bit 3 FMC B, Bit 4 FMC C , Bit 5 FMC D , Bit 6 FMC E, Bit 7 FMC A and F. Default all enabled (1)
1	FAN1 PWM	FAN1 PWM (0%-100%, Default 30%)
2	FAN2 PWM	FAN2 PWM (0%-100%, Default 30%)
3	FAN3 PWM	FAN3 PWM (0%-100%, Default 30%)

Read Access:

Register Address	Name	Description
0	FAN CTRL	FAN Control register
1	FAN1 RPS	FAN1 Revolutions per second
2	FAN2 RPS	FAN2 Revolutions per second
3	FAN3 RPS	FAN3 Revolutions per second

FMC

FMC present (FMCx_PRESNT) signals are used for board detect and enables.

FMC JTAG: See JTAG section

FAN : See FAN section

UART

UART is connected to FPGA XMOOD on J24. XMOD UART RXD output is connected to MIO42. MIO43 is connected to XMOD UART TX input.

USR Buttons and Switches

LED

LED	Description
LED4 (D16 red)	User FPGA IO B67_T3
LED3 (D15 green)	User FPGA IO B67_T2
LED2 (D14 green)	PS Status. Status depends on blink sequence and priority. 1. ******** : Reset button is pressed 2. *****ooo : Init_B failed 3. ****oooo : PS_Error_Status and PS_Error failed 4. ***ooooo : PS_Error_Status failed 5. **oooooo : PS_Error failed 6. *ooooooo : Done is low-> SoC PL not programmed 7. LED OFF or ON : user defined from MIO30
LED4 (D13 green)	Power LED. Status depends on blink sequence and priority. 1. LED OFF: Power button is pressed (Note, 1 and 8 are swapped with CPLD REV03) 2. ******** : Main power up failed 3. *****ooo : Main power error after successfully startup 4. *****ooo : MGT or Periphery power up failed 5. ***ooooo : MGT or Periphery power error after successfully startup 6. **oooooo : FMC power up failed 7. *ooooooo : FMC power error after successfully startup 8. LED ON: Power good (Note, 1 and 8 are swapped with CPLD REV03)
FPGA XMOD (J24-XMOD2)	Boot Mode. Status depends on blink sequence and priority. 1. LED ON : JTAG 2. ******** : Error unknown state 3. *****ooo : not used 4. *****ooo : not used 5. ***ooooo : not used 6. **oooooo : QSPI 7. *ooooooo : PJTAG_0 8. LED OFF : SD1

CPLD XMOD (J35-XMOD1)	1. ******** : one or more of FMCx_PG_M2C of connected FMC are not ready 2. LED OFF : all connected FMCx_PG_M2C are ready
ETH LED Left (Green/Orange)	OFF, if Main Power Failed otherwise PHY_LED0(depends on PHY Configuration) ▪ Green, if FAN1...3 enabled and FMC FAN with connected modules are enabled ▪ Orange, if one of FAN1..3 or FMC FAN wirg connected modules are disabled
ETH LED Right (Yellow)	OFF, if Main Power Failed otherwise PHY_LED1(depends on PHY Configuration)

Appx. A: Change History and Legal Notices

Revision Changes

CPLD REV04 to REV05

- add can
- DP_TX_HPD input pin threshold changed

CPLD REV03 to REV04

- bugfix FMC JTAG (support multiple device in the chain now)

CPLD REV02 to REV03

- add main Reset to optional User Button 3 (only on PCB REV04 usable)
- add PHY LEDs
- add emmC Boot Mode
- new I2C controller
- swapped LED1 0,7 state (LED ON is ready now)

CPLD REV01 to REV02

- Correction of FAN_A_EN and FAN_AF_EN Location constrains
- Add Pullup attribute to FMCX_PRSNT signals
- I2C Enable mapping is changed

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV05	REV02, REV03, REV04	Error rendering macro 'page-info'	• firmware update • released at 2019-09-10

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]			Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.	

				String, class com. atlassian. confluence .core. ContentEn tityObject] [interface com. atlassian. user. User, class java. lang. String, class com. atlassian. confluence .core. ContentEn tityObject]	
2018-12-10	v.29	REV04	REV02, REV03, REV04	John Hartfiel	• firmware update • released at 2018-12-06
2018-11-19	v.28	REV03	REV02, REV03, REV04	John Hartfiel	• firmware update • released at 2018-11-19
2018-02-02	v.24	REV02	REV02, REV03	John Hartfiel	• add PCB REV03 support
2017-09-18	v.23	REV02	REV02	John Hartfiel	• Revision 02 finished
2017-08-16	v.21	REV01	REV02	John Hartfiel	• Revision 01 finished
2017-07-25	v.1	REV01	REV02		

					Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.	• Initial release

				confluence .user. Confluenc eUser, class java. lang. String, class com. atlassian. confluence .core. ContentEn tityObject] [interface com. atlassian. user. User, class java. lang. String, class com. atlassian. confluence .core. ContentEn tityObject]	
	All			**Error rendering macro 'page-info'** Ambiguou s method	

overloadin
g for
method
jdk.
proxy279.
$Proxy402
2#hasCont
entLevelP
ermission.
Cannot
resolve
which
method to
invoke for
[null,
class java.
lang.
String,
class com.
atlassian.
confluence
.pages.
Page] due
to
overlappin
g
prototypes
between:
[interface
com.
atlassian.
confluence
.user.
Confluenc
eUser,
class java.
lang.
String,
class com.

				atlassian. confluence .core. ContentEn tityObject] [interface com. atlassian. user. User, class java. lang. String, class com. atlassian. confluence .core. ContentEn tityObject]	

Legal Notices

Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

Copyright Notice

Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]