EDDP User Manual

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Introduction

The Electronic Drive Development Platform (EDDP) provides all necessary software and hardware components for development and evaluation of motor control applications. While these components (both software and hardware) can also be used separately, this manual describes EDDP usage with default reference hardware platform (EDDP Kit) only.

Hardware components/boards delivered in EDDP Kit are not intended to be used in final products. All software and hardware parts of the EDDP are intended for developers evaluating Motor Control Applications with Xilinx FPGA and/or SoC devices.

Use of Terms

The terms and acronyms used in the EDDP User Manual and EDPS User Manual are listed in the **Table 1**.

Term	Description
Adapter Board	Adapts the Reference Motor to the EDPS Board.
Control Board	An electronic board for controlling the EDPS Board, a Digilent board Arty Z7.
EDDP	Electronic Drive Development Platform.
EDDP Kit	A kit consisting of the EDPS Board, the Reference Motor, the Adapter board and.
EDPS Board	An Electric Drive Power Stage Board, a Trenz Electronic GmbH board TEC0053.

Host PC	A computer capable of running a web browser in order to run the Web UI.
Reference Motor	The motor included in the EDDP Kit. This motor is of brushless type and is already mated with an encoder.
Web UI	A user interface in the form of a web page permitting operating the EDDP.

Table 1: Terms and acronyms used.

Requirements for the Functional Test

The purpose of the Functional Test is to verify the functionality of the hardware by using the default firmware supplied.

Following items are required in addition to the EDDP Kit:

- Micro-USB Cable for the USB console of the Controller Board.
- Ethernet-based LAN with a DHCP server.
- RJ45 ethernet Cable.
- Computer with web browser to access the Web UI.
- Card reader supporting micro-SD Cards.
- Access to internet (to download SD Card images).

⚠ In order to pass EMC radiated emission (EN 55011) class B requirements option "Spread Spectrum" must be activated (standard setting).

⚠ Software version that was used in EMC test: (Visible in the GUI main screen) 2017-7-31 (SVN Tag 5745).

Requirements for the Development

Requirements for the development with SDSoC:

- All items listed under the Requirements for Functional Test.
- Basic knowledge of Xilinx All Programmable FPGA and/or SoC devices, basic knowledge of Xilinx SDK and C/C++ programming in order to be able to adapt the firmware to your requirements.
- A PC capable of running Xilinx SDSoC 2017.1 development environment.
- A valid Xilinx SDSoC license or voucher.

Requirements for the development with HLS:

- All items listed under Requirements for Functional Test.
- Basic knowledge of Xilinx All Programmable FPGA and/or SoC devices, basic knowledge of Xilinx SDK and C/C++ programming in order to be able to adapt the firmware to your requirements.
- A PC capable of running Xilinx Vivado 2017.1

Installation

⚠ Micro-SD is delivered without Linux images to avoid any issues related to US export control regulations.

Hardware Assembly

When delivered as full EDDP Kit several components are pre-assembled.

Motor Adapter Board

The Reference Motor with Encoder is connected to the EDPS Board using the Adapter Board (see Figure 1). In the EDDP Kit the Reference Motor is pre-assembled.

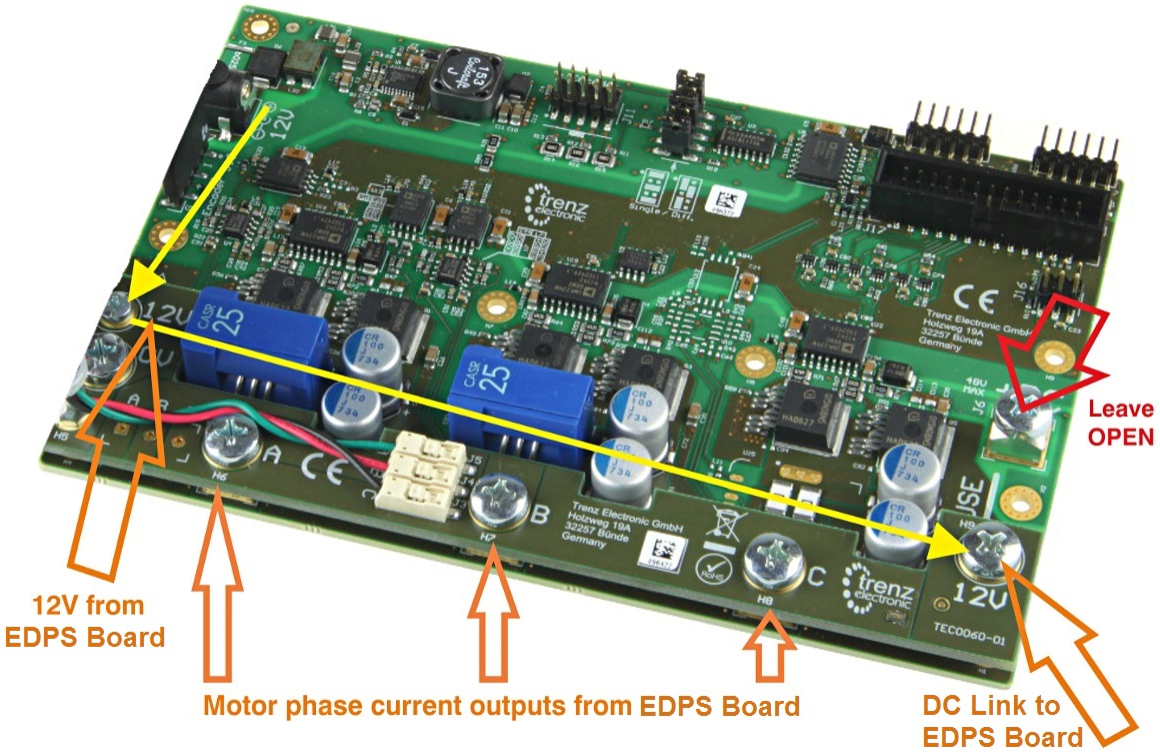

Figure 1: Top view of the EDPS Board with the Adapter Board mounted.

The Adapter Board is mounted to the EDPS Board using 5 x M6 screws (Labels 0V, A, B, C, 12V on Adapter Board) and with M3 screws and spacer - marked 12V at the left. This Adapter Board "forwards" (the yellow arrow) the EDPS Board pre-driver supply (12V) to the DC Link main terminal on the EDPS board, so that separate DC Link power supply is not needed allowing easy evaluation of the complete system.

Note terminal marked+DC must be left open when using the Adapter Board!

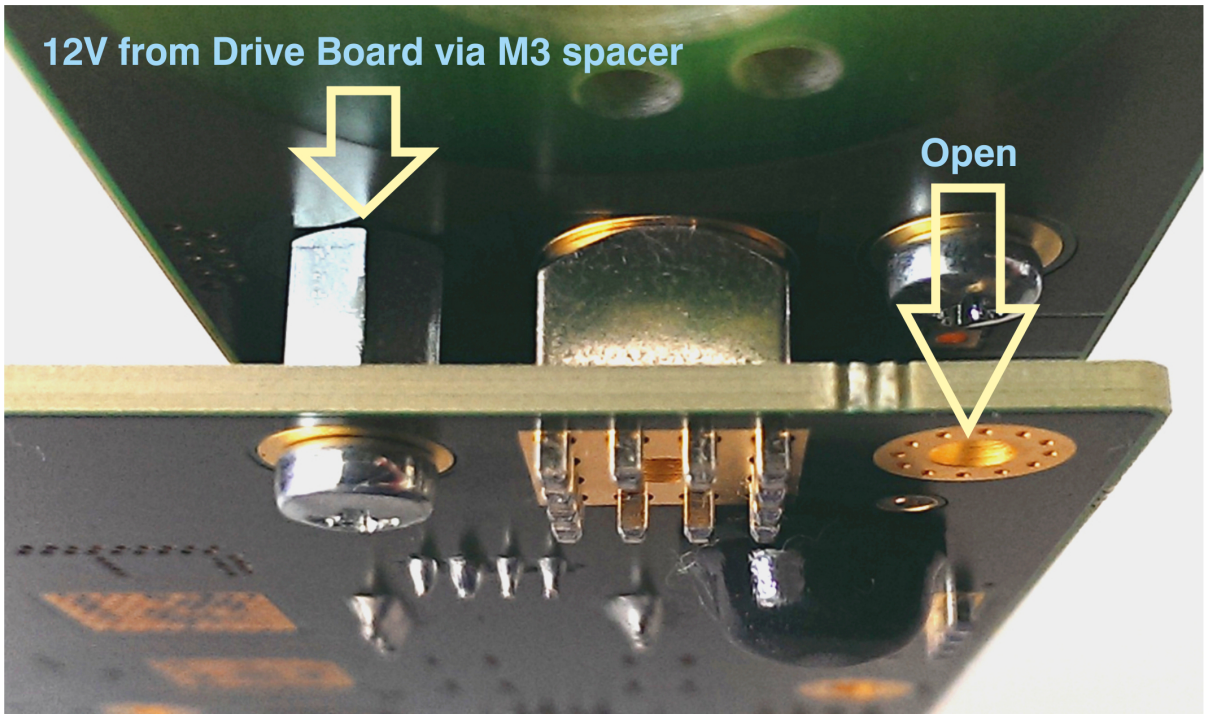

Figure 2: M3 spacer and two M3 screws connect 12V from the EDPS board to the Adapter Board.

Motor Connection

In the EDDP Kit the Reference Motor stator wires for all three phases are already connected to the Adapter Board. Instructions for manual assembly below:

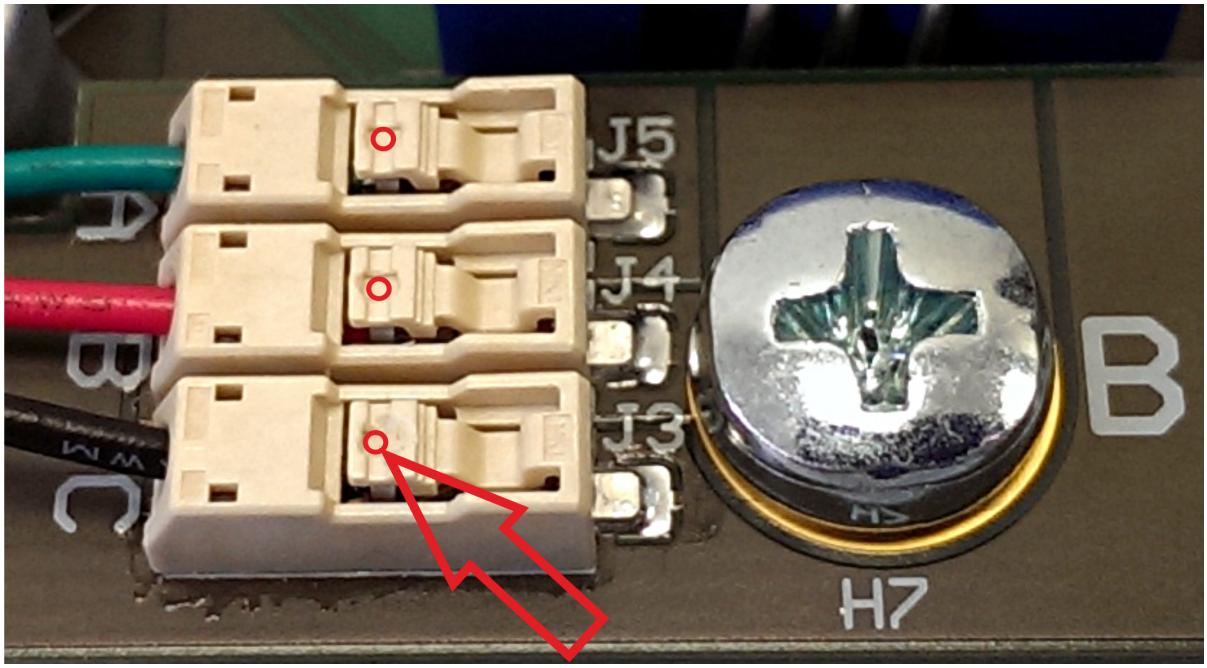

Figure 3: Red dots and arrow mark the place where wire terminal can be released for insertion or removal.

Use a ball-point pen or similar tool to apply gentle force at the dot to release the wires. Do not try to remove the wires by simply pulling them out without releasing them first! Do not apply force in any other region of the white plastic except as marked, because it is easy to damage the plastic.

Encoder Connection

One 6-pin Pmod cable is included with the EDDP Kit. It is already assembled between the encoder and the EDPS Board. Instructions for manual assembly are below:

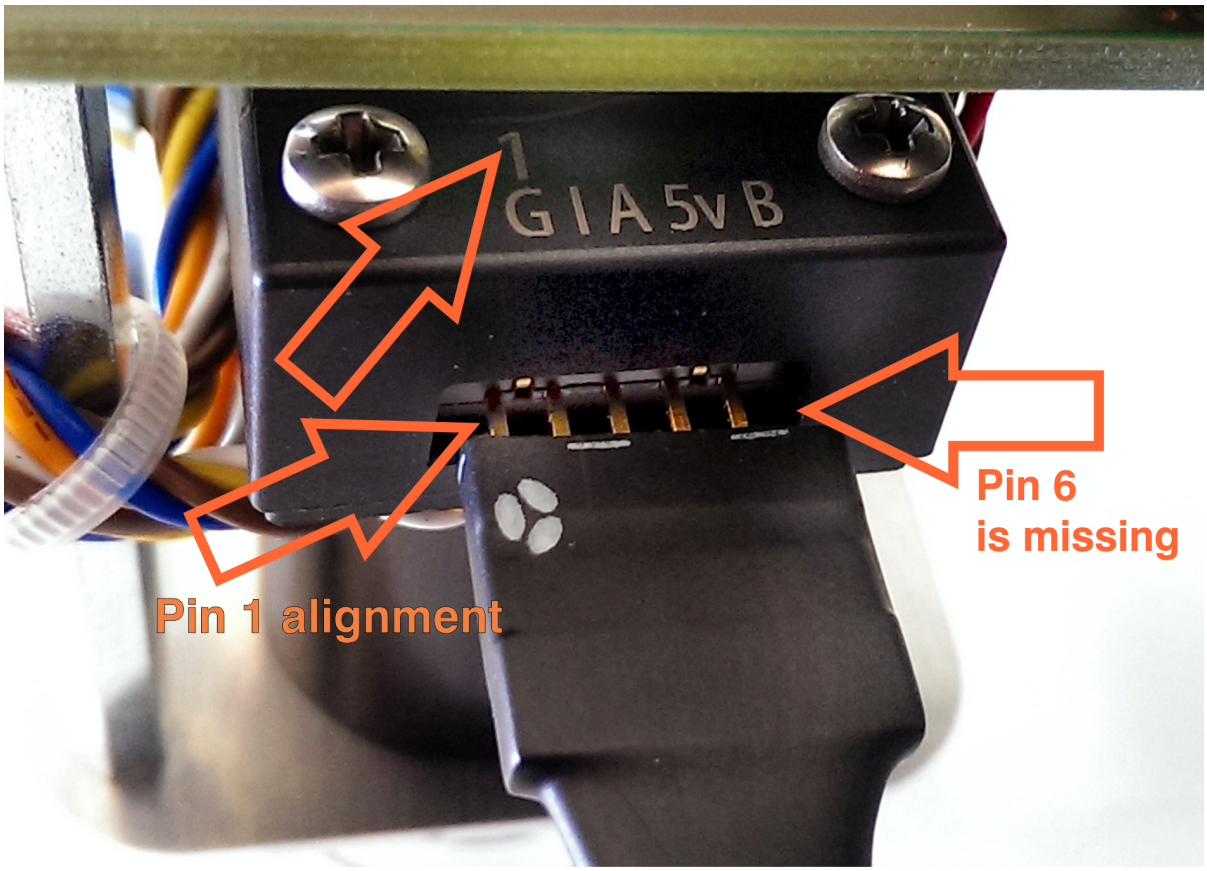

Figure 4: Pmod cable alignment to the Encoder connector.

Notice that there are 5 pins in the Encoder header while the PMoD female connector has 6 terminals. Red Arrow marks the "empty" terminal at the PMoD Cable.

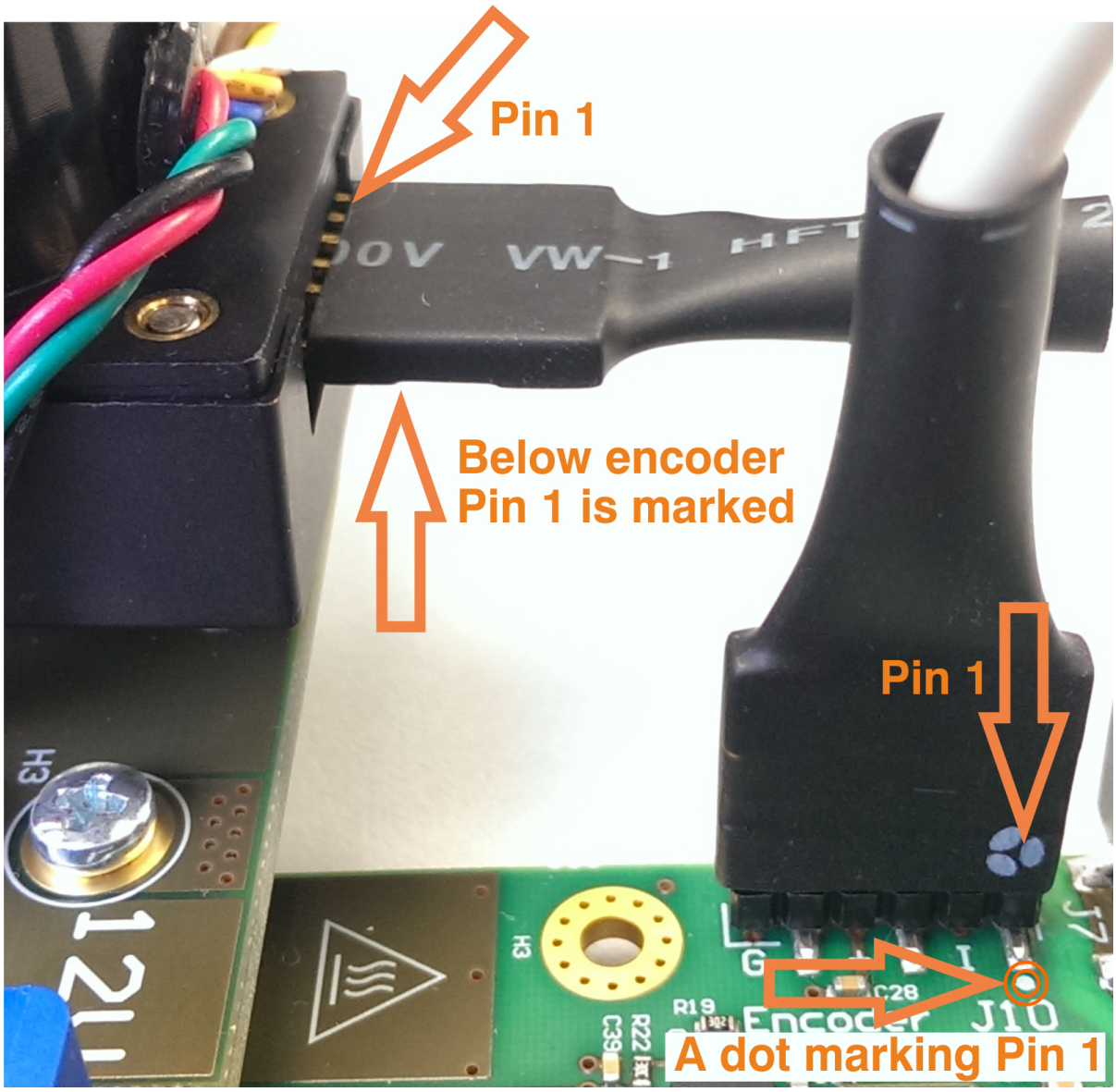

Figure 5: Pmod cable installation.

Pin 1 markings are indicated with the arrows, on the EDPS Board a white dot marks 6-pin Pmod header pin 1. This pin should be aligned to the Encoder Pin marked "G" and "1" visible when looking from the bottom up. Please note that Encoder header has 5 terminals while the driver board and Pmod cable have 6 terminals.

Network configuration on the Host PC (Optional)

An overview of network configuration and some methods for network troubleshooting are given.

It is assumed that the operating system on the Host PC is Microsoft Windows 7 or newer. For other operating systems, the basic network principles are the same, but the means of configuration are different; consult the corresponding user guides.

Open the Control Panel and click on the Network and Sharing Center. The following window appears:

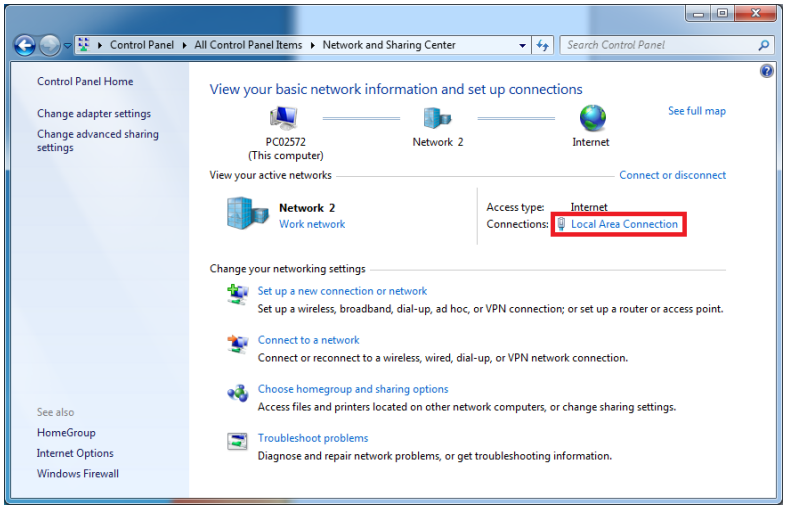

Figure 6: The Network and Sharing Centre, with the network connection used for communication with the Control Board highlighted.

Viewing network connection status

Locate the network connection that is to be used for communication with the Control Board and click on it. The network connection status dialog appears (Figure 7).

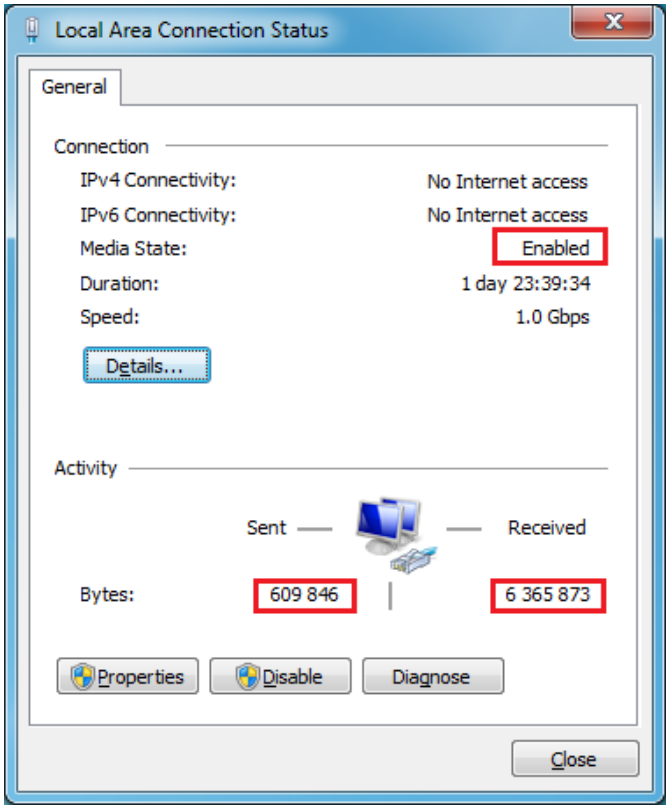

Figure 7: A network connection status dialog, with the media status and number of bytes sent and received highlighted.

For normal operation, the media state should read "Enabled".

During normal operation, the number of bytes sent and received should increase when there is network traffic, for example, when pinging the Control Board, when operating the Web UI, when pinging, etc.

Checking network connectivity to the Control Board

On the Start Menu, select "All Programs" "Accessories" "Command Prompt. A command prompt window appears. Enter the command

```
ping IP
```

where IP is the IP address of the Control Board. The result should be similar to the one on the following figure (Figure 8):

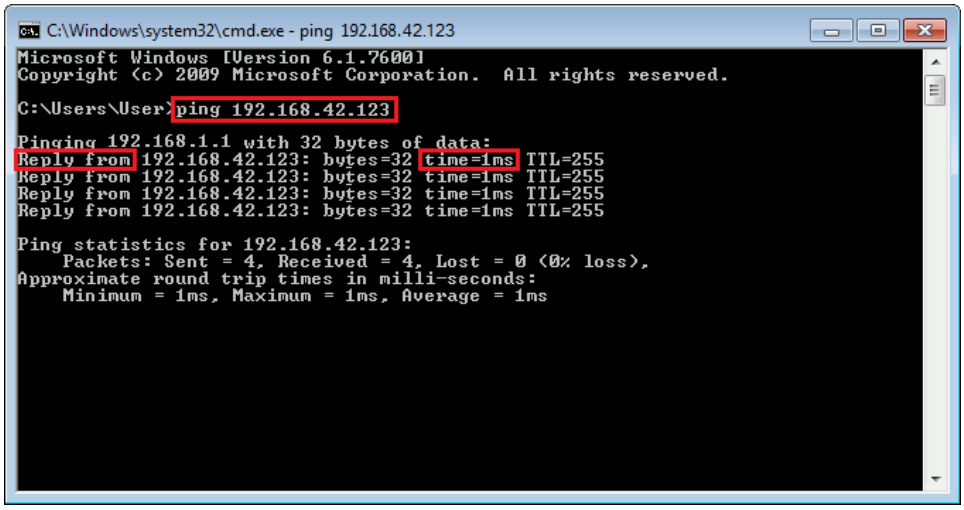

Figure 8: Successful check of network connectivity to the Control Board. The command entered by the user is highlighted, as are the important keywords that should be present in the output of the command "ping".

Note: After a recent change of network settings, it can happen that the ping is not successful because the changes haven't propagated to the other participiants on the network yet. It can be sometimes remedied by running the command "ping" on the other computer, in this case, on the Control Board, pinging the IP address of the Host PC.

Verifying network adapter settings

In the network connection status dialog (Figure 7), click "Details". A Network Connection Details dialog appears:

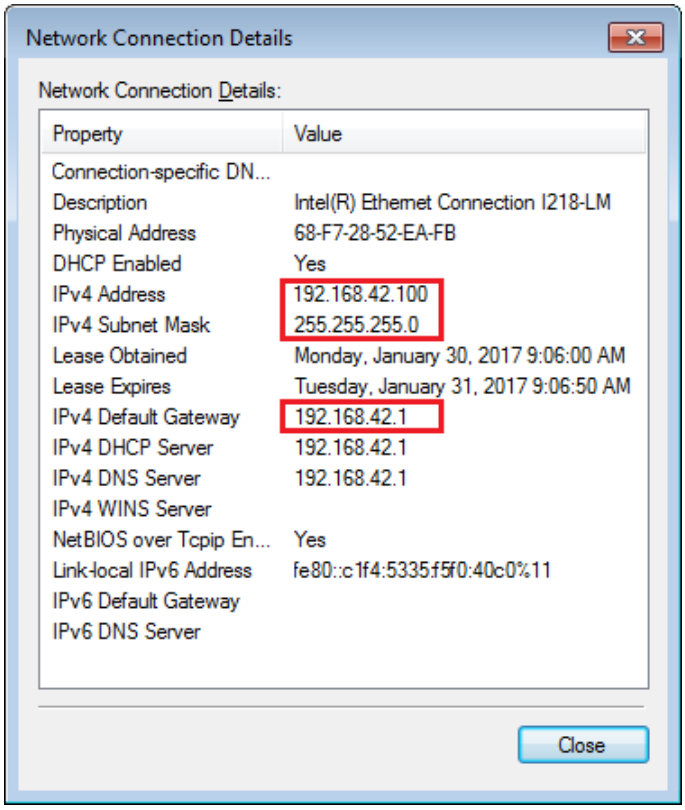

Figure 8: A Network Connection Details dialog, with the important IP settings highlighted.

The network settings should be such that the Control Board is reachable from the Host PC. In the case when they are in the same network segment (gateway is not involved), the following conditions should hold:

1. The subnet mask should be the same for the Control Board and the Host PC.
2. The IP addresses for the Control Board and Host PC must be different.
3. The subnet mask divides the IP address into two parts according to the the bits set in the binary notation (255 in decimal = 11111111 in binary):
    a. The network address, which corresponds to the the bits set in the subnet mask. This should be the same for the Control Board and the Host PC.
    b. The host address, which corresponds to the bits not set in the subnet mask. This should be different for the Control Board and the Host PC. Additional constraint: it cannot be neither null nor the maximum value.

On the example of settings shown on Figure 8 and the default configuration in the default firmware, the conditions are fulfilled as follows:

1. The subnet mask, 255.255.255.0, is the same for both.
2. The IP addresses, 192.168.42.100 for the Host PC and 192.168.42.123 for the Control Board, differ.
3. The subnet mask checks out as follows:
    a. The network address, 192.168.42.0, is the same for the Host PC and the Control Board.
    b. The host addresses, 0.0.0.100 for the Host PC and 0.0.0.123 for the Control Board, are different. In addition, neither is 0 nor the maximum value, 255 in this case.

Alternative method of viewing network settings: Open command prompt (see Figure 8) and execute the following command:

```
ipconfig
```

It will list all network connections and their associated IP addresses.

Changing the IP settings of a network connection

On the network connection status dialog (Figure 7), click "Properties". The following dialog (Figure 9) appears:

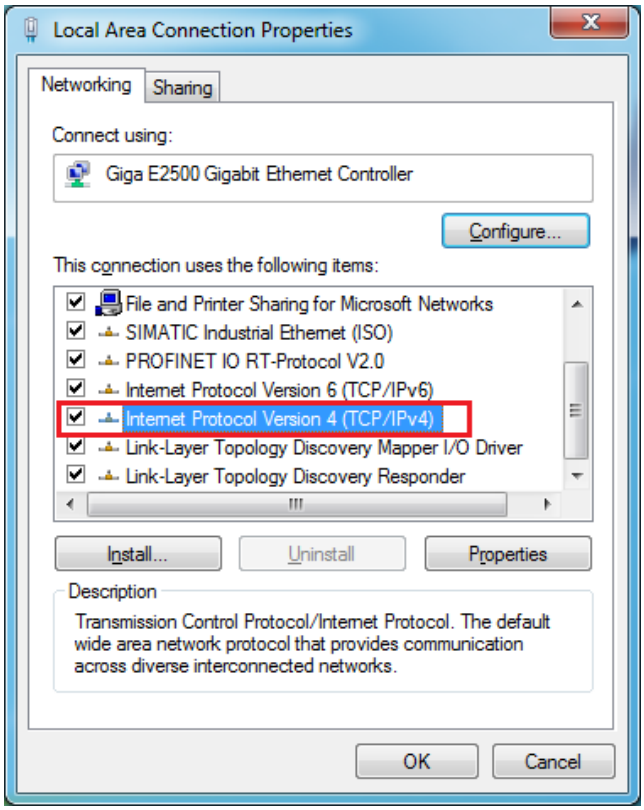

Figure 9: A network connection properties dialog. The item "Internet Protocol Version 4 (TCP/IPv4)" is selected and highlighted.

In the list of items used, select "Internet Protocol Version 4 (TCP/IPv4)" and click "Properties". The following dialog appears:

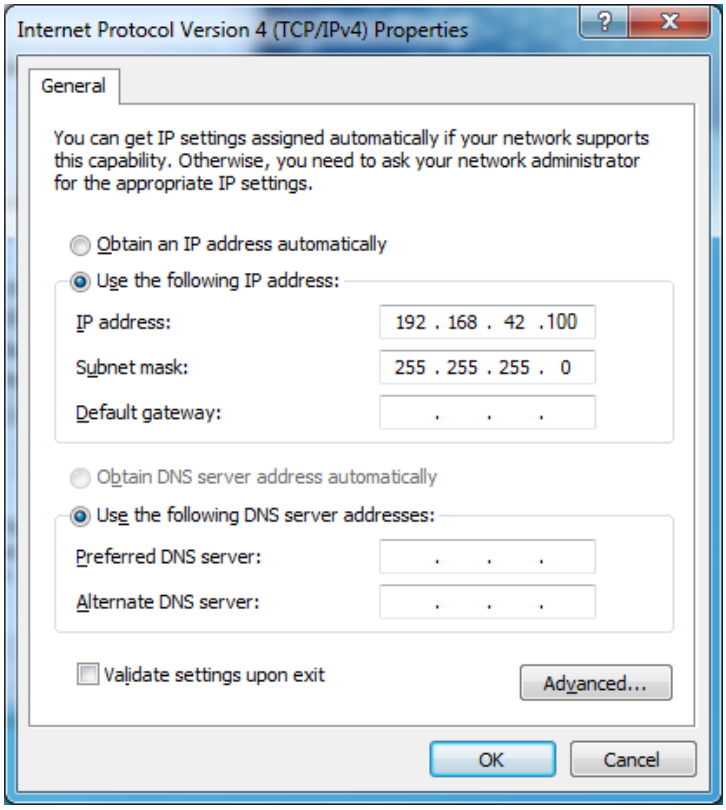

Figure 10: A TCP/IPv4 Properties dialog.

The settings on this dialog have to match the actual network settings.

In most network setups, settings are as follows:

- Checked: Obtain an IP address automatically.
- Checked: Obtain DNS server address automatically.

In the case when using an network adapter dedicated solely for nothing else but communication with the Control Board, a static IP configuration (as shown on Figure 10) is to be used as follows:

- Checked: Use the following IP address:
  - IP address: 192.168.42.100
  - Subnet mask: 255.255.255.0
  - Default gateway: not configured.

Other cases are not considered here; consultation with network administration and/or appropriate handbooks is recommended.

EDDP System Components

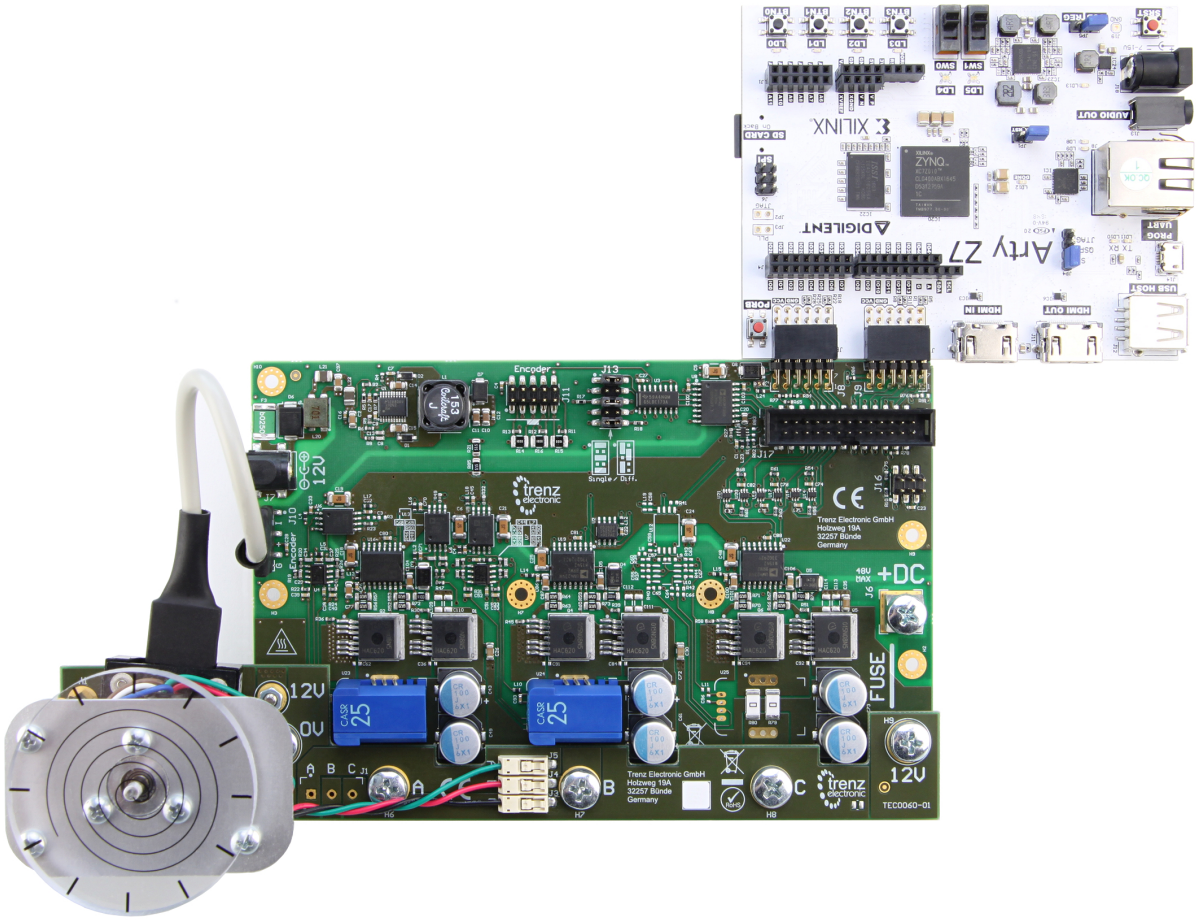

Figure 11: EDDP Kit assembly.

EDDP Kit Content

1. Control Board: ARTY-Z-7010
2. EDPS Board: TEC0053
3. Adapter Board: TEC0060
4. Reference Motor with Encoder: BLRW-111D-24V-10000-1000-SI
5. Plastic DEMO load for Motor
6. One 6 Pin PMoD cable
7. Two 12V Power Supplies
8. Screws and other accessories used to mount the motor
9. One spare M6 Screw
10. Plastic cover for Driver Board use without TEC0060
11. 30A Fuse for Driver Board use without TEC0060
12. Micro SD Card
13. Quickstart Guide

⚠ The Motor is pre-mounted to the EDPS Board using the Adapter Board and accessories.

Control Board

The default Control Board is the Digilent ARTY-Z 7010, which is delivered as part of the EDDP Kit. This manual contains information relevent to the actual use of the ARTY-Z as a Control Board within the EDDP only; all technical data and user guides and manuals for the Controller Board are provided by the controller board manufacturer (Digilent Inc.). Use of the other Control boards with the EDPS Board is also outside the scope of this manual. Primary support for other control boards is currently provided by QDESYS.

Software

The software delivered on the SD card configures the FPGA on the ARTY-Z board with the Field-Oriented Control algorithm and starts the web server to serve the Web UI.

To observe the IP address of the Control Board, open the USB serial console at the baud rate of 115200 shortly after powering up the Control Board. There should be boot messages on the console and they should contain the IP address shown on the following Figure:

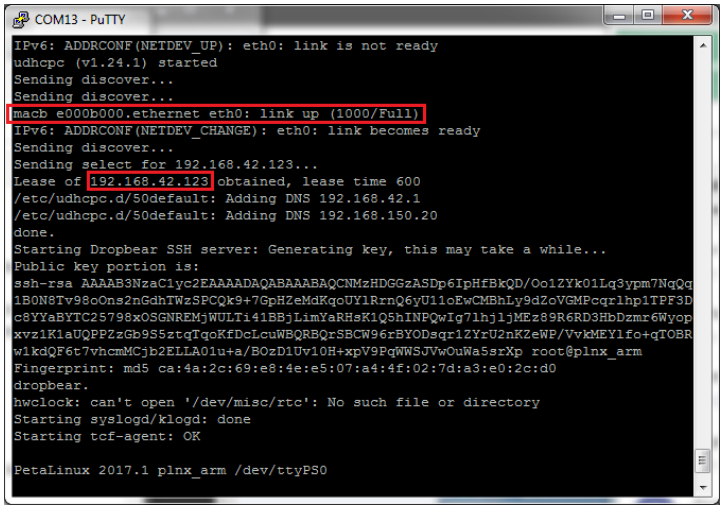

Figure 12: USB serial console log, with the network status message and IP address obtained via DHCP highlighted.

In the case the boot message was not seen for any reason, the network configuration can be seen by logging in as "root" with the password "root" and executing the command "ifconfig" as shown on the following figure:

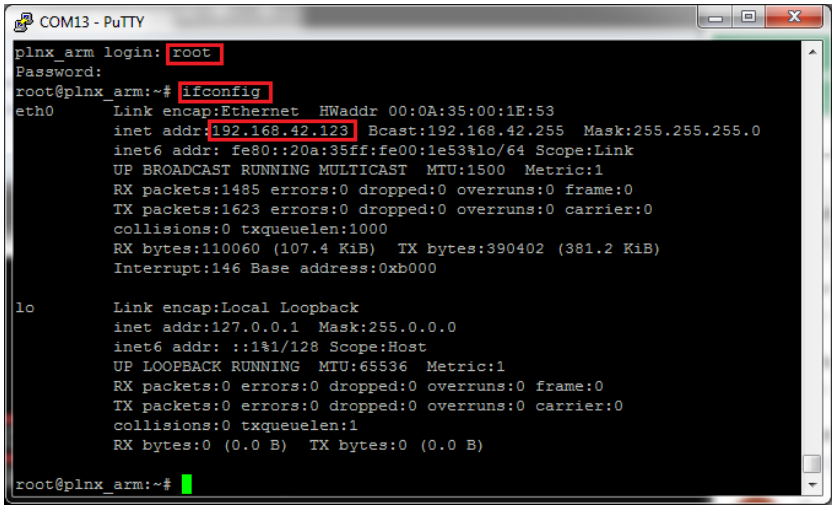

Figure 13: USB serial console, with login dialog, command "ifconfig" and the IP address highlighted.

To access the EDDP Web UI, enter IP address of the Control Board to the web browser address field. The following page appears:

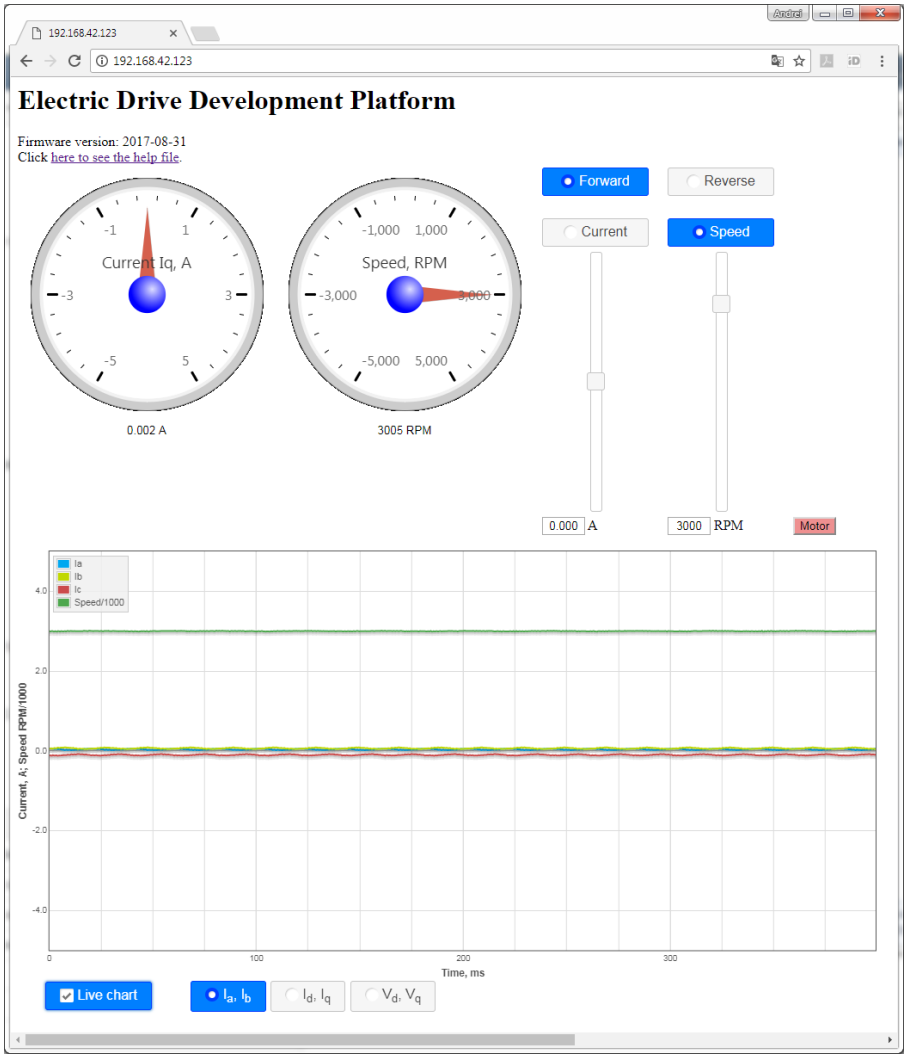

Figure 14: The Web UI.

To start the motor, click the button "Motor". The motor will make 3 rotations in order to make sure that encoder finds the initial position before starting in correct mode and the button will turn red. To stop the motor, click the button "Motor" again; the button will turn green.

The gauges show the stator current I_q and the motor speed in RPM.

To see the charts live, enable checkbox "Live charts". The following charts are available:

- I_a,I_b - shows stator currents I_a,I_b, the calculated current I_c and motor speed.
- I_d,I_q - shows stator currents I_d, I_q and motor speed.
- V_d,V_q - shows stator voltages V_d and V_q.

The radio buttons "Current" and "Speed" permit switching the control modes.

The sliders permit selecting the target speed and target current when in the appropriate mode. The direction radio buttons "Forward" and "Reverse" will be changed accordingly when the sign of the value is changed.

The radio buttons "Forward" and "Reverse" can be used to change the direction; the target slider will be changed accordingly.

Motor/Encoder

The Reference Motor is supplied in the EDDP Kit; see the chapter Reference Motor in the EDPS User Manual for details. Use of custom motors is outside the scope of this manual.

Functional description

A 3-phase permanent-magnet synchronous motor with attached encoder and mechanical load is mounted to a EDPS Board by using an Adapter Board. The EDPS Board is connected to a Control Board through PMOD connectors. A Host PC running a Web Browser connects to the Control Board through a Network.
On the EDPS Board, the 3-phase power stage drives the motor according to the PWM signal. The current transducers on the Driver Board transform the phase currents on 2 (optionally 3) phases into voltages, which, along with the DC Link voltage, are converted by ADC-s into a delta-sigma bitstream. The encoder signals and the sigma-delta bitstream are passed through the galvanic isolation to the Control Board. The PWM signal and ADC clock from the Control Board are passed through the galvanic isolation as well.
On the Control Board, the FPGA configuration is determined with the SDSoC Application built on top of the SDSoC Hardware Platform and the ARM Cortex-A9 CPU is running the Embedded Linux Code.
The SDSoC Hardware Platform provides a stream-oriented interface of the underlying hardware to the FOC algorithm. The streams are as follows:

1. The data stream to the FOC algorithm consists of the concatenated stream of rotor angle and motor speeds and the stream of discrete ADC samples.
2. The stream of PWM duty cycles from the FOC algorithm, which are converted to the PWM signals for the power stage.
3. The stream of monitor data from the FOC algorithm, which is captured and written to the DMA buffer in the main memory. This monitor data stream consists either of phase current data, stator current data or stator voltage data.

The SDSoC Application provides the FOC algorithm. The FOC algorithm operates on the AXI4 Stream to and from the SDSoC Hardware Platform and provides a set of AXI registers to control and monitor the status of the FOC algorithm. The control registers determine the FOC algorithm operating parameters and the source of the monitor data stream.

The Embedded Linux Code, running on the ARM Cortex-A9 CPU consists of the following:

1. The Linux OS, that manages the hardware and provides execution environment for the programs to run in, which includes a TCP/IP network stack. The drivers included provide access to the control and status registers of the FOC algorithm and to the DMA buffer of the monitor data stream.
2. The Network API, a server program, which provides an API built on top of Websockets protocol to control and monitor the FOC algorithm and to capture the monitor data stream.
3. The Web Server, which is used to host the Web UI.

The Web UI running in a web browser on the Host PC enables use of the EDDP Kit from anywhere in the network.

Block Diagram

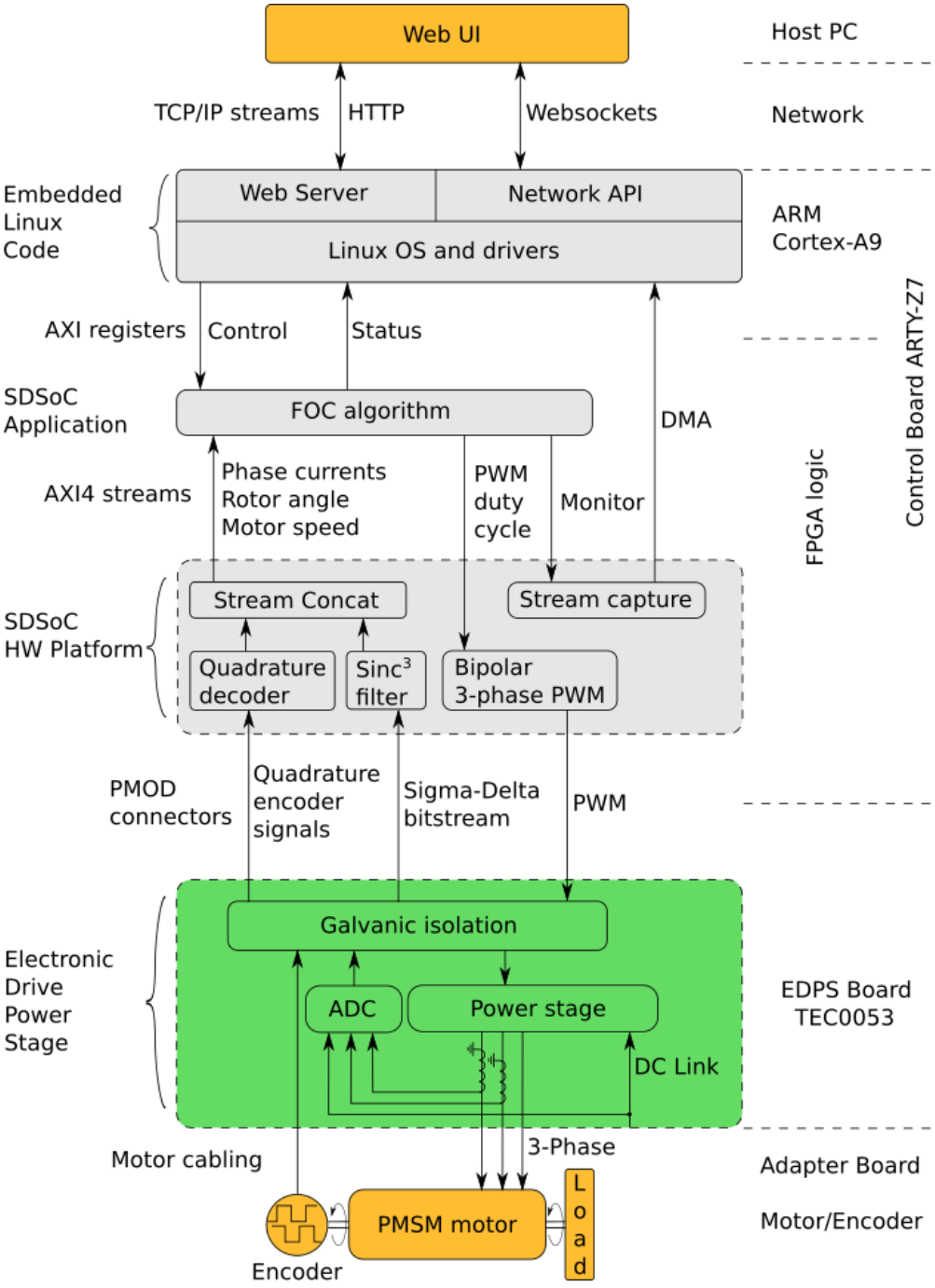

Figure 15: Block diagram of the EDDP.

FPGA resources utilization

An excerpt of the FPGA resource utilization by the FOC SDSoC Application Project is shown in the Table 2. The FPGA used on the Controller Board is Xilinx 7z010clg400-1.

The power draw of the design is about 220mW as measured by the increase of the power draw of the Control Board after configuring the FPGA.

Type	Used	Available	Util%
Slice LUTs	5758	17600	32.72
Slice Registers	7277	35200	20.67
F7 Muxes	33	8800	0.38
RAMB36/FIFO	21	60	35
RAMB18	4	120	3.33
DSP48E1	34	80	42.50
BUFGCTRL	4	32	12.50
MMCME2_ADV	1	2	50

Table 2: FPGA resources utilization.

List of additional documents

The additional documents, listed in the Table 3, can be downloaded from Trenz EDDP Web Hub:

http://trenz.org/EDDP

Title	Description
FOC SDSoC	Implementation of a Field-Oriented Control algorithm in C++ with Vivado SDSoC
SDSoC Hardware Platform ARTY-Z7	A basis for building Vivado SDSoC applications running on an Arty-Z7 board connected to a TEC0053 board
AXI4-Stream AD7403	An IP core for filtering the delta-sigma bitstream read from one or more ADC-s of type of AD7403 to an AXI4-Stream of samples
AXI4-Stream Encoder	An IP core for converting impulses from a relative index encoder with an index signal to an AXI4-Stream of position and speed data
AXI4-Stream PWM	An IP core for generating PWM signals according to the input AXI4-Stream
AXI4-Stream Concat	An IP core for concatenating AXI4-Streams
Web GUI	A Web UI to control and monitor an EDPS Board over the Network API
Network API	A communication protocol, based on Websockets, to control an EDPS board
Embedded Linux Code	A server program interfacing to an EDPS board and implementing the Network API and the functions of a Web Server

Table 3: List of additional documents.

References

All resource links for other relevant documents and websites are available from Trenz EDDP Web Hub:

http://trenz.org/EDDP

Document Change History

Date	Revision	Contributors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	Unknown macro: 'metadata'	Jan Kumann	General formatting changes and small corrections.
2017-08-14	v.10	Antti Lukats, Andrei Errapart	Initial document.

Table 4: Document change history.

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REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.