

# TE0791 TRM

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## Overview

The Trezz Electronic TE0791-01 is an adapter board for use with the XMOD [TE0790](#) board. The adapter board provides several connector types to get access to the signals and interfaces of the XMOD board. As further option footprints are available for JST Wire-To-Board IDC connectors with two different pin-assignments.

## Key Features

- Xmod form-factor
  - size: 20 x 25 mm
  - M3 mounting hole
- Different connector types available
  - 2x6 PMOD connector
  - JTAG 1-row pin header female
  - 2x optional JST Wire-To-Board 6-pin IDC connector
  - 2x optional JST Wire-To-Board 10-pin IDC connector
  - IDC connectors with different pin-assignment each

## Block Diagram

# TE0791-01

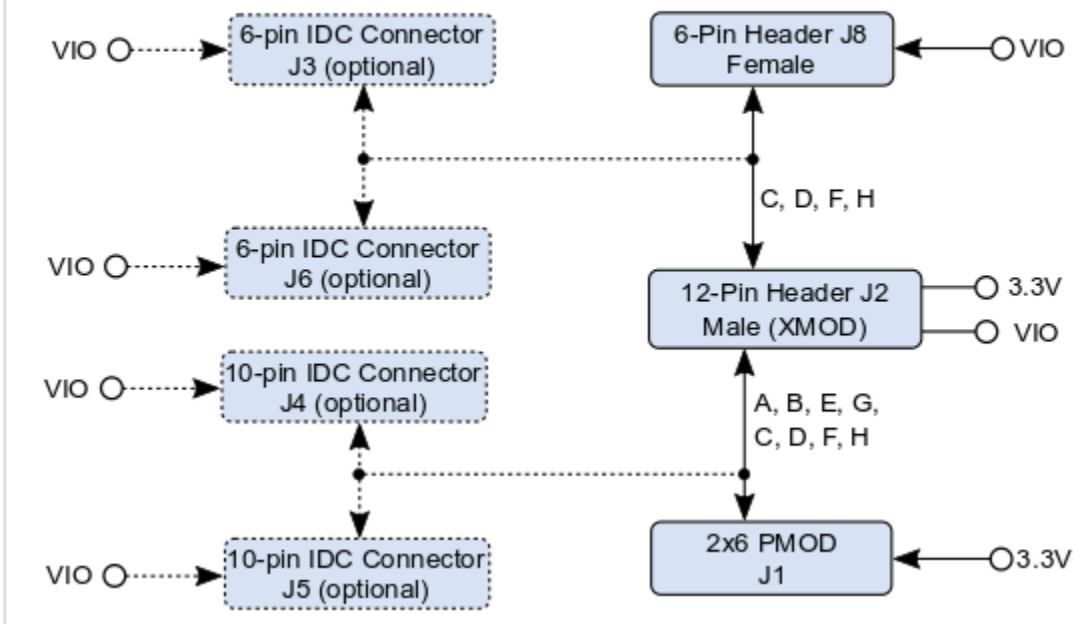


Figure 1: TE0791-01 block diagram.

## Main Components

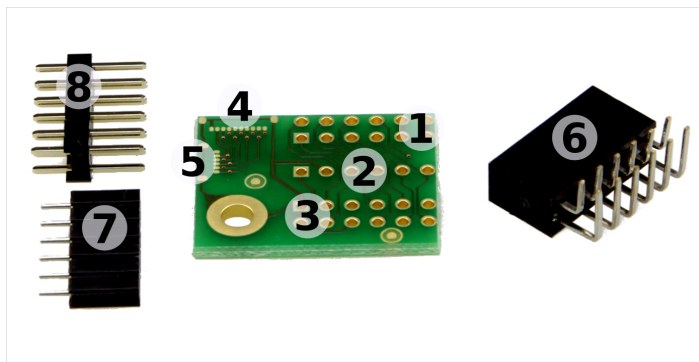


Figure 2: TE0790-02 main components. Top side view

1. 2x6 PMOD connector solder pads, J1 (on bottom side)
2. 6-Pin header solder pads, J8
3. 12-Pin header solder pads, J2
4. 10-pin IDC connector solder pads, J4 (solder pads J5 on bottom side)
5. 6-pin IDC connector solder pads, J3 (solder pads J6 on bottom side)
6. 2x6 PMOD connector
7. 1-row 6-pin header female (2.54 mm pitch)
8. 2-row 12-pin header male (2.54 mm pitch)

# Signals, Interfaces and Pins

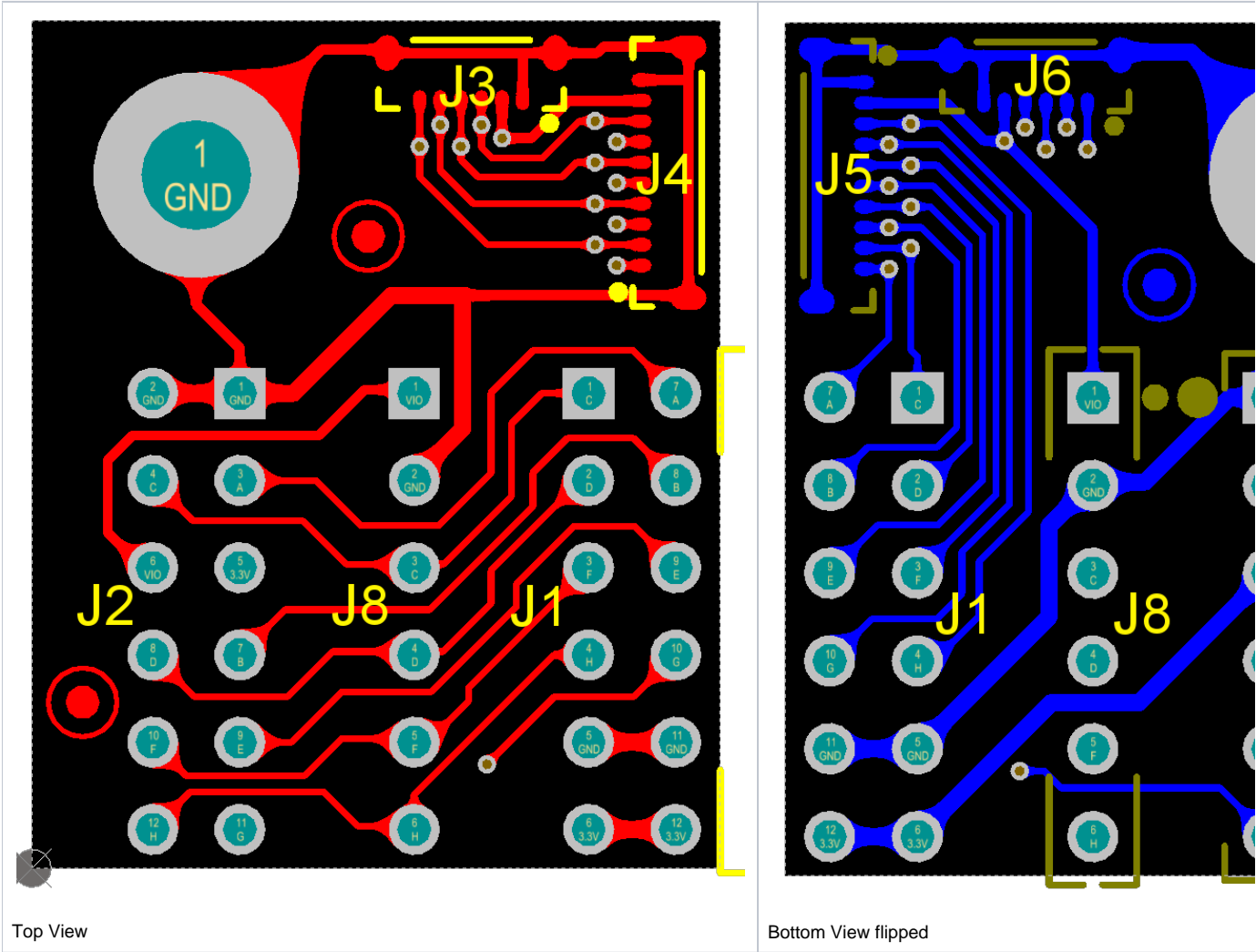


Figure 3: Connector Location

## 2x6 Pin Header

The 2x6 pin header (2.54mm grid size, male) J2 of the TE0791 board have to be connected to the corresponding XMOD pin header on the TE0790 board. The signal assignment of the pin header on the TE0790 board depends on the configuration of its System Controller CPLD firmware.

The pin assignment on the TE0791 adapter board is the same as on the TE0790 XMOD board:

Signal	J2 Pin Name	J2 Pin Name	Signal
GND		1*	GND
User Defined	C	A	User Defined
VIO			VDD 3.3V

User Defined	D	B	User Defined
User Defined	F	E	User Defined
User Defined	H	G	User Defined / Button (Reset_n)

**Table 1:** Pin header J2 signal assignment. \*pin 1 on header J2 of the adapter board

## 1x6 Pin Header

On the female 1-row 6-pin header (2.54mm grid size, female) J8 are the XMOD signals C, D, F and H available. At standard System Controller CPLD firmware, this signals create the JTAG interface of the XMOD board:

J8 Pin Number	J8 Pin Name	Signal	Note
1	VIO	VCCIO	check TE0790 DIP-switch settings
2	GND	Ground	-
3	C	TCK	-
4	D	TDO	-
5	F	TDI	-
6	H	TMS	-

**Table 2:** Pin header J8 signal assignment with standard TE0790 CPLD firmware

## 2x6 PMOD Header

On the 2x6 PMOD header J1 are all XMOD signals A - H available. The pin- and signal-assignment with standard System Controller CPLD firmware of the XMOD board are as follows:

Note	Signal	J1 Pin Name	J1 Pin Number	J1 Pin Number	J1 Pin Name	Signal	Note
-	UART TXD	A	7	1	C	TCK	-
-	UART RXD	B	8	2	D	TDO	-
usable as GPIO	LED on TE0790	E	9	3	F	TDI	-
usable as GPIO	Button on TE0790	G	10	4	H	TMS	-
-	Ground	GND	11	5	GND	Ground	-
check TE0790 DIP-switch settings	VCC / VCCIO	3.3V	12	6	3.3V	VCC / VCCIO	check TE0790 DIP-switch settings

**Table 3:** PMOD J1 signal assignment with standard TE0790 CPLD firmware

## 10-pin IDC Connector

On the TE0791 board are footprints available for 10-pin JST Wire-To-Board IDC connectors J4 and J5 with two different pin-assignments, where all XMOD signals A - H are available. The pin- and signal-assignment with standard System Controller CPLD firmware of the XMOD board are as follows:

Pin Name	J4 Pin Number	J5 Pin Number	Signal	Note
A	1	10	UART TXD	
B	3	8	UART RXD	-
C	2	9	TCK	-
D	4	7	TDO	-
E	5	6	LED on TE0790	usable as GPIO

F	6	5	TDI	-
G	7	4	Button on TE0790	usable as GPIO
H	8	3	TMS	-
VIO	9	2	VCC / VCCIO	check TE0790 DIP-switch settings
GND	10	1	Ground	-

**Table 4:** IDC connector J4 and J5 signal assignment with standard TE0790 CPLD firmware

## 6-pin IDC Connector

On the TE0791 board are footprints available for 6-pin JST Wire-To-Board IDC connectors J3 and J6 with two different pin-assignments, where the XMOD signals C, D, F and H are available. At standard System Controller CPLD firmware, this signals create the JTAG interface of the XMOD board:

Pin Name	J3 Pin Number	J6 Pin Number	Signal	Note
C	6	1	TCK	-
D	5	2	TDO	-
F	4	3	TDI	-
H	3	4	TMS	-
VIO	2	5	VCC / VCCIO	check TE0790 DIP-switch settings
GND	1	6	Ground	-

**Table 5:** IDC connector J3 and J6 signal assignment with standard TE0790 CPLD firmware

## Technical Specification

### Physical Dimensions

- Module size: 24,65mm x 20,02mm. Please download the assembly diagram for exact numbers.
- Mating height with standard pin headers: 9.5 mm.
- PCB thickness: 1.6 mm.
- Highest part on PCB: approx. 7 mm on top side, 5 mm on bottom side. Please download the step model for exact numbers.

All dimensions are given in millimeters and mil.

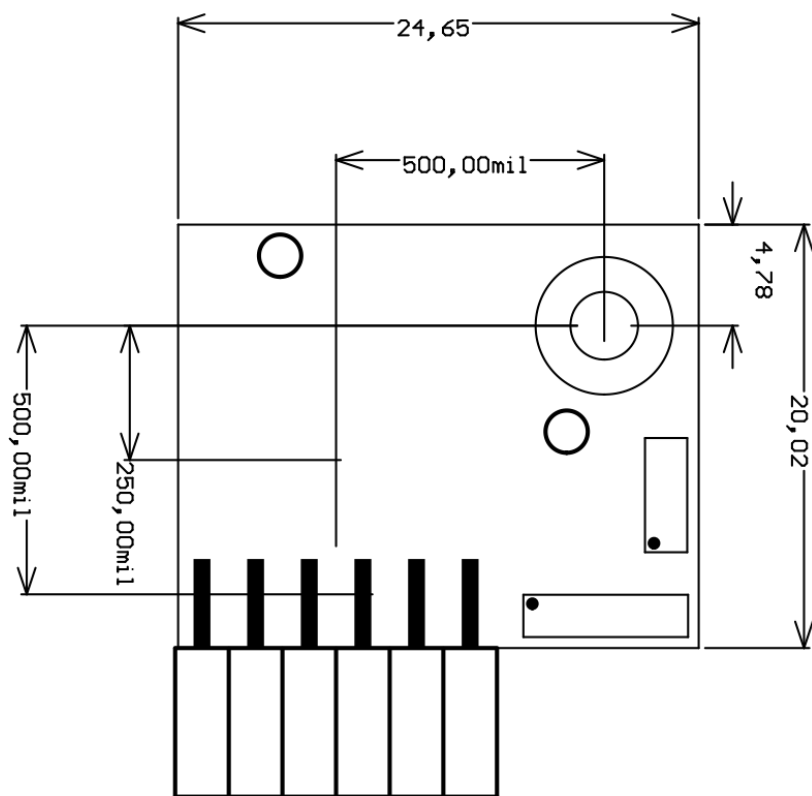


Figure 4: Board physical dimensions drawing.

## Revision History


### Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
-	01	current available revision	-	<a href="#">TE0791-01</a>

Table 6: Board hardware revision history.

### Document Change History

Date	Revision	Contributors	Description
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<div> <div> Error rendering macro 'page-info' </div> <div> <p>Ambiguous method overloading for method jdk.  proxy241.\$Proxy3496#hasContentLevelPermission.  Cannot resolve which method to invoke for [null, class  java.lang.String, class com.atlassian.confluence.pages.  Page] due to overlapping prototypes between: [interface  com.atlassian.confluence.user.ConfluenceUser, class  java.lang.String, class com.atlassian.confluence.core.  ContentEntityObject] [interface com.atlassian.user.User,  class java.lang.String, class com.atlassian.confluence.  core.ContentEntityObject]</p> </div> </div>	<div> <div>  Unknown macro: 'metadata' </div> </div>	John Hartfiel	<ul style="list-style-type: none"> <li>add Figure 3: Connector Location</li> </ul>
2017-10-19	v.9	Ali Naseri	<ul style="list-style-type: none"> <li>initial document</li> </ul>

**Table 7:** Document change history.

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Ambiguous method overloading for method `jdk.proxy241.$Proxy3496#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`