

TE0630 B2B Connector Pin Description

This section describes how the various pins on B2B connectors J4 and J5 are connected to TE0630 on-board components. There are four main signal types connected to B2B connectors:

- FPGA users signals;
- USB signals;
- Power signals;
- System reset signals.

 **TE0303 Prototyping Carrier Board connection with TE0300 module**

The connection between TE0630 module connectors J(M)4/J(M)5 and TE0303 Prototyping Carrier Board connectors J1/J2/J3/J4 is documented [here](#). TE0300 modules and TE0630 modules fit onto the same TE0303 Prototyping Carrier Board.

 **TE0304 Application Demo Carrier Board connections with TE0300 module**

The connection between TE0630 module connectors J(M)4/J(M)5 and TE0304 Application Demo Carrier Board connectors J1/J2/J3/J4 is documented [here](#). TE0300 modules and TE0630 modules fit onto the same TE0304 Application Demo Carrier Board.

Pin Labelling

FPGA user signals connected to B2B connectors are characterized by the "Vx_IO_yy_p" naming convention, where:

- Vx defines the FPGA bank (x = bank number);
- IO defines an "FPGA to B2B" signal type;
- yy defines a differential pair or signal number (yy = pair number);
- p defines a differential signal polarity (P = positive, N = negative); single ended signals do not have this field.

Remaining signals use custom names.

Pin Types

Most pins of B2B connectors J4 and J5 are general-purpose, user-defined I/O pins (GPIOs). There are, however, up to ~~5~~ 8 different functional types of pins on the TE0630, as outlined in the tables J4 below. In pin-out tables Table J4 and Table J5, the individual pins are colour-coded according to pin type as defined in the table below.

type colour code	description
DIO	Unrestricted, general-purpose differential user-I/O pin.
SIO	Unrestricted, general-purpose user-I/O pin.
CIO	Unrestricted, general-purpose differential user-I/O pin. This pin also can be used as FPGA clock input.
USB	USB signals.
JTAG	Dedicated JTAG signals.
GND	Dedicated ground pin. All must be connected.
SYS	System signal. See the description of each pin in the user manual for additional information on the corresponding signals.
POW	Power signals.

TE0630 pin types

B2B Connector Pin-Outs

Connector J4: Pin-Out Information

J4 pin	Net	Type	FPGA pin	Net Length (mm)	J4 pin	Net	Type	FPGA pin	Net Length (mm)
1	VCCIO0	POW	-	-	2	VCCIO0	POW	-	-
3	VCCIO0	POW	-	-	4	VCCIO0	POW	-	-
5	V3_IO_01	SIO	G6	13.30	6	V3_IO_06	SIO	C4	15.26
7	V3_IO_02	SIO	G4	11.05	8	V3_IO_07	SIO	D3	17.04
9	V3_IO_03	SIO	F5	10.46	10	V3_IO_08	SIO	E6	14.97
11	V3_IO_04	SIO	E5	10.08	12	V3_IO_09	SIO	D5	13.84
13	GND	GND	-	-	14	GND	GND	-	-
15	V3_IO_05	SIO	F7	10.16	16	V0_IO_11_P	DIO	B6	12.29
17	V0_IO_01	SIO	A4	5.16	18	V0_IO_11_N	DIO	A6	10.84
19	V0_IO_01_N	DIO	A5	5.14	20	V0_IO_12_N	DIO	A7	10.95
21	V0_IO_01_P	DIO	C5	6.84	22	V0_IO_12_P	DIO	C7	12.30
23	GND	GND	-	-	24	GND	GND	-	-
25	V0_IO_02_N	DIO	C6	7.27	26	V0_IO_13_N	DIO	A8	10.41
27	V0_IO_02_P	DIO	D6	8.16	28	V0_IO_13_P	DIO	B8	11.74
29	V0_IO_03_P	DIO	D7	7.93	30	V0_IO_14_N	DIO	A9	10.40
31	V0_IO_03_N	DIO	C8	7.21	32	V0_IO_14_P	DIO	C9	12.81
33	3.3V	POW	-	-	34	3.3V	POW	-	-
35	V0_IO_04_P	DIO	D9	9.34	36	V3_IO_10	SIO	M7	21.84
37	V0_IO_04_N	DIO	D8	10.08	38	V0_CLK_04_N	CIO	C12	12.96
39	V0_CLK_03_P	CIO	B12	6.00	40	V0_CLK_04_P	CIO	D11	13.32
41	V0_CLK_03_N	CIO	A12	05.01	42	V0_CLK_01_N	CIO	A10	10.97
43	GND	GND	-	-	44	V0_CLK_01_P	CIO	B10	11.84
45	V0_CLK_02_P	CIO	C11	7.93	46	GND	GND	-	-
47	V0_CLK_02_N	CIO	A11	10.76	48	V0_IO_15_N	DIO	A15	11.79
49	V0_IO_05_P	DIO	C13	7.20	50	V0_IO_15_P	DIO	C15	13.66
51	V0_IO_05_N	DIO	A13	6.11	52	V3_IO_11	SIO	M8	26.06
53	2.5V	POW	-	-	54	2.5V	POW	-	-
55	V0_IO_06_P	DIO	D10	12.84	56	V0_IO_16_P	DIO	B16	12.98
57	V0_IO_06_N	DIO	C10	13.09	58	V0_IO_16_N	DIO	A16	10.96
59	V0_IO_07_P	DIO	F10	16.22	60	V0_IO_17_P	DIO	C17	16.33
61	V0_IO_07_N	DIO	E10	15.43	62	V0_IO_17_N	DIO	A17	13.51
63	GND	GND	-	-	64	GND	GND	-	-
65	V0_IO_08_N	DIO	A14	8.21	66	V0_IO_18_P	DIO	B18	15.19
67	V0_IO_08_P	DIO	B14	9.11	68	V0_IO_18_N	DIO	A18	13.77
69	V0_IO_09_N	DIO	C14	9.40	70	TDI	JTAG	E18	-
71	V0_IO_09_P	DIO	D15	9.40	72	TDO	JTAG	E14	-
73	1.2V	POW	-	-	74	1.2V	POW	-	-
75	V0_IO_10_N	DIO	C16	9.65	76	TCK	JTAG	D14	-
77	V0_IO_10_P	DIO	D17	9.58	78	TMS	JTAG	E16	-

79	GND	GND	-	-	80	GND	GND	-	-
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J4 connector pin-out

Connector J5: Pin-Out Information

J5 pin	Net	Type	FPGA pin	Net Length (mm)	J5 pin	Net	Type	FPGA pin	Net Length (mm)
1	5Vb2b	POW	-	-	2	5Vb2b	POW	-	-
3	5Vb2b	POW	-	-	4	5Vb2b	POW	-	-
5	5V	POW	-	-	6	/MR	SYS	-	-
7	B2B_D_P	USB	-	-	8	/RESET	SYS	-	-
9	B2B_D_N	USB	-	-	10	RESET	SYS	-	-
11	GND	GND	-	-	12	GND	GND	-	-
13	V3_IO_12	SIO	T2	19.97	14	V3_IO_16	SIO	U1	10.26
15	V3_IO_13	SIO	T1	18.91	16	V3_IO_17	SIO	U3	11.74
17	V2_IO_01	SIO	V15	18.18	18	V3_IO_18	SIO	V1	9.72
19	V3_IO_14	SIO	AA2	16.26	20	V3_IO_19	SIO	V2	10.03
21	V3_IO_15	SIO	AB2	15.23	22	V3_IO_20	SIO	Y1	9.21
23	GND	GND	-	-	24	GND	GND	-	-
25	V2_IO_01_N	DIO	AB6	10.68	26	V3_IO_21	SIO	Y2	8.73
27	V2_IO_01_P	DIO	AA6	12.54	28	V3_IO_22	SIO	AB3	6.68
29	V2_IO_02_P	DIO	Y7	13.32	30	V3_IO_23	SIO	Y3	8.38
31	V2_IO_02_N	DIO	AB7	11.56	32	V3_IO_24	SIO	AB4	6.65
33	V3_IO_27	SIO	U8	8.41	34	V3_IO_25	SIO	AA4	7.51
35	3.3V	POW	-	-	36	3.3V	POW	-	-
37	V2_IO_03_N	DIO	AB8	12.43	38	V3_IO_26	SIO	Y4	8.41
39	V2_IO_03_P	DIO	AA8	13.01	40	V2_IO_10_P	DIO	W6	9.20
41	V2_IO_02	SIO	AB12	12.62	42	V2_IO_10_N	DIO	Y6	8.31
43	GND	GND	-	-	44	GND	GND	-	-
45	V2_CLK_01_N	CIO	AB11	11.34	46	V2_IO_11_N	DIO	Y8	8.09
47	V2_CLK_01_P	CIO	Y11	12.64	48	V2_IO_11_P	DIO	W9	9.10
49	V2_IO_04_P	DIO	W15	14.63	50	V2_IO_12_P	DIO	Y9	8.40
51	V2_IO_04_N	DIO	Y16	12.42	52	V2_IO_12_N	DIO	AB9	6.60
53	2.5V	POW	-	-	54	2.5V	POW	-	-
55	V2_IO_05_N	DIO	U14	17.21	56	V2_CLK_02_N	CIO	AB10	7.26
57	V2_IO_05_P	DIO	T14	18.75	58	V2_CLK_02_P	CIO	AA10	8.16
59	V2_IO_06_P	DIO	AA14	12.39	60	V2_IO_13_P	DIO	W11	11.39
61	V2_IO_06_N	DIO	AB14	11.34	62	V2_IO_13_N	DIO	Y10	10.30
63	GND	GND	-	-	64	GND	GND	-	-
65	V2_IO_07_N	DIO	AB15	11.87	66	V2_IO_14_N	DIO	Y12	9.80
67	V2_IO_07_P	DIO	Y15	13.55	68	V2_IO_14_P	DIO	W12	10.80
69	V2_IO_08_P	DIO	AA16	12.61	70	V2_IO_15_P	DIO	Y13	10.20
71	V2_IO_08_N	DIO	AB16	11.72	72	V2_IO_15_N	DIO	AB13	8.40
73	1.2V	POW	-	-	74	1.2V	POW	-	-
75	V2_IO_09_N	DIO	AB18	11.91	76	V2_IO_16_N	DIO	Y14	9.72
77	V2_IO_09_P	DIO	AA18	12.57	78	V2_IO_16_P	DIO	W14	10.72
79	GND	GND	-	-	80	GND	GND	-	-

J5 connector pin-out

Signal integrity considerations

Traces of differential signals pairs are routed symmetrically (as symmetric pairs).

Traces of differential signals pairs are NOT routed with equal length (difference in signal lines length is negligible for used signal frequency). For applications where traces length has to be matched or timing differences have to be compensated, Table J4 and Table J5 (above) list the trace length of I/O signal lines measured from FPGA balls to B2B connector pins.

Traces of differential signals pairs are routed with a differential impedance between the two traces of 100 ohm. Single ended traces are routed with 60 ohm impedance.

An electronic version of these pin-out tables are available for download from the Trenz Electronic support area of the web site.