TEBF0808 Slave CPLD

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Overview

Firmware for PCB-Slave CPLD with designator U39. Second CPLD Device in Chain: LCMX02-1200HC

Feature Summary

- Power Management
- Reset Management
- Boot Mode
- LEDs
- RGPIO
- SD Selection
- UART

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Description
1.8V_EN / EN_1V8	out	106	Power
5V_EN / EN_5V	out	115	Enable 5V, can be permanently enabled by S4-4
C_TCK		131	JTAG J28 (XMOD2) / internal currently_not_used
C_TDO		137	JTAG J28 (XMOD2) / internal currently_not_used
C_TDO1		136	JTAG J28 (XMOD2) / internal currently_not_used
C_TMS		130	JTAG J28 (XMOD2) / internal currently_not_used
CLK_A / AUD_CLK	out	1	AUDIO U3 CLK
CLK_CPLD / MEMS_CLKIN	in	128	U25 24,576MHz
DONE	in	67	PS Done
EN_DDR	out	86	Enable DDR Power
EN_FMC / FMC_EN	out	104	FMC
EN_FPD	out	81	Enable PS FPD Power
EN_GT_L	out	77	Enable GT Power
EN_GT_R	out	93	Enable GT Power
EN_LPD	out	84	Enable PS LPL Power
EN_PL	out	95	Enable PL Power
EN_PLL_PWR	out	78	Enable SI5345 Power
EN_PSGT / EN_PSGTR	out	75	Enable PS GT Power
ERR_OUT / ERROR	in	70	PS Error Out / Status / readable via RGIO
ERR_STATUS / ERROR_STAT	in	69	PS Error Status / Status / readable via RGIO
F1PWM	out	121	FAN1
F1SENSE	in	125	FAN1
FAN_FMC_EN / FMC_FAN_EN	out	132	FMC FAN
FMC_PG_C2M	out	141	FMC PG
HD_LED_N / HDLED_N	out	112	J10 HD LED
HD_LED_P / HDLED_P	out	110	J10 HD LED
HDIO_SC0 / SC0	in	32	FPGA IO / forward to HD_LED_P / HDLED_P
HDIO_SC1 / SC1	in	33	FPGA IO / currently_not_used
HDIO_SC2 / SC2	in	34	FPGA IO / currently_not_used
HDIO_SC3 / SC3	out	35	FPGA IO / currently_not_used
HDIO_SC4 / SC4	out	25	FPGA IO / currently_not_used
HDIO_SC5 / SC5	out	26	FPGA IO / RGPIO
HDIO_SC6 / SC6	in	27	FPGA IO / RGPIO CLK
HDIO_SC7 / SC7	in	28	FPGA IO / RGPIO
I2C_SCL / SCL	in	50	I2C / currently_not_used
I2C_SDA / SCA	in	52	I2C / currently_not_used
INIT_B / INIT	in	68	PS init B

JTAGENB		120	external Pin for CPLD Firmware Update
LP_GOOD / PG_LPD	in	83	LP Power Good
MIO24		38	MIO / currently_not_used
MIO25		39	MIO / currently_not_used
MIO30	in	48	MIO / force reboot after FSBL-PLL config for PCIe
MIO31	in	49	MIO / PCIe reset
MIO32		40	MIO / currently_not_used
MIO33		41	MIO / currently_not_used
MIO34		42	MIO / currently_not_used
MIO35		43	MIO / currently_not_used
MIO36		44	MIO / currently_not_used
MIO37		45	MIO / currently_not_used
MIO40	in	54	MIO / forwarded to PWRLED_P / LED_P
MIO41		55	MIO / currently_not_used
MIO42	out	60	FPGA UART RX
MIO43	in	61	FPGA UART TX
MIO44	out	47	MIO / SD_WP to FPGA
MOD_EN	out	119	Module Power 3.3V Enable
MODE0	out	6	Boot Mode
MODE1	out	9	Boot Mode
MODE2	out	10	Boot Mode
MODE3	out	11	Boot Mode
MR / MRESETn	out	92	PS Reset
PCI_SFP_EN	out	76	SFP
PER_EN	out	117	Baseboard Power 3.3V Enable
PERST / PERSTn	out	139	PCIE Resetn
PG_DDR	in	91	Power Good / Status / readable via RGIO
PG_FPD	in	85	Power Good / Status / readable via RGIO
PG_GT_L	in	96	Power Good / Status / readable via RGIO
PG_GT_R	in	94	Power Good / Status / readable via RGIO
PG_PL	in	82	Power Good / Status / readable via RGIO
PG_PLL_1V8 / PG_PLL	in	73	Power Good / Status / readable via RGIO
PG_PSGT	in	74	Power Good / Status / readable via RGIO
PLL_LOLN / PLL_LOL	in	58	Module U5 Si5345 / readable via RGIO / currently_not_used
PLL_RST / PLL_RSTn	out	56	Module U5 Si5345
PLL_SEL0	out	57	Module U5 Si5345
PLL_SEL1	out	59	Module U5 Si5345
POK_1V8	in	107	Power
POK_FMC	in	99	FMC Power/ readable via RGIO
PROG_B	inout	71	PS_PROG_B

PSON	out	105	ATX J20 PS_ON_N
PWR_BTN	in	113	Power Button S1 or J10
PWRLED_N / LED_N	out	111	J10 PWR
PWRLED_P / LED_P	out	109	J10 PWR
PWROK	in	100	ATX J20 PWROK / readable via RGIO
RST_BTN	in	114	Reset Button S2 or J10
S_1		127	Beeper/ currently_not_used
SC_IO0 / X0	out	12	Master-Slave SC-Communication / Power Reset
SC_IO1 / X1	out	13	Master-Slave SC-Communication / Power Reset
SC_IO2 / X2	out	14	Master-Slave SC-Communication / currently_not_used
SC_IO3 / X3	out	20	Master-Slave SC-Communication / currently_not_used
SC_IO4 / X4	in	21	Master-Slave SC-Communication /MMC SD WP
SC_IO5 / X5	in	22	Master-Slave SC-Communication / currently_not_used
SC_IO6 / X6	in	23	Master-Slave SC-Communication / Sanity check from other CPLD (FMC VADJ Enable)
SC_IO7 / X7	in	24	Master-Slave SC-Communication / Sanity check from other CPLD (FMC VADJ Enable)
SC_IO8 / dummy		126	/ currently_not_used / ! not available on PCB REV2 !
SC2_SW1	in	133	S5-1 / Boot Mode Selection / readable via RGIO
SC2_SW2	in	138	S5-2 / Boot Mode Selection / readable via RGIO
SD_A_EN	out	140	Micro SD
SD_B_EN	out	122	MMC SD
SD_CD / SD_CD_OUT	out	65	SD Card detect to FPGA
SD_CD_B	in	143	MMC SD / readable via RGIO
SD_CD_S	in	142	Micro SD / readable via RGIO
SEL_SD / SD_SEL	out	62	Select SD
SRST_B / SRSTn	out	19	PS_SRST_B
STAT_LED2 / LED2	out	98	LED D6 Green
STAT_LED3 / LED3	out	97	LED D7 Red
XMOD2_A / XMOD_TXD	out	5	J12 (XMOD 1)
XMOD2_B / XMOD_RXD	in	4	J12 (XMOD 1)
XMOD2_E / XMOD_LED	out	3	J12 (XMOD 1)
XMOD2_G / XMOD_BTN	in	2	J12 (XMOD 1) / readable via RGIO

Functional Description

JTAG

JTAGENB set carrier board CPLD into the chain for firmware update. For Update set DIP S4-3 to ON.

Power

PSON signal will be enabled/disabled after delay, when Power Button is pressed. Power Button is debounced.

Stage	Power Enable Signal	Enable Power domain	Note
1	PSON	ATX PSON (12V from ATX power supply)	Signal will be enabled/disabled after delay, when Power Button is pressed.Power Button is debounced.
2	PWROK(ATX Power)	5V_EN (5V)	Note 1: If S4-4 is on, 5V is always on. S4-4 must be on, if TEBF0808 is used with external 12V instead of ATX Power. Note 2: CPLD Pullup is used for PWROK to works without external 12V only.
2	PWROK	MOD_EN (Module 3.3V), EN_LPD, EN_FPD, EN_PL	Module B2B connector Main Power and enables
3	PG_FPD	EN_DDR, EN_PLL_PWR, EN_PSGTR	Module periphery power
3	PG_PL	EN_GT_R, EN_GT_L	Module periphery power
4	PG_FPD and PG_PL	PER_EN(Periphery 3.3V), EN_1V8(Periphery 1.8V), PCI_SFP_EN (PCIe and SFP)	Carrier periphery power
4	PWROK and PG_FPD and PG_PL and PSON and Master CPLD status	FMC_EN (FMC VADJ)	FMC VADJ
5	PWROK and PG_FPD and PG_PL and PSON and POK_FMC(VADJ)	FMC_PG_C2M	FMC supply power status to FMC connector

Note: Power Status is visible on LEDs, see LED section

⚠ TE0808 module is not completely powered off with power button, if 12V power jack (J25) is used for power supply. 12V Power ON/OFF is only with ATX power supply usable.

Enable

SD's will be enabled by PWROK and PG_FPD and PG_PL and PSON;.

FMC_FAN_EN will be enabled by PWROK and PG_FPD and PG_PL and PSON_i or RGPIO (11) controlled, when active. F1PWM is constant on.

Reset

Power Button is debounced.

Reset will be also set via modified FSBL, if PCIe is detected.

Name	Description
PLL_RSTn	not RGPIO (0) when active else '1'
SRSTn	'1'
MRESETn	RST_BTN and PWROK and PG_FPD and PG_PL and PSON and "PS reboot via FSBL"
PERSTn	not RGPIO (1) and MIO31 when active else rst_btn_i and MIO31
Master CPLD Reset	PWROK and PG_FPD and PG_PL and PSON and Reset Button over CPLD interconnect.
PS reboot via FSBL	Reboot possible over FSBL over MIO30 (need for proper PCI initialization on first power on without press Reset Button)

Note: Reset Status is visible on LEDs, see LED section

Boot Mode

S5-1	S5-2	Description

ON	ON	Default, boot from SD/microSD or SPI Flash if no SD is detected
OFF	ON	Boot from eMMC
ON	OFF	Boot mode PJTAG0
OFF	OFF	Boot mode main JTAG

Note: Boot Mode Status is visible on LEDs, see LED section

UART

XMOD_TXD is sourced by MIO43 and MIO42 by XMOD_RXD.

Module SI5345

Module U5 Selection Pins are constant zero.

SD Card

SD Card selection is done via Micro SD Card detection.

SD WP is forwarded to ZynqMP from Master CPLD.

RGPIO

RGPIO Pin to FPGA	Value
0	SW1
1	SW2
2	XMOD_BTN
3	Force FSBL reboot done
4	SD_CD_S
5	SD_CD_B
6	Error
7	ERR_STAT
11-8	Boot Mode
12	PG_LPD
13	PG_DDR
14	PG_FPD
15	PG_PSGT
16	PG_GT_L
17	PG_GT_R
18	POK_FMC
19	DET_POWROK

20	PWROK
21	PG_PL
22	PG_PLL
23	PLL_LOL
24-27	reserved
28-31	Interface detection

RGPIO Pin from FPGA	Value
0	PLL_RSTn
1	PERSTn
2	FMC_FAN_EN
7	LED_N
8	LED_P
9	HDLED_N
10	HDLED_P
12-23	unused
24-27	reserved
28-31	Interface detection

LED

LED2 D6 Green (near FAN1 connector on PCB)		
Power Flags	**Blink Sequence**	**Comment**
PWROK	********	ATX Power failed or PCB is powered off
PG_LPD	*****ooo	Module Low Power Domain failed
PG_FPD	****oooo	Module Full Power Domain failed
PG_PL	***ooooo	Module PL Power Domain failed
POK_1V8 or POK_FMC	**oooooo	Carrier 1V8 or FMC VADJ Power Domain failed
PG_DDR='0' or PG_GT_L='0' or PG_GT_R='0' or PG_PSGT='0' or PG_PLL='0'	*ooooooo	Module DDR, PL GT, PS GT or PLL Power Domain failed
	OFF	All Ready

LED3 D7 Red (near FAN1 connector on PCB)		
Bode Mode	**Blink Sequence**	**Comment**

Error	********	ERROR
JTAG	*****ooo	JTAG
PJTAG0	****oooo	Boot Mode is set to PJTAG0
eMMC	***ooooo	Boot Mode is set to eMMC
SPI Boot	**oooooo	Boot Mode is set to QSPI
SD Boot	*ooooooo	Boot Mode is set to SD
	ON	Reset is on

XMOD LED Red (XMOD1 on J12 with green dot)		
Status	**Blink Sequence**	**Comment**
PS_INIT_B	********	Indicates the PS is not initialized after a power-on reset (POR).
PS_ERROR_OUT	*****ooo	The PS_ERROR_OUT signal is asserted for accidental loss of power, an error, or an exception in the PMU.
DONE	ON or OFF	Indicates the PL configuration is completed (LED is OFF).

LED_P/N (BLUE Power LED on enclosure)		
Status/ User	**Blink Sequence**	**Comment**
Power	******** (slow blink)	Indicate board is powered off.
RGPIO controlled	User Defined	RGPIO 14 and 15, if RGPIO is active.
MIO40	User Defined	MIO40, if RGPIO is deactivated

HDLED_P/N (Red HD LED on enclosure)		
Status/ User	**Blink Sequence**	**Comment**
PS_INIT_B	********	Indicates the PS is initialized after a power-on reset (POR).
PS_ERROR_OUT	*****ooo	The PS_ERROR_OUT signal is asserted for accidental loss of power, an error, or an exception in the PMU.
ERR_STAT	****oooo	The PS_ERROR_STATUS indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.
RGPIO controlled	User Defined	RGPIO 16 and 17, if RGPIO is active
SC0	User Defined	SC0 (PL IO), if RGPIO is deactivated

Blink Frequency:

Blink Sequence	**Comment**
********	~5,8 Hz
*****ooo	~0,7 Hz, duty cycle 5/8

****oooo	~0,7 Hz, duty cycle 4/8
***ooooo	~0,7 Hz, duty cycle 3/8
**oooooo	~0,7 Hz, duty cycle 2/8
*ooooooo	~0,7 Hz, duty cycle 1/8

Appx. A: Change History

Revision Changes

CPLD REV05 to REV06

- LED Status changes of LED D2 D3 and HD_LED, XMOD LED
- extended Power Management

CPLD REV04 to REV05

- PS reboot via FSBL over MIO30 (need for proper PCI initialization on first power on without press Reset Button)
- SD Boot from micoSD only if switch S5-1/-2 is selected to ON
- RGPIO connection
- Add SD WP to FPGA
- Power, Rest Button debounced
- direct LED access via MIO and PL

Older Revision (PCB REV03) to CPLD REV04

- Bugfix: PCIe Reset Pin location.
- Bugfix: Swapping HDLED and PWRLED location.
- Bugfix: MEMS_CLKIN Pin location.
- Add XMOD 1 LED

Older Revision (PCB REV02) to CPLD REV04

- Add all functionality from older Revision (PCB REV03)

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV06	REV02, REV03, REV04	Error rendering macro 'page-info' Ambig	• typo correction

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

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2017-11-15	v.38	REV06	REV02, REV03, REV04	John Hartfiel	• Correctio n Boot Mode Section
2017-10-18	v.36	REV06	REV02, REV03, REV04	John Hartfiel	• Revision 06 finished
2017-06-20	v.29	REV05	REV02, REV03, REV04	John Hartfiel	• descriptio n and style bug-fix
2017-06-09	v.28	REV05	REV02, REV03, REV04	John Hartfiel	• Revision 05 finished
2017-06-08	v.23	REV05	REV02, REV03, REV04	John Hartfiel	• Documen t style update
2017-05-08	v.22	REV05	REV02, REV03, REV04	John Hartfiel	• Revision 05 working in process
2017-02-08	v.19	REV04	REV02, REV03, REV04	John Hartfiel	• Revision 04 finished
2016-04-11	v.1	---			• Initial release

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