TE0820 Test Board

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Overview

ZynqMP PS Design with Linux Example and simple frequency counter to measure SI5338 Reference CLK with Vivado HW Manager

Wiki Resources page

Key Features

- Vitis/Vivado 2023.2
- PetaLinux
- SD
- ETH
- USB
- I2C
- RTC
- FMeter
- MAC from EEPROM
- User LED (PCB REV03 only)
- Modified FSBL for SI5338 programming

Revision History

Date	Vivado	Project Built	Authors	Description
2024-03-05	2023.2	TE0820-test_board-vivado_2023.2-build_4_20240305102020.zip TE0820-test_board_noprebuilt-vivado_2023.2-build_4_20240305102020.zip	Manuela Strücker	• bugfix file_location.txt • update USB available in uboot
2024-02-23	2023.2	TE0820-test_board-vivado_2023.2-build_4_20240222140518.zip TE0820-test_board_noprebuilt-vivado_2023.2-build_4_20240222140518.zip	Manuela Strücker	• 2023.2 release • new assembly variants
2023-06-22	2022.2	TE0820-test_board-vivado_2022.2-build_2_20230622121437.zip TE0820-test_board_noprebuilt-vivado_2022.2-build_2_20230622121437.zip	Manuela Strücker	• 2022.2 release • new assembly variants

2023-03-24	2021.2.1	TE0820-test_board-vivado_2021.2-build_20_20230324121549.zip TE0820-test_board_noprebuilt-vivado_2021.2-build_20_20230324121549.zip	Manuela Strücker	• new assembly variants
2022-09-28	2021.2.1	TE0820-test_board-vivado_2021.2-build_17_20220928065907.zip TE0820-test_board_noprebuilt-vivado_2021.2-build_17_20220928065907.zip	Manuela Strücker	• bugfix fsbl generation • new assembly variants
2022-09-12	2021.2.1	TE0820-test_board-vivado_2021.2-build_15_20220912132233.zip TE0820-test_board_noprebuilt-vivado_2021.2-build_15_20220912132233.zip	Manuela Strücker	• update board part files compatible to Vivado 2021.2.1 • new assembly variants
2022-01-28	2021.2	TE0820-test_board-vivado_2021.2-build_11_20220128090819.zip TE0820-test_board_noprebuilt-vivado_2021.2-build_11_20220128090819.zip	Manuela Strücker	• new assembly variants
2022-01-24	2021.2	TE0820-test_board-vivado_2021.2-build_10_20220124111148.zip TE0820-test_board_noprebuilt-vivado_2021.2-build_10_20220124111148.zip	John Hartfiel	• adding missing u-boot device tree to the boot.bin
2022-01-14	2021.2	TE0820-test_board-vivado_2021.2-build_8_20220114123035.zip TE0820-test_board_noprebuilt-vivado_2021.2-build_8_20220114123035.zip	John Hartfiel	• 2021.2 release • new assembly variants • remove alle PCB Revision 02 variant with 1GB DDR
2021-06-01	2020.2	TE0820-test_board-vivado_2020.2-build_5_20210601084124.zip TE0820-test_board_noprebuilt-vivado_2020.2-build_5_20210601092528.zip	John Hartfiel	• 2020.2 release • new assembly variants

2020-04-08	2019.2	TE0820-test_board_noprebuilt-vivado_2019.2-build_10_20200408073458.zip TE0820-test_board-vivado_2019.2-build_10_20200408073444.zip	John Hartfiel	• script update • new assembly variants
2020-03-25	2019.2	TE0820-test_board_noprebuilt-vivado_2019.2-build_8_20200325083817.zip TE0820-test_board-vivado_2019.2-build_8_20200325083750.zip	John Hartfiel	• script update • Board Part update (minor changes)
2020-01-22	2019.2	TE0820-test_board_noprebuilt-vivado_2019.2-build_3_20200122154341.zip TE0820-test_board-vivado_2019.2-build_3_20200122154318.zip	John Hartfiel	• script update for linux user
2020-01-14	2019.2	TE0820-test_board-vivado_2019.2-build_3_20200114081551.zip TE0820-test_board_noprebuilt-vivado_2019.2-build_3_20200114081612.zip	John Hartfiel	• add fsbl_flash binary • Vitis script updates (include linux domain and prebuilt linux files for vitis) • prebuilt binary export on selection guide
2019-12-19	2019.2	TE0820-test_board-vivado_2019.2-build_1_20191219075647.zip TE0820-test_board_noprebuilt-vivado_2019.2-build_1_20191219080228.zip	John Hartfiel	• 2019.2 update • Vitis support
2019-10-29	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_09_20191029071045.zip TE0820-test_board-vivado_2018.3-build_09_20191029071028.zip	John Hartfiel	• new assembly variants
2019-08-09	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_07_20190809084040.zip TE0820-test_board-vivado_2018.3-build_07_20190809083901.zip	John Hartfiel	• bugfix fsbl (removed second PSU init)

2019-06-19	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_06_20190619073300.zip TE0820-test_board-vivado_2018.3-build_06_20190619073243.zip	John Hartfiel	• new assembly variants • USB2 only (change PS IP and device tree) • FSBL changes
2019-04-01	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_03_20190401130135.zip TE0820-test_board-vivado_2018.3-build_03_20190401130123.zip	John Hartfiel	• renamed ...D variants to ...A
2019-02-21	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_01_20190221103025.zip TE0820-test_board-vivado_2018.3-build_01_20190221102913.zip	John Hartfiel	• TE Script update • rework of the FSBLs • SI5338 CLKBuilder Pro Project • some additional Linux features • MAC from EEPROM • new assembly variants • remove special compiler flags, which was needed in 2018.2
2018-10-31	2018.2	TE0820-test_board_noprebuilt-vivado_2018.2-build_03_20181031164506.zip TE0820-test_board-vivado_2018.2-build_03_20181031164452.zip	John Hartfiel	• new assembly variants • update optional petalinux startup init script

2018-09-12	2018.2	TE0820-test_board_noprebuilt-vivado_2018.2-build_03_20180912094615.zip
		TE0820-test_board-vivado_2018.2-build_03_20180912094558.zip
			John Hartfiel	• correction:
				  ○ TE0820-03-4EV-1EA has 2GB DDR, now 2GB instead of 1GB is initialised
				  ○ small changes on DDR setup of TE0820-02-2EG-1EE

2018-08-15	2018.2	TE0820-test_board-vivado_2018.2-build_01_20180706212937.zip TE0820-test_board_noprebuilt-vivado_2018.2-build_01_20180706212952.zip	John Hartfiel	• different design for REV03 • small petalinux changes • IO renaming • additional notes for FSBL generated with Win SDK • changed *.bif
2018-06-19	2017.4	TE0820-test_board-vivado_2017.4-build_10_20180619160713.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_10_20180619160728.zip	John Hartfiel	• bugfix board part files BANK1 MIO voltages • Add "dummy" PS USB3 parameter so solve problems with some USB2 devices
2018-05-24	2017.4	TE0820-test_board-vivado_2017.4-build_10_20180524151356.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_10_20180524151342.zip	John Hartfiel	• solved Linux Flash issue • new assembly variant
2018-04-25	2017.4	TE0820-test_board-vivado_2017.4-build_07_20180425134435.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_07_20180425134459.zip	John Hartfiel	• new assembly variants
2018-02-06	2017.4	TE0820-test_board-vivado_2017.4-build_06_20180206203359.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_06_20180206203414.zip	John Hartfiel	• solved JTAG /Linux issue
2018-02-01	2017.4	TE0820-test_board-vivado_2017.4-build_05_20180201084319.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_05_20180201094724.zip	John Hartfiel	• board part csv update

2018-01-24	2017.4	TE0820-test_board-vivado_2017.4-build_05_20180124085247.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_05_20180124085303.zip	John Hartfiel	• rework board part files • solved USB, QSPI and PHY issue
2017-11-21	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171121160552.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171121160606.zip	John Hartfiel	• solved SD SDX Cards Problem • Separate csv name for all assembly variants
2017-11-20	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171120162931.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171120162851.zip	John Hartfiel	• solved SD WP Problem
2017-10-19	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171019104824.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171019104837.zip	John Hartfiel	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Uboot: Ethernet not present	Ethernet in Uboot cannot be used due to no MAC address set (Error: ethernet@ff0e0000 address not set.)	please set CONFIG_NET_RANDOM_ETHADDR in petalinux-config -c u-boot as a side effect, MAC address will be random in Linux also	2023.2 version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated between 2021.2 and 2021.2.1 patch, see Xilinx Forum Request	use corresponding board files for the Vivado versions	--
Uboot did not start	Effected Design: TE0820-test_board-vivado_2020.2-build_5_20210601084124.zip TE0820-test_board_noprebuilt-vivado_2020.2-build_5_20210601092528.zip	Use older version, this will be fixed as soon as possible	**Solved** with 20220124 update

Flash access on Linux	Device tree is not correct on Linux	add compatibility to "comp atible “jedec,spi-nor”"	**Solved** with 20180524 update
USB UART Terminal is blocked / SDK Debugging is blocked	This happens only with 2017.4 Linux , when JTAG connection is established on Vivado HW Manager.	Do not use HW Manager connection, or if debugging is necessary: 1. Boot linux with usb terminal 2. From the terminal: root root mount ifconfig eth0 3. Open two new SSH terminals via ethernet: root root , run user application ... 4. Exit and close the usb terminal	**Solved** with 20180206 update

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2023.2	needed, Vivado is included into Vitis installation
PetaLinux	2023.2	needed
SI ClockBuilder Pro	---	optional

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
~~TE0820-ES1~~	~~es1~~	~~REV01~~	~~1GB~~	~~64MB~~	~~4GB~~	~~NA~~	~~Not longer supported by vivado~~
~~TE0820-02-02CG-1E~~	~~2cg_1e_1gb~~	~~REV02~~	~~1GB~~	~~64MB~~	~~4GB~~	~~NA~~	~~Not longer supported use 2020.2 or older~~
~~TE0820-02-02CG-1EA~~	~~2cg_1e_1gb~~	~~REV02~~	~~1GB~~	~~128MB~~	~~4GB~~	~~NA~~	~~Not longer supported use 2020.2 or older~~
~~TE0820-02-02EG-1E~~	~~2eg_1e_1gb~~	~~REV02~~	~~1GB~~	~~64MB~~	~~4GB~~	~~NA~~	~~Not longer supported use 2020.2 or older~~

~~TE0820-02-02EG-1E3~~	~~2eg_1e_1gb~~	~~REV02~~	~~1GB~~	~~64MB~~	~~4GB~~	~~2.5 mm connectors~~	~~Not longer supported use 2020.2 or older~~
~~TE0820-02-02EG-1EA~~	~~2eg_1e_1gb~~	~~REV02~~	~~1GB~~	~~128MB~~	~~4GB~~	~~NA~~	~~Not longer supported use 2020.2 or older~~
~~TE0820-02-02EG-1EL~~	~~2eg_1e_1gb~~	~~REV02~~	~~1GB~~	~~128MB~~	~~4GB~~	~~2.5 mm connectors~~	~~Not longer supported use 2020.2 or older~~
~~TE0820-02-03CG-1E~~	~~3eg_1e_1gb~~	~~REV02~~	~~1GB~~	~~64MB~~	~~4GB~~	~~NA~~	~~Not longer supported use 2020.2 or older~~
~~TE0820-02-03CG-1EA~~	~~3eg_1e_1gb~~	~~REV02~~	~~1GB~~	~~128MB~~	~~4GB~~	~~NA~~	~~Not longer supported use 2020.2 or older~~
~~TE0820-02-03EG-1E~~	~~3eg_1e_1gb~~	~~REV02~~	~~1GB~~	~~64MB~~	~~4GB~~	~~NA~~	~~Not longer supported use 2020.2 or older~~
~~TE0820-02-03EG-1E3~~	~~3eg_1e_1gb~~	~~REV02~~	~~1GB~~	~~64MB~~	~~4GB~~	~~2.5 mm connectors~~	~~Not longer supported use 2020.2 or older~~
~~TE0820-02-03EG-1EA~~	~~3eg_1e_1gb~~	~~REV02~~	~~1GB~~	~~128MB~~	~~4GB~~	~~NA~~	~~Not longer supported use 2020.2 or older~~
~~TE0820-02-03EG-1EL~~	~~3eg_1e_1gb~~	~~REV02~~	~~1GB~~	~~128MB~~	~~4GB~~	~~2.5 mm connectors~~	~~Not longer supported use 2020.2 or older~~
~~TE0820-02-04CG-1EA~~	~~4eg_1e_1gb~~	~~REV02~~	~~1GB~~	~~128MB~~	~~4GB~~	~~NA~~	~~Not longer supported use 2020.2 or older~~
TE0820-03-02CG-1EA	2cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02CG-1ED	2cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-02EG-1EA	2eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02EG-1EL	2eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-03CG-1EA	3cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-03EG-1EA	3eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-03EG-1EL	3eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-04CG-1EA	4cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-04EV-1EA	4ev_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-2AE21FA	2cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2AI21FA	2cg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BE21FA	2eg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BE21FL*	2eg_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA

TE0820-03-2BI21FA	2eg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BI21FL	2eg_1i_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-3AE21FA	3cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3AI210A	3cg_1i_2gb	REV03	2GB	128MB	0GB	NA	NA
TE0820-03-3AI21FA	3cg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3BE21FA	3eg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3BE21FL	3eg_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-4AE21FA	4cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4AI21FI	4cg_1i_x_2gb	REV03	2GB	128MB	8GB	without ETH PHY	NA
TE0820-03-4DE21FA	4ev_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4DE21FC	4ev_1e_2gb	REV03	2GB	128MB	8GB	without encryption NCNR	NA
TE0820-03-4DE21FL	4ev_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-4DI21FA	4ev_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-5DI21FA	5ev_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-5DR21FA	5ev_1q_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-04-2AE21FA	2cg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2AI21FA	2cg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2AI21MC	2cg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BE21-V1	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	Customised
TE0820-04-2BE21FA	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BE21FAJ	2eg_1e_2gb	REV04	2GB	128MB	8GB	without spacers	NA
TE0820-04-2BE21FL	2eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-04-2BE21MA	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BE21MAJ	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BI21FA	2eg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BI21FL	2eg_1i_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-04-2BI21MA	2eg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BI21ML	2eg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3AE21FA	3cg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3AE21MA	3cg_1e_2gb	REV04	2GB	128MB	8GB	NA	Other EMMC mfr

TE0820-04-3AI21FA	3cg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3AI21FAT	3cg_1i_2gb	REV04	2GB	128MB	8GB	NA	Customer supplied
TE0820-04-3BE21FA	3eg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3BE21FL	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-04-3BE21KA	3eg_1e_2gb	REV04	2GB	128MB	64GB	NA	NA
TE0820-04-3BE21MA	3eg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3BE21ML	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	Other EMMC mfr
TE0820-04-3BE21MLZ	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	Other EMMC mfr
TE0820-04-4AE21FA	4cg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-4AE21MA	4cg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-4AI21FI	4cg_1i_x_2gb	REV04	2GB	128MB	8GB	without ETH PHY	NA
TE0820-04-4BI21KL	4eg_1i_2gb	REV04	2GB	128MB	64GB	2.5 mm connectors	NA
TE0820-04-4DE21FA	4ev_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-4DE21FL	4ev_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-04-4DE21MA	4ev_1e_2gb	REV04	2GB	128MB	8GB	NA	Other EMMC mfr
TE0820-04-4DI21FA	4ev_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-4DI21MA	4ev_1i_2gb	REV04	2GB	128MB	8GB	NA	Other EMMC mfr
TE0820-04-5DI21FA	5ev_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-5DI21MA	5ev_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-5DR21FA	5ev_1q_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-S002	3eg_1e_2gb	REV04	2GB	128MB	8GB	NA	Other EMMC mfr|Custom supplied TE0820-04-3BE21MA
TE0820-04-S002C1	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	CAO
TE0820-04-S003	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	Other EMMC mfr
TE0820-04-S004	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	CAO
TE0820-04-S005	4cg_1e_2gb	REV04	2GB	128MB	8GB	NA	Other EMMC mfr|Custom supplied TE0820-04-4AE21MA
TE0820-04-S006	4ev_1e_2gb	REV04	2GB	128MB	8GB	NA	CAO:Other EMMC mfr
TE0820-04-S009	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	Other EMMC mfr
TE0820-04-S010	4ev_1e_2gb	REV04	2GB	128MB	8GB	NA	CAO:Other EMMC mfr

TE0820-04-S013	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	CAO:Other EMMC mfr
TE0820-04-S016	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	CAO:Other EMMC mfr
TE0820-04-S018	4cg_1e_2gb	REV04	2GB	128MB	8GB	NA	CAO
TE0820-05-2AE21MA	2cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2AE21MAZ	2cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2AE81MA	2cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2AI21MA	2cg_1i_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2AI81MA	2cg_1i_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2BE21MA	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2BE21MAJ	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2BI21MA	2eg_1i_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2BI81ML	2eg_1i_2gb	REV05	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-05-3AE21MA	3cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-3AE81MA	3cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-3BE21MA	3eg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-3BE21MAZ	3eg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-3BE81MA	3eg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-3BE81ML	3eg_1e_2gb	REV05	2GB	128MB	8GB	2.5 mm connectors	Other EMMC mfr
TE0820-05-3BI21ML	3eg_1i_2gb	REV05	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-05-4AE21MA	4cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-4AE81MA	4cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-4AI21MI	4cg_1i_x_2gb	REV05	2GB	128MB	8GB	without ETH PHY	NA
TE0820-05-4BI21PL	4eg_1i_2gb	REV05	2GB	128MB	64GB	2.5 mm connectors	NA
TE0820-05-4BI21PLZ	4eg_1i_2gb	REV05	2GB	128MB	64GB	2.5 mm connectors	NA
TE0820-05-4DE21MA	4ev_1e_2gb	REV05	2GB	128MB	8GB	NA	Other EMMC mfr
TE0820-05-4DI21MA	4ev_1i_2gb	REV05	2GB	128MB	8GB	NA	Other EMMC mfr
TE0820-05-4DI81MA	4ev_1i_2gb	REV05	2GB	128MB	8GB	NA	Other EMMC mfr
TE0820-05-5DI21MA	5ev_1i_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-5DI81MA	5ev_1i_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-S002C1	4cg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO

TE0820-05-S003	4ev_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S004C1	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S005	3eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S008C1	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO:without PLL
TE0820-05-S013	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO:without PLL
TE0820-05-S014C1	4cg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S016	3eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S017C1	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO:without PLL
TE0820-05-S018	3cg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S020	3eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S022	3cg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S024C1	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TE0701	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers
TE0703*	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 cm carriers • Used as reference carrier.
TE0705	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers
TE0706	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers
TEB0707	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers

TEBA0841	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers • No SD Slot available, pins goes to Pin Header • For TEBA0841 REV01, please contact TE support
TEF1002	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI
Cooler	It's recommended to use cooler on ZynqMP device

Additional Hardware

Content

For general structure and of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Design sources

Additional Sources

Type	Location	Notes

SI5338	<project folder>\misc\Si5338	SI5338 Project with current PLL Configuration
init.sh	<project folder>\misc\sd\	Additional Initialization Script for Linux

Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Script-File	*.scr	Distro Boot Script file
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebuilt content)

Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0820 "Test Board" Reference Design

Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

> ⚠ **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
------------------------Set design paths----------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
--------------------------------------------------------------------
-------------------------TE Reference
Design---------------------------
--------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
    - optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

    > ⚠ Note: Select correct one, see also Vivado Board Part Flow

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

```
TE::hw_build_design -export_prebuilt
```

> Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see PetaLinux KICKstart
   - use TE Template from "<project folder>\os\petalinux"
   - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>" . **Note:** HW Export from Vivado GUI creates another path as default workspace.
6. Configure the **boot.scr** file as needed, see Distro Boot with Boot.scr
7. Generate Programming Files with Vitis
   a. Copy PetaLinux build image files to prebuilt folder
      i. copy **u-boot.elf, system.dtb, bl31.elf**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

      > "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

   b. Generate Programming Files

      run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

      ```
      TE::sw_run_vitis -all
      TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE Scripts on Vivado TCL)
      ```

      > TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

8. Generate Programming Files with Petalinux (alternative), see PetaLinux KICKstart

Launch

Programming

> Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging

Note: Depending on CPLD Firmware and Boot Mode settings, QSPI boot with Linux image on SD or complete SD Boot is possible.

Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection

c. Select create and open delivery binary folder

> Note: Folder "<project folder>/_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash and **image.ub,** and **boot.scr** on **SD** or **USB**.

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)
`TE::pr_program_flash -swapp u-boot` `TE::pr_program_flash -swapp hello_te0820 (optional)`

> To program with Vitis/Vivado GUI, use special FSBL (fsbl_flash) on setup

3. Copy **image.ub,** and **boot.scr** on **SD** or **USB**
   - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder,see: Get prebuilt boot binaries
   - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
4. Set Boot Mode to **QSPI-Boot** and insert **SD** or **USB**.
   - Depends on Carrier, see carrier TRM.

SD-Boot mode

1. Copy **image.ub, boot.src** and **Boot.bin** on **SD**
   - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder, see: Get prebuilt boot binaries
   - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
2. Set Boot Mode to SD-Boot.
   - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

JTAG

Not used on this example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)

> Note: See TRM of the Carrier, which is used.

> Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.
> The boot options described above describe the common boot processes for this hardware; other boot options are possible.
> For more information see Distro Boot with Boot.scr

4. Power On PCB

   1. ZynqMP Boot ROM loads FSBL from SD/QSPI into OCM,

   2. FSBL init the PS, programs the PL using the bitstream and loads PMU, ATF and U-boot from SD/QSPI into DDR,

   3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

Linux

1. Open Serial Console (e.g. putty)
   - Speed: 115200
   - select COM Port

   > Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

2. Linux Console:

   > Note: Wait until Linux boot finished

3. You can use Linux shell now.

```
i2cdetect -y -r 0        (check I2C 0 Bus)
dmesg | grep rtc        (RTC check)
udhcpc                                (ETH0 check)
lsusb                                (USB check)
```

4. Option Features

   - Webserver to get access to Zynq
     - insert IP on web browser to start web interface
   - init.sh scripts
     - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD")

Vivado HW Manager

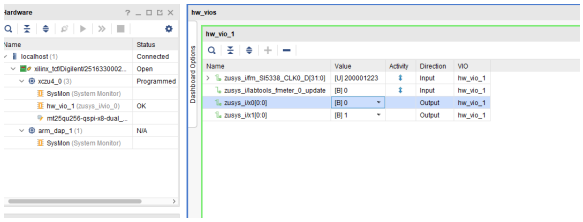
Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)

- Control:
  - User LED (PCB REV03 and newer)
- Monitoring:
  - SI5338_CLK0 Counter:

- Set radix from VIO signals to unsigned integer.
  Note: Frequency Counter is inaccurate and displayed unit is Hz
- SI5338 CLK is configured to 200MHz by default.

PCB REV03 Design:

- User LED, see: TE0820 CPLD#LED

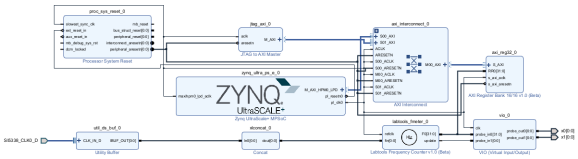


Vivado Hardware Manager

System Design - Vivado

Block Design

PCB REV03



Block Design PCB REV03

PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
I2C0	MIO
UART0	MIO
GPIO0	MIO
SWDT0..1	
TTC0..3	

GEM3	MIO
USB0	MIO, USB2 only

Constrains

Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design
```

Design specific constrain

_i_io.xdc

```
set_property PACKAGE_PIN K9 [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property IOSTANDARD LVDS [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property DIFF_TERM TRUE [get_ports {SI5338_CLK0_D_clk_p[0]}]

set_property PACKAGE_PIN H1 [get_ports {x0[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x0[0]}]
set_property PACKAGE_PIN J1 [get_ports {x1[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x1[0]}]
```

Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis

Application

Template location: "<project folder>\sw_lib\sw_apps\"

zynqmp_fsbl

TE modified 2023.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)
- General Changes:
    - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te_*
    - Si5338 Configuration
    - ETH+OTG Reset over MIO

zynqmp_pmufw

Xilinx default PMU firmware.

hello_te0820

Hello TE0820 is a Xilinx Hello World example as endless loop instead of one console output.

u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- select SD default instead of eMMC:
    - CONFIG_SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT=y
- add new flash partition for bootscr and sizing
    - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART0_SIZE=0xA00000
    - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART1_SIZE=0x2000000
    - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART2_SIZE=0x40000
    - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART3_NAME="bootscr"
    - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART3_SIZE=0x80000
- Identification
    - CONFIG_SUBSYSTEM_HOSTNAME="Trenz"
    - CONFIG_SUBSYSTEM_PRODUCT="TE0820"

U-Boot

Start with **petalinux-config -c u-boot**
Changes:

- MAC from eeprom together with uboot and device tree settings:
    - CONFIG_ENV_OVERWRITE=y
    - CONFIG_NVMEM=y
    - CONFIG_DM_RTC=y (needed for nvmem driver because of bug in uboot)
- Boot Modes:
    - CONFIG_QSPI_BOOT=y
    - CONFIG_SD_BOOT=y
    - CONFIG_ENV_IS_IN_FAT is not set
    - CONFIG_ENV_IS_IN_NAND is not set
    - CONFIG_ENV_IS_IN_SPI_FLASH is not set
    - CONFIG_BOOT_SCRIPT_OFFSET=0x2A40000
- Identification
    - CONFIG_IDENT_STRING=" TE0820"

Change platform-top.h:

```
#include <configs/xilinx_zynqmp.h> #no changes
```

Device Tree

project-spec\meta-user\recipes-bsp\device-tree\files\system-user.dtsi

```
/include/ "system-conf.dtsi"


/*-------------------- SD0 eMMC ----------------*/
&sdhci0 {
    // disable-wp;
    no-1-8-v;
};


/*-------------------- SD1 sd2.0 ----------------*/
&sdhci1 {
    disable-wp;
    no-1-8-v;
};


/*-------------------- USB 2.0 only ----------------*/
&usb0 {
    status = "okay";
    clock-names = "bus_clk";
    clocks = <&zynqmp_clk USB0_BUS_REF>;
    assigned-clocks = <&zynqmp_clk USB0_BUS_REF>;
};


&dwc3_0 {
    dr_mode = "host";
};


/*------------------ ETH PHY --------------------*/
&gem3 {
    //required otherwise petalinux gives a static address here
    /delete-property/ local-mac-address;
    phy-handle = <&phy0>;

    nvmem-cells = <&eth0_addr>;
    nvmem-cell-names = "mac-address";

    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};


/*------------------ QSPI -------------------- */
&qspi {
```

```
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;

        spi-rx-bus-width = <4>;
        spi-tx-bus-width = <4>;
        spi-max-frequency = <90000000>;
    };
};


/*------------------ I2C --------------------*/
&i2c0 {
    eeprom: eeprom@50 {
        compatible = "microchip,24aa025", "atmel,24c02";
        reg = <0x50>;

            #address-cells = <1>;
            #size-cells = <1>;
            eth0_addr: eth-mac-addr@FA {
              reg = <0xFA 0x06>;
            };
        };
};
```

Kernel

Start with **petalinux-config -c kernel**

Changes:

- Only needed to fix JTAG Debug issue:
    - CONFIG_CPU_FREQ is not set

Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- for web server app:
    - CONFIG_busybox-httpd=y
- For additional test tools only:
    - CONFIG_i2c-tools=y
    - CONFIG_packagegroup-petalinux-utils(util-linux,cpufrequtils,bridge-utils,mtd-utils, usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)
- For auto login:
    - CONFIG_imagefeature-serial-autologin-root=y

FSBL patch (alternative for vitis fsbl trenz patch)

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-bsp\embeddedsw"

Petalinux Troubleshoot#Petalinux2023.2

Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

startup

Script App to load init.sh from SD Card if available.

webfwu

Webserver application suitable for Zynq access. Need busybox-httpd

Additional Software

SI5338

File location "<project folder>\misc\Si5338\Si5338-*.slabtimeproj"

General documentation how you work with these project will be available on Si5338

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method	**Error rendering macro 'page-info'** Ambiguous method	**Error rendering macro 'page-info'** Ambiguous method	• bugfix file_location.txt • update USB available in uboot

overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.

overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.

overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.

atlassian . confluence.user. ConfluenceUser , class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject] [interface com. atlassian .user. User, class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject]	atlassian . confluence.user. ConfluenceUser , class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject] [interface com. atlassian .user. User, class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject]	atlassian . confluence.user. ConfluenceUser , class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject] [interface com. atlassian .user. User, class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject]	

2024-02-23	v.78	Manuela Strücker	• 2023.2 update • new assembly variants
2024-02-13	v.77	Markus Kirberg	• update Release notes and known issues
2023-06-22	v.76	Manuela Strücker	• 2022.2 update • new assembly variants
2023-03-28	v.75	Manuela Strücker	• new assembly variants
2022-09-28	v.74	Manuela Strücker	• bugfix fsbl generation • new assembly variants
2022-09-12	v.73	Manuela Strücker	• update board part files compatible to Vivado 2021.2.1 • new assembly variants
2022-09-06	v.72	Manuela Strücker	• new assembly variants
2022-01-26	v.70	John Hartfiel	• add missing uboot notes
2022-01-24	v.68	John Hartfiel	• Add new delivery design with uboot bugfix
2022-01-21	v.67	John Hartfiel	• Add Known issues
2022-01-14	v.66	John Hartfiel	• 2021.2 release
2021-06-09	v.65	Manuela Strücker	• document style update
2021-06-01	v.64	John Hartfiel	• 2020.2 update • new assembly variants • document style update
2020-05-07	v.62	John Hartfiel	• update programming section

2020-04-08	v.61	John Hartfiel	• script update • new assembly variants
2020-03-25	v.60	John Hartfiel	• script update
2020-01-21	v.59	John Hartfiel	• Script update for linux user
2020-01-14	v.58	John Hartfiel	• Script update, new features • doc update • add missing binary files
2019-12-19	v.57	John Hartfiel	• 2019.2 release
2019-10-29	v.56	John Hartfiel	• new assembly variants
2019-08-09	v.55	John Hartfiel	• bugfix fsbl
2019-06-19	v.54	John Hartfiel	• design changes • new variants
2019-04-01	v.53	John Hartfiel	• some notes • renamed ..D variants to ...A
2018-09-21	v.47	John Hartfiel	• 2018.3 release finished (include design reworks)
2018-10-31	v.43	John Hartfiel	• Update Design files for 2GB variants • rebuilt petalinux for optional init script
2018-09-12	v.41	John Hartfiel	• Update Design files for 2GB variants
2018-07-11	v.40	John Hartfiel	• add notes to ES1
2018-07-06	v.38	John Hartfiel	• 2018.2 release finished
2018-06-19	v.34	John Hartfiel	• Design Files Update
2018-02-13	v.29	John Hartfiel	

			• Design Files Update
2018-02-06	v.27	John Hartfiel	• Design Files Update
2018-01-29	v.26	John Hartfiel	• Update Known Issues
2018-01-24	v.25	John Hartfiel	• Release 2017.4
2018-01-10	v.24	John Hartfiel	• Update Known Issues
2017-12-20	v.23	John Hartfiel	• Typo correction • Update HW Module Table Description
2017-11-21	v.19	John Hartfiel	• Design Update
2017-11-20	v.18	John Hartfiel	• Design Update • Add Variants with 128MB Flash
2017-11-13	v.16	John Hartfiel	• Update Carrier sections
2017-11-06	v.15	John Hartfiel	• Typo corrected
2017-10-23	v.13	John Hartfiel	• Update Key Features section • Style Update Additional Software section
2017-10-19	v.9	John Hartfiel	• Release 2017.2
2017-09-11	v.1	**Error rendering macro 'page-info'** Ambiguous	Initial release

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Document change history.

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Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

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ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.
ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class
com.atlassian.confluence.core.ContentEntityObject]