

TE0808 TRM

[Download PDF version of this document.](#)

Table of Contents

- [Overview](#)
 - [Key Features](#)
 - [Block Diagram](#)
 - [Main Components](#)
 - [Initial Delivery State](#)
- [Signals, Interfaces and Pins](#)
 - [Board to Board \(B2B\) connectors](#)
 - [MGT Lanes](#)
 - [JTAG Interface](#)
 - [Configuration Bank Control Signals](#)
 - [Analog Input](#)
 - [Quad SPI Interface](#)
- [Boot Process](#)
- [On-board Peripherals](#)
 - [Flash](#)
 - [DDR4 SDRAM](#)
 - [Programmable PLL Clock Generator](#)
 - [Oscillators](#)
 - [On-board LEDs](#)
- [Power and Power-On Sequence](#)
 - [Power Consumption](#)
 - [Power Distribution Dependencies](#)
 - [Power-On Sequence Diagram](#)
 - [Operation Conditions of the DC-DC Converter Control Signals](#)
 - [Voltage Monitor Circuit](#)
 - [Power Rails](#)
 - [Bank Voltages](#)
- [B2B connectors](#)
 - [Features](#)
 - [Connector Stacking height](#)
 - [Current Rating](#)
 - [Connector Speed Ratings](#)
 - [Manufacturer Documentation](#)
- [Variants Currently In Production](#)
- [Technical Specifications](#)
 - [Absolute Maximum Ratings](#)
 - [Recommended Operating Conditions](#)
 - [Operating Temperature Ranges](#)
 - [Physical Dimensions](#)
- [Revision History](#)
 - [Hardware Revision History](#)
 - [Document Change History](#)
- [Disclaimer](#)
 - [Data Privacy](#)
 - [Document Warranty](#)
 - [Limitation of Liability](#)
 - [Copyright Notice](#)
 - [Technology Licenses](#)
 - [Environmental Protection](#)
 - [REACH, RoHS and WEEE](#)

Overview

The Trencz Electronic TE0808 is an industrial-grade MPSoC SoM integrating a Xilinx Zynq UltraScale+ MPSoC, up to 8 GBytes of DDR4 SDRAM via 64-bit wide data bus, max. 512 MByte Flash memory for configuration and operation, 20 Gigabit transceivers and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os are provided via rugged high-speed stacking connections. All this in a compact 5.2 x 7.6 cm form factor, at the competitive price.

Key Features

- MPSoC: ZYNQ UltraScale+ ZU9EG 900 pin package
- Memory
 - 64-Bit DDR4, 8 GByte maximum
 - Dual SPI boot Flash in parallel, 512 MByte maximum
- User I/Os
 - 65 x PS MIOs, 48 x PL HD GPIOs, 156 x PL HP GPIOs (3 banks)
 - Serial transceivers: 4 x GTR + 16 x GTH
 - Transceiver clocks inputs and outputs
 - PLL clock generator inputs and outputs
- Si5345 - 10 output PLL
- All power supplies on board, single 3.3V power source required
 - 14 on-board DC-DC regulators and 13 LDOs
 - LP, FP, PL separately controlled power domains
- Support for all boot modes (except NAND) and scenarios
- Support for any combination of PS connected peripherals
- Size: 52 x 76 mm, 3 mm mounting holes for skyline heat spreader
- B2B connectors: 4 x 160 pin

Block Diagram

TE0808-04

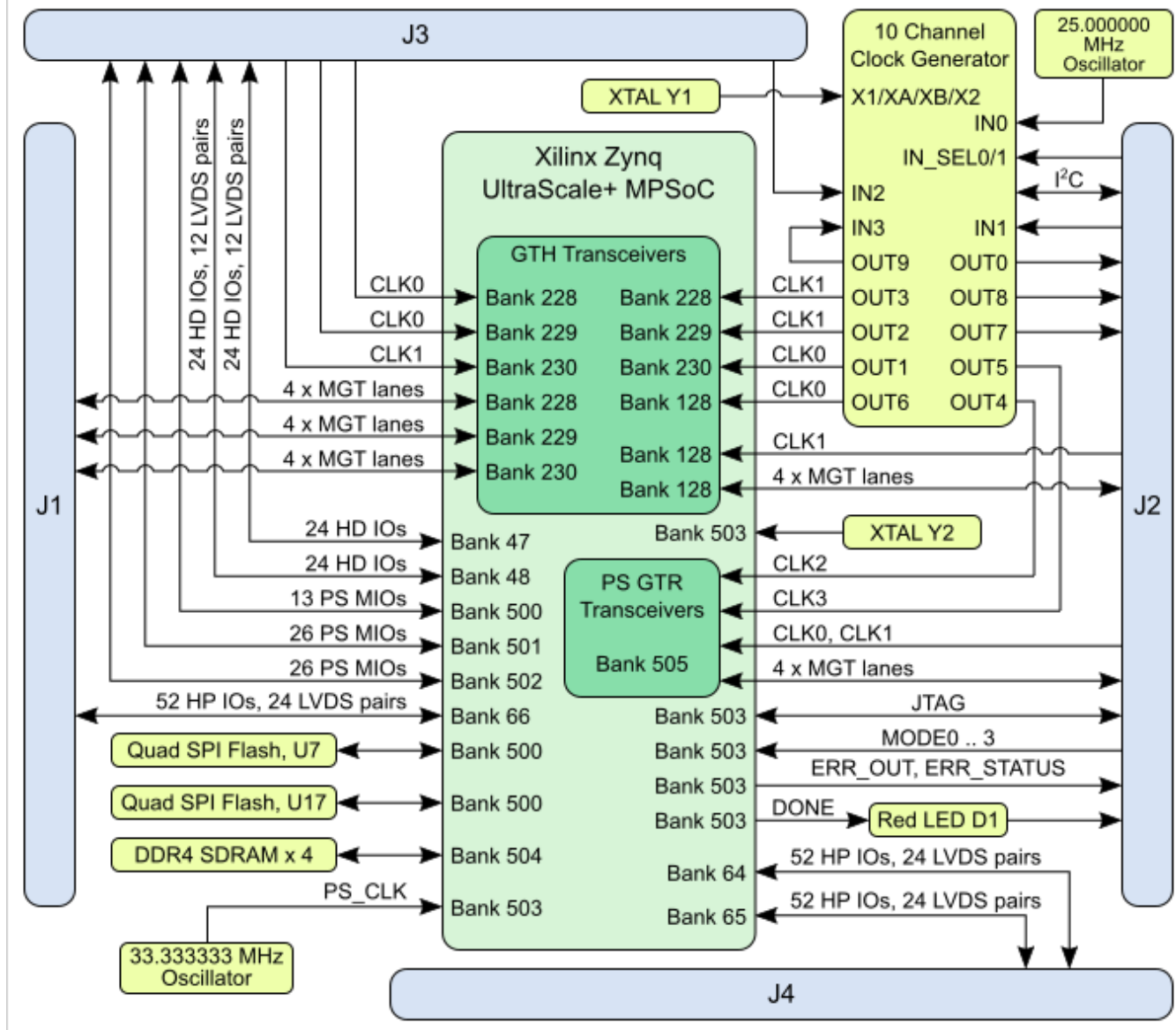


Figure 1: TE0808-04 Block Diagram.

Main Components

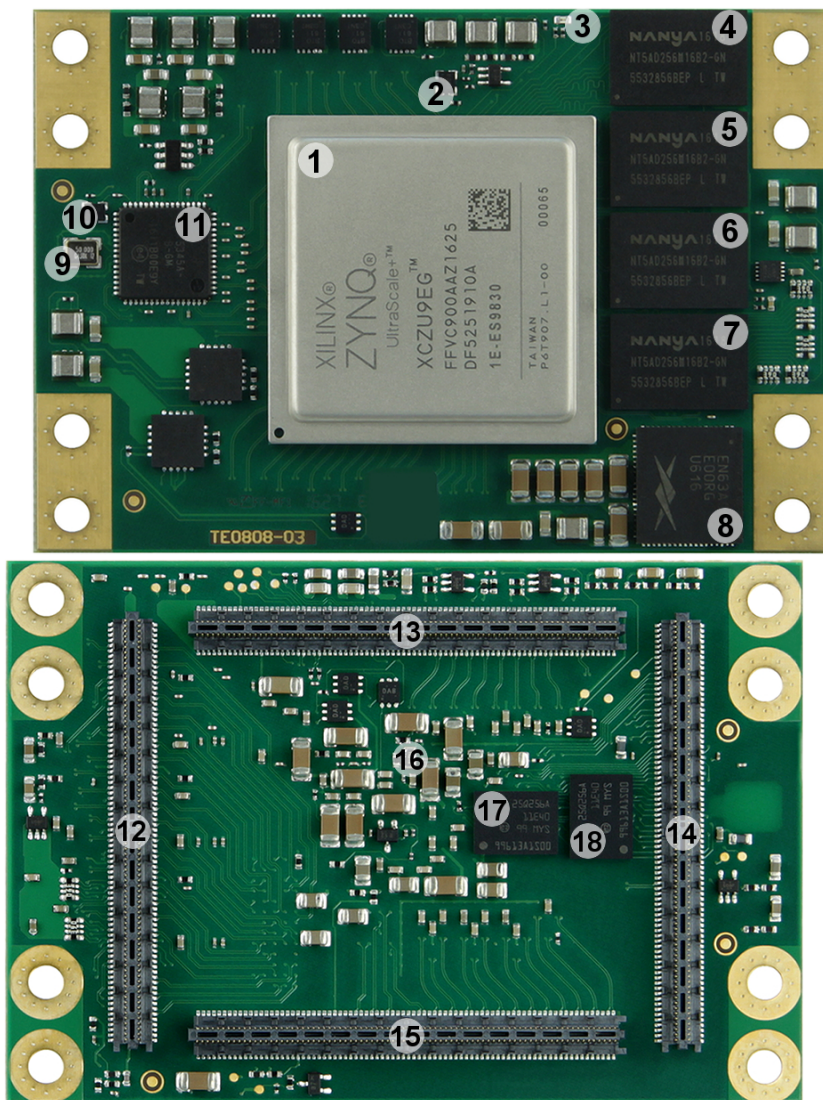


Figure 2: TE0808 MPSoC module.

1. Xilinx ZYNQ UltraScale+ XCZU9EG MPSoC, U1
2. Low-power programmable oscillator @ 33.333333 MHz (PS_CLK), U32
3. Red LED (DONE), D1
4. 256Mx16 DDR4-2400 SDRAM, U12
5. 256Mx16 DDR4-2400 SDRAM, U9
6. 256Mx16 DDR4-2400 SDRAM, U2
7. 256Mx16 DDR4-2400 SDRAM, U3
8. 12A PowerSoC DC-DC converter, U4
9. Quartz crystal, Y1
10. Low-power programmable oscillator @ 25.000000 MHz (IN0 for U5), U25
11. 10-channel programmable PLL clock generator, U5
12. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J4
13. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J2
14. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J3
15. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J1
16. Quartz crystal, Y2
17. 256 Mbit serial NOR Flash memory, U7

18. 256 Mbit serial NOR Flash memory, U17

Initial Delivery State

| Storage device name | Content | Notes |
|----------------------------------|----------------|-------|
| SPI Flash main array | Not programmed | - |
| eFUSE Security | Not programmed | - |
| Si5345A programmable PLL NVM OTP | Not programmed | - |

Table 1: Initial Delivery State of the flash memories.

Signals, Interfaces and Pins

Board to Board (B2B) connectors

The TE0808 MPSoC SoM has four Board to Board (B2B) connectors with 160 contacts per connector.

Each connector has a specific arrangement of the signal pins, which are grouped together in categories related to their functionalities and to their belonging to particular units of the Zynq UltraScale+ MPSoC like I/O banks, interfaces and Gigabit transceivers or to the on-board peripherals.

Following table lists the I/O-bank signals, which are routed from the MPSoC's PL and PS banks as LVDS pairs or single ended I/O's to the B2B connectors.

| Bank | Type | B2B Connector | Schematic Names / Connector Pins | I/O Signals | LVDS Pairs | VCCO Bank Voltage | Notes |
|------|------|---------------|---|-------------|------------|------------------------------|---|
| 47 | HD | J3 | B47_L1_P ... B47_L12_P B47_L1_N ... B47_L12_N | 24 I/Os | 12 | VCCO47 pins J3-43, J3-44 | VCCO max. 3.3V usable as single-ended I/Os |
| 48 | HD | J3 | B48_L1_P ... B48_L12_P B48_L1_N ... B48_L12_N | 24 I/Os | 12 | VCCO48 pins J3-15, J3-16 | VCCO max. 3.3V usable as single-ended I/Os |
| 64 | HP | J4 | B64_L1_P ... B64_L24_P B64_L1_N ... B64_L24_N B_64_T0 ... B_64_T3 | 52 I/O's | 24 | VCCO64 pins J4-58, J4-106 | VCCO max. 1.8V usable as single-ended I/Os |
| 65 | HP | J4 | B65_L1_P ... B65_L24_P B65_L1_N ... B65_L24_N B_65_T0 ... B_65_T3 | 52 I/Os | 24 | VCCO65 pins J4-69, J4-105 | VCCO max. 1.8V usable as single-ended I/Os |
| 66 | HP | J1 | B66_L1_P ... B66_L24_P B66_L1_N ... B66_L24_N B_66_T0 ... B_66_T3 | 48 I/Os | 24 | VCCO66 pins J1-90, J1-120 | VCCO max. 1.8V usable as single-ended I/Os |
| 500 | MIO | J3 | MIO13 ... MIO25 | 13 I/Os | - | PS_1V8 | User configurable I/Os on B2B |
| 501 | MIO | J3 | MIO26 ... MIO51 | 26 I/Os | - | PS_1V8 | User configurable I/Os on B2B |
| 502 | MIO | J3 | MIO52 ... MIO77 | 26 I/Os | - | PS_1V8 | User configurable I/Os on B2B |

Table 2: B2B connector pin-outs of available PL and PS banks of the TE0808-04 SoM.

All MIO banks are powered from on-module DC-DC power rail. All PL I/O Banks have separate VCCO pins in the B2B connectors, valid VCCO should be supplied from the baseboard.

For detailed information about the B2B pin-out, please refer to the [Pin-out](#) table.

The configuration of the I/O's MIO13 - MIO77 are depending on the base-board peripherals connected to these pins.

MGT Lanes

The B2B connector J1 and J2 provide also access to the MGT banks of the Zynq UltraScale+ MPSoC. There are 20 high-speed data lanes (Xilinx GTH / GTR transceiver) available composed as differential signaling pairs for both directions (RX/TX).

The MGT banks have also clock input-pins which are exposed to the B2B connectors J2 and J3. Following MGT lanes are available on the B2B connectors:

| Bank | Type | B2B Connector | Count of MGT Lanes | Schematic Names / Connector Pins | MGT Bank's Reference Clock Inputs |
|------|------|---------------|------------------------------|--|---|
| 228 | GTH | J1 | 4 GTH lanes (4 RX / 4 TX) | B228_RX3_P, B228_RX3_N, pins J1-51, J1-53 B228_TX3_P, B228_TX3_N, pins J1-50, J1-52 B228_RX2_P, B228_RX2_N, pins J1-57, J1-59 B228_TX2_P, B228_TX2_N, pins J1-56, J1-58 B228_RX1_P, B228_RX1_N, pins J1-63, J1-65 B228_TX1_P, B228_TX1_N, pins J1-62, J1-63 B228_RX0_P, B228_RX0_N, pins J1-69, J1-71 B228_TX0_P, B228_TX0_N, pins J1-68, J1-70 | 1 reference clock signal (B228_CLK0) from B2B connector J3 (pins J3-60, J3-62) to bank's pins R8/R7 1 reference clock signal (B228_CLK1) from programmable PLL clock generator U5 to bank's pins N8/N7 |
| 229 | GTH | J1 | 4 GTH lanes (4 RX / 4 TX) | B229_RX3_P, B229_RX3_N, pins J1-27, J1-29 B229_TX3_P, B229_TX3_N, pins J1-26, J1-28 B229_RX2_P, B229_RX2_N, pins J1-33, J1-35 B229_TX2_P, B229_TX2_N, pins J1-32, J1-34 B229_RX1_P, B229_RX1_N, pins J1-39, J1-41 B229_TX1_P, B229_TX1_N, pins J1-38, J1-40 B229_RX0_P, B229_RX0_N, pins J1-45, J1-47 B229_TX0_P, B229_TX0_N, pins J1-44, J1-46 | 1 reference clock signal (B229_CLK0) from B2B connector J3 (pins J3-65, J3-67) to bank's pins L8/L7 1 reference clock signal (B229_CLK1) from programmable PLL clock generator U5 to bank's pins J8/J7 |
| 230 | GTH | J1 | 4 GTH lanes (4 RX / 4 TX) | B230_RX3_P, B230_RX3_N, pins J1-3, J1-5 B230_TX3_P, B230_TX3_N, pins J1-2, J1-4 B230_RX2_P, B230_RX2_N, pins J1-9, J1-11 B230_TX2_P, B230_TX2_N, pins J1-8, J1-10 B230_RX1_P, B230_RX1_N, pins J1-15, J1-17 B230_TX1_P, B230_TX1_N, pins J1-14, J1-16 B230_RX0_P, B230_RX0_N, pins J1-21, J1-23 B230_TX0_P, B230_TX0_N, pins J1-20, J1-22 | 1 reference clock signal (B230_CLK1) from B2B connector J3 (pins J3-59, J3-61) to bank's pins E8/E7 1 reference clock signal (B230_CLK0) from programmable PLL clock generator U5 to bank's pins G8/G7 |

| | | | | | |
|-----|-----|----|------------------------------|--|--|
| 128 | GTH | J2 | 4 GTH lanes (4 RX / 4 TX) | B128_RX3_N, B128_RX3_P, pins J2-28, J2-30 B128_TX3_N, B128_TX3_P, pins J2-25, J2-27 B128_RX2_N, B128_RX2_P, pins J2-34, J2-36 B128_TX2_N, B128_TX2_P, pins J2-31, J2-33 B128_RX1_N, B128_RX1_P, pins J2-40, J2-42 B128_TX1_N, B128_TX1_P, pins J2-37, J2-39 B128_RX0_N, B128_RX0_P, pins J2-46, J2-48 B128_TX0_N, B128_TX0_P, pins J2-43, J2-45 | 1 reference clock signal (B128_CLK1) from B2B connector J2 (pins J2-22, J2-24) to bank's pins D25/D26 1 reference clock signal (B128_CLK0) from programmable PLL clock generator U5 to bank's pins F25/F26 |
| 505 | GTR | J2 | 4 GTR lanes (4 RX / 4 TX) | B505_RX3_N, B505_RX3_P, pins J2-52, J2-54 B505_TX3_N, B505_TX3_P, pins J2-49, J2-51 B505_RX2_N, B505_RX2_P, pins J2-58, J2-60 B505_TX2_N, B505_TX2_P, pins J2-55, J2-57 B505_RX1_N, B505_RX1_P, pins J2-64, J2-66 B505_TX1_N, B505_TX1_P, pins J2-61, J2-63 B505_RX0_N, B505_RX0_P, pins J2-70, J2-72 B505_TX0_N, B505_TX0_P, pins J2-67, J2-69 | 2 reference clock signals (B505_CLK0, B505_CLK1) from B2B connector J2 (pins J2-10/J2-12, J2-16/J2-18) to bank's pins P25/P26, M25/M26 2 reference clock signal (B505_CLK2, B505_CLK3) from programmable PLL clock generator U5 to bank's pins K25/K26, H25/H26 |

Table 3: B2B connector pin-outs of available MGT lanes of the MPSoC.

JTAG Interface

JTAG access is provided through the MPSoC's PS configuration bank 503 with bank voltage PS_1V8.

| JTAG Signal | B2B Connector Pin |
|-------------|-------------------|
| TCK | J2-120 |
| TDI | J2-122 |
| TDO | J2-124 |
| TMS | J2-126 |

Table 4: B2B connector pin-out of JTAG interface.

Configuration Bank Control Signals

The Xilinx Zynq UltraScale+ MPSoC's PS configuration bank 503 control signal pins are accessible through B2B connector J2.

For further information about the particular control signals and how to use and evaluate them, refer to the [Xilinx Zynq UltraScale+ MPSoC TRM](#) and [UltraScale Architecture Configuration - User Guide](#).

| Signal | B2B Connector Pin | Function |
|-------------------------|------------------------------|---|
| DONE | J2-116 | PL configuration completed. |
| PROG_B | J2-100 | PL configuration reset signal. |
| INIT_B | J2-98 | PS is initialized after a power-on reset. |
| SRST_B | J2-96 | System reset. |
| MODE0 ... MODE3 | J2-109/J2-107/J2-105 /J2-103 | 4-bit boot mode pins. For further information about the boot modes refer to the Xilinx Zynq UltraScale+ MPSoC TRM section 'Boot and Configuration'. |
| ERR_STATUS / ERR_OUT | J2-86 / J2-88 | ERR_OUT signal is asserted for accidental loss of power, an error, or an exception in the MPSoC's Platform Management Unit (PMU). ERR_STATUS indicates a secure lock-down state. |
| PUDC_B | J2-127 | Pull-up during configuration (pulled-up to PL_1V8). |

Table 5: B2B connector pin-out of MPSoC's PS configuration bank.

Analog Input

The Xilinx Zynq UltraScale+ MPSoC provides differential pairs for analog input values. The pins are exposed to B2B-connector J2.

| Signal | B2B Connector Pin | Function |
|------------|-------------------|--------------------------------|
| V_P, V_N | J2-113, J2-115 | System Monitor |
| DX_P, DX_N | J2-119, J2-121 | Temperature-sensing diode pins |

Table 6: B2B connector pin-out of analog input pins

Quad SPI Interface

Quad SPI Flash memory ICs U7 and U17 are connected to the Zynq MPSoC PS QSPI0 interface via PS MIO bank 500, pins MIO0 ... MIO5 and MIO7 ... MIO12.

| MIO | Signal Name | U7 Pin | | MIO | Signal Name | U17 Pin |
|-----|---------------|--------|--|-----|---------------|---------|
| 0 | SPI Flash CLK | B2 | | 7 | SPI Flash CS | C2 |
| 1 | SPI Flash IO1 | D2 | | 8 | SPI Flash IO0 | D3 |
| 2 | SPI Flash IO2 | C4 | | 9 | SPI Flash IO1 | D2 |
| 3 | SPI Flash IO3 | D4 | | 10 | SPI Flash IO2 | C4 |
| 4 | SPI Flash IO0 | D3 | | 11 | SPI Flash IO3 | D4 |
| 5 | SPI Flash CS | C2 | | 12 | SPI Flash CLK | B2 |

Table 7: PS MIO pin assignment of the Quad SPI Flash memory ICs.

Boot Process

The boot device and mode of the Zynq UltraScale+ MPSoC can be selected via 4 dedicated pins accessible on B2B connector J2:

| Boot Mode Pin | B2B Pin |
|---------------|---------|
| PS_MODE0 | J2-109 |
| PS_MODE1 | J2-107 |
| PS_MODE2 | J2-105 |
| PS_MODE3 | J2-103 |

Table 8: Boot mode pins on B2B connector J2.

Following boot modes are possible on the TE0808 UltraScale+ module by generating the corresponding 4-bit code by the pins PS_MODE0 ... PS_MODE3 (little-endian alignment):

| Boot Mode | Mode Pins [3:0] | MIO Location | Description |
|-----------|-----------------|--------------|--|
| JTAG | 0x0 | JTAG | Dedicated PS interface. |
| QSPI32 | 0x2 | MIO[12:0] | Configured on module with dual QSPI Flash Memory. 32-bit addressing. Supports single and dual parallel configurations. Stack and dual stack is not supported. |
| SD0 | 0x3 | MIO[25:13] | Supports SD 2.0. |
| SD1 | 0x5 | MIO[51:38] | Supports SD 2.0. |
| eMMC_18 | 0x6 | MIO[22:13] | Supports eMMC 4.5 at 1.8V. |
| USB 0 | 0x7 | MIO[52:63] | Supports USB 2.0 and USB 3.0. |
| PJTAG_0 | 0x8 | MIO[29:26] | PS JTAG connection 0 option. |
| SD1-LS | 0xE | MIO[51:39] | Supports SD 3.0 with a required SD 3.0 compliant level shifter. |

Table 9: Selectable boot modes by dedicated boot mode pins.

For functional details see [ug1085 - Zynq UltraScale+ TRM \(Boot Modes Section\)](#).

On-board Peripherals

Flash

The TE0808 SoM can be configured with max. 512 MByte Flash memory for configuration and operation.

| Name | IC | Designator | PS7 | MIO | Notes |
|-----------|------------------|------------|-------|----------------|--|
| SPI Flash | N25Q256A11E1240E | U7 | QSPI0 | MIO0 ... MIO5 | dual parallel booting possible, 32 MByte memory per Flash IC at standard configuration |
| SPI Flash | N25Q256A11E1240E | U17 | QSPI0 | MIO7 ... MIO12 | as above |

Table 10: Peripherals connected to the PS MIO pins.

DDR4 SDRAM

The TE0808-04 SoM is equipped with with four DDR4-2400 SDRAM chip with up to 8 GByte memory density. The SDRAM chips are connected to the Zynq MPSoC's PS DDR controller (bank 504) with a 64-bit data bus.

Refer to the Xilinx Zynq UltraScale+ datasheet [DS925](#) for more information on whether the specific package of the Zynq UltraScale+ MPSoC supports.

Programmable PLL Clock Generator

Following table illustrates on-board Si5345A programmable clock multiplier chip inputs and outputs:

| Input | Connected to | Frequency | Notes |
|--------|---|---------------|--------------------------------|
| IN0 | On-board Oscillator (U25) | 25.000000 MHz | - |
| IN1 | B2B Connector pins J2-4, J2-6 (differential pair) | User | AC decoupling required on base |
| IN2 | B2B Connector pins J3-66, J3-68 (differential pair) | User | AC decoupling required on base |
| IN3 | OUT9 | User | Loop-back from OUT9 |
| Output | Connected to | Frequency | Notes |
| OUT0 | B2B Connector pins J2-3, J2-1 (differential pair) | User | Default off |
| OUT1 | B230 CLK0 | User | Default off |
| OUT2 | B229 CLK1 | User | Default off |
| OUT3 | B228 CLK1 | User | Default off |
| OUT4 | B505 CLK2 | User | Default off |
| OUT5 | B505 CLK3 | User | Default off |
| OUT6 | B128 CLK0 | User | Default off |
| OUT7 | B2B Connector pins J2-13, J2-15 (differential pair) | User | Default off |
| OUT8 | B2B Connector pins J2-7, J2-9 (differential pair) | User | Default off |
| OUT9 | IN3 (Loop-back) | User | Default off |
| XA/XB | Quartz (Y1) | 50.000 MHz | - |

Table 11: Programmable PLL clock generator input/output.

The Si5345A programmable clock generator's control interface pins are exposed to B2B connector J2. For further information refer to the Si5345A data sheet.

| Signal | B2B Connector Pin | Function |
|---------------------|-------------------|---|
| PLL_FINC | J2-81 | Frequency increment. |
| PLL_LOLN | J2-85 | Loss of lock (active-low). |
| PLL_SEL0 / PLL_SEL1 | J2-93 / J2-87 | Manual input switching. |
| PLL_FDEC | J2-94 | Frequency decrement. |
| PLL_RST | J2-89 | Device reset (active-low) |
| PLL_SCL / PLL_SDA | J2-90 / J2-92 | I ² C interface, external pull-ups needed for SCL / SDA lines. I ² C address in current configuration: 1101001b. |

Table 12: B2B connector pin-out of Si5345A programmable clock generator.



Si5345 OTP ROM is not programmed by default at delivery, so it is customers responsibility to either configure Si5345 during FSBL or then use SiLabs programmer and program the OTP ROM with customer fixed clock setup.

Si5345 OTP can only be programmed two times, as different user configurations may required different setup TE0808 is normally shipped with blank OTP. For more information refer to [Si5345 at SiLabs](#).

Oscillators

The TE0808-04 SoM is equipped with two on-board oscillators to provide the Zynq's MPSoC's PS configuration bank 503 with reference clock signals.

| Clock | Frequency | Bank 503 Pin | Connected to |
|--------------|---------------|--------------|----------------------|
| PS_CLK | 33.333333 MHz | P20 | MEMS Oscillator, U32 |
| PS_PAD (RTC) | 32.768 kHz | R22/R23 | Quartz crystal, Y2 |

Table 13: Reference clock-signals to PS configuration bank 503.

On-board LEDs

| LED | Color | Connected to | Description and Notes |
|-----|-------|---|--|
| D1 | Red | DONE signal (PS Configuration Bank 503) | This LED goes ON when power has been applied to the module and stays ON until MPSoC's programmable logic is configured properly. |

Table 14: LED's description.

Power and Power-On Sequence

Power Consumption

The maximum power consumption of a module mainly depends on the design which is running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki [FAQ](#).

| Power Input Pin | Typical Current |
|-----------------|-----------------|
| DCDCIN | TBD* |
| LP_DCDC | TBD* |
| PL_DCIN | TBD* |
| PS_BATT | TBD* |

Table 15: Maximum current of power supplies. *to be determined soon with reference design setup.

Power supply with minimum current capability of 3A for system startup is recommended. For the lowest power consumption and highest efficiency of on board DC/DC regulators it is recommended to powering the module from one single 3.3V supply. Except 'PS_BATT', all input power supplies have a nominal value of 3.3V. Although the input power supplies can be powered up in any order, it is recommended to power them up simultaneously.

The TE0808 module equipped with the Xilinx Zynq UltraScale+ MPSoC delivers a heterogeneous multi-processing system with integrated programmable logic and independently operable elements and is designed to meet embedded system power management requirement by advanced power management features. This features allow to offset the power and heat constraints against overall performance and operational efficiency.

This features allowing highly flexible power management are achieved by establishing Power Domains for power isolation. The Zynq UltraScale+ MPSoC has multiple power domains, whereby each power domain requires its own particular external DC-DC converters.

The Processing System contains three Power Domains:

- Battery Power Domain (BBRAM and RTC)
- Full-Power Domain (Application Processing Unit, DDR Controller, Graphics Processing Unit and High-Speed Connectivity)
- Low-Power Domain (Real-Time Processing Unit, Security and Configuration Unit, Platform Management Unit, System Monitor and General Connectivity)

The fourth Power Domain is for the Programmable Logic (PL). If individual Power Domain control is not required, power rails can be shared between domains.

On the TE0808-04 SoM, following power domains can be powered up individually with power rails available on the B2B connectors:

- Full-power domain, supplied by power rail **DCDCIN**
- Low-power domain, supplied by power rail **LP_DCDC**
- Programmable logic, supplied by power rail **PL_DCIN**
- Battery power domain, supplied by power rail **PS_BATT**

Each power domain has its own enable and power good signals. The power rail **GT_DCDC** is needed to generate the voltages for the Multi Gigabit Transceiver units of the Zynq UltraScale+ MPSoC.

Power Distribution Dependencies

The power rails DCDCIN, LP_DCDC, PL_DCIN, PS_BATT have to be powered up on the assigned pins of the B2B connectors as listed on the section "Power Rails". Except 'PS_BATT' (see section "Recommended Operation Conditions"), all power-rails can be powered from 3.3V power sources (also share the same source, if power domain control is not required).

There are following dependencies how the initial voltages of the power rails on the B2B connectors are distributed to the on-board DC-DC converters, which power up further DC-DC converters and the particular on-board voltages:

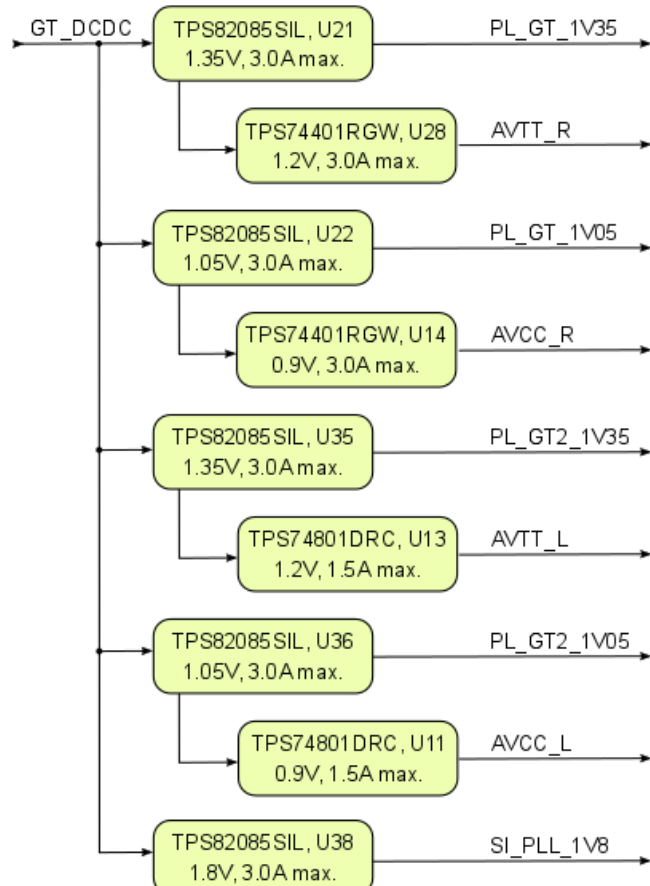
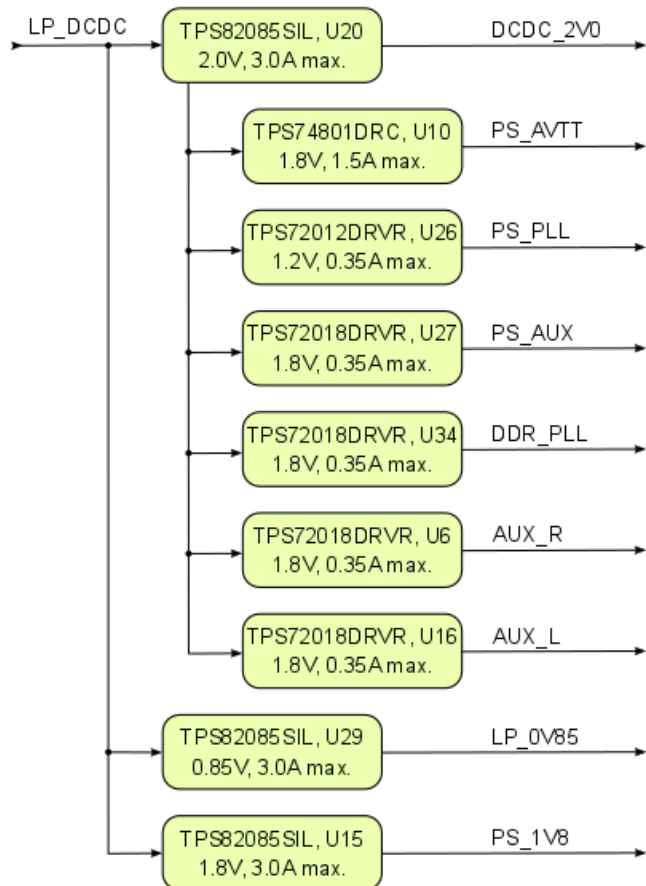
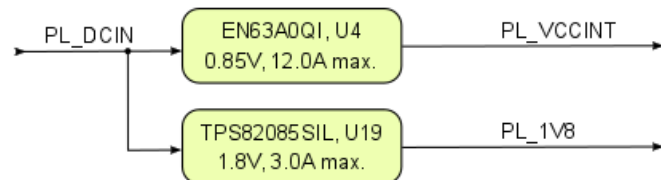
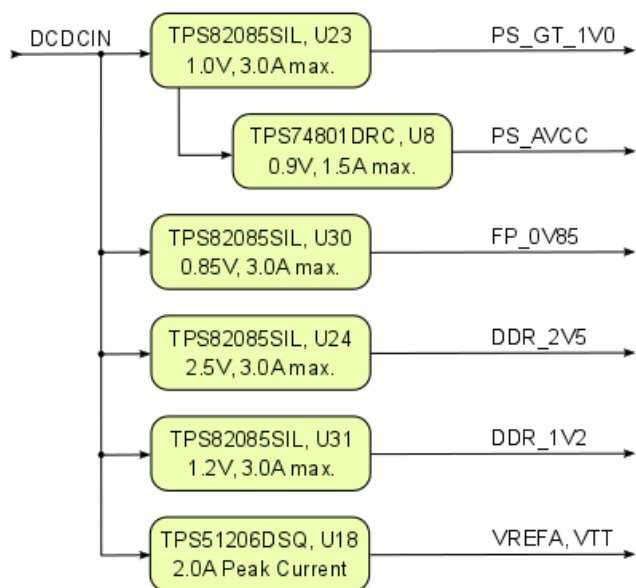


Figure 3: Power Distribution Diagram.



Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

Power-On Sequence Diagram

The TE0808 SoM meets the recommended criteria to power up the Xilinx Zynq UltraScale+ MPSoC properly by keeping a specific sequence of enabling the on-board DC-DC converters dedicated to the particular Power Domains and powering up the on-board voltages.

The on-board voltages of the TE0808 SoM will be powered-up in order of a determined sequence by activating the above-mentioned power rails and the Enable-Signals of the DC-DC converters. The on-board voltages will be powered up at three steps.

1. Low-Power Domain (LPD) and on-board Si5345A programmable clock generator supply voltage
2. Programmable Logic (PL) and Full-Power Domain (FPD)
3. GTH, PS GTR transceiver and DDR memory

Hence, those three power instances will be powered up consecutively and the Power-Good-Signals of the previous instance has to be asserted.

Following diagram describes the sequence of enabling the three power instances utilizing the DC-DC converter control signals (Enable, Power-Good), which will power-up in descending order as listed in the blocks of the diagram.

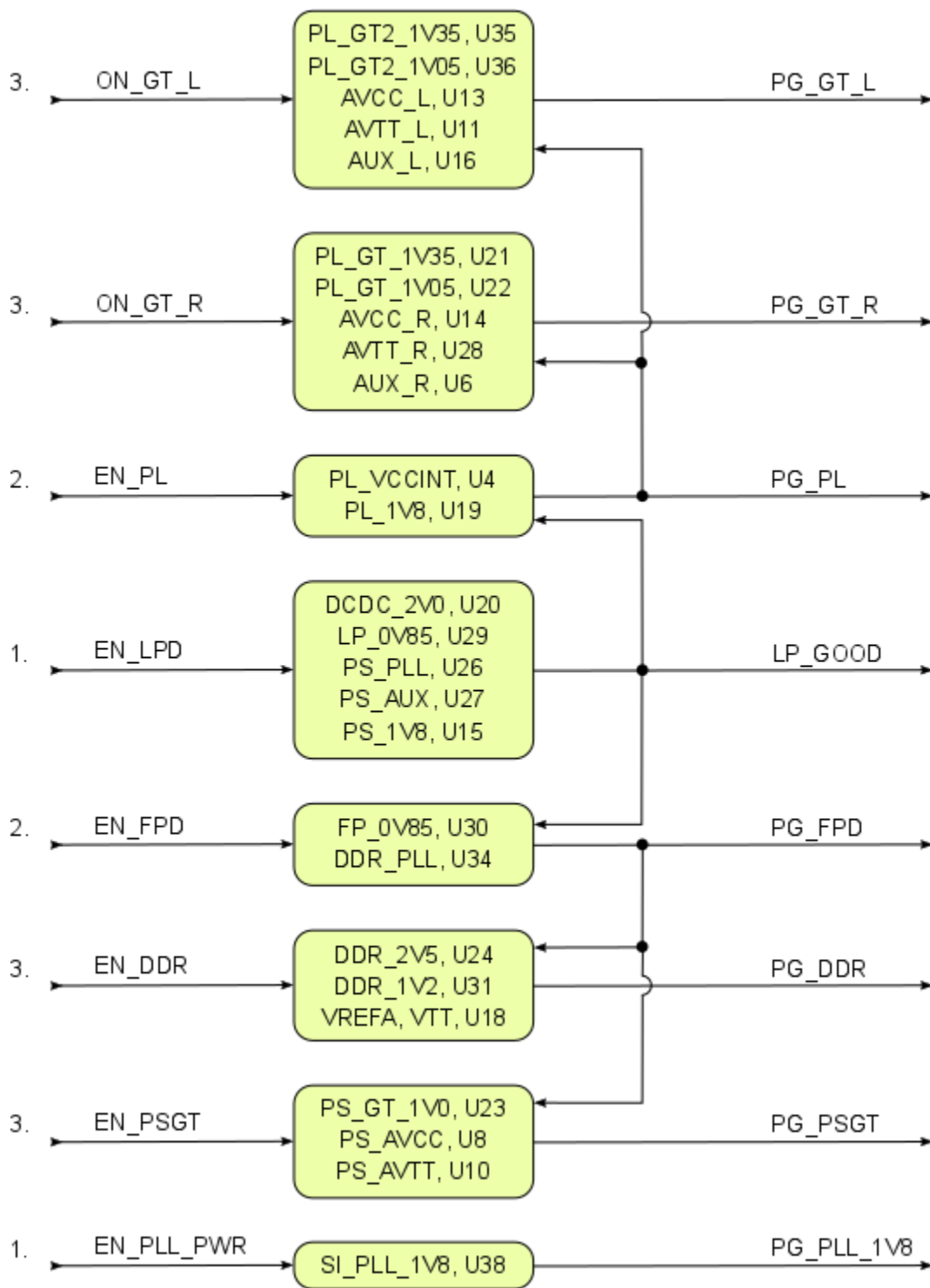


Figure 4: Power-On Sequence Utilizing DC-DC Converter Control Signals.

Operation Conditions of the DC-DC Converter Control Signals

The control signals have to be asserted on the B2B connector J2, whereby some of the Power-Good signals need external pull-up resistors.

| Enable-Signal | B2B Connector Pin | Max. Voltage | Note | | Power-Good-Signal | B2B Connector Pin | Pull-up Resistor | Note |
|---------------|-------------------|--------------|---|--|-------------------|-------------------|---|------------------------------------|
| EN_LPD | J2-108 | 6V | TPS82085SIL data sheet | | LP_GOOD | J2-106 | 4K7, pulled up to LP_DCDC | - |
| EN_FPD | J2-102 | DCDCIN | NC7S08P5X data sheet | | PG_FPD | J2-110 | 4K7, pulled up to DCDCIN | - |
| EN_PL | J2-101 | PL_DCIN | left floating for logic high (drive to GND for logic low) | | PG_PL | J2-104 | 4K7, pulled up to PL_DCIN | TPS82085SIL / NC7S08P5X data sheet |
| EN_DDR | J2-112 | DCDCIN | NC7S08P5X data sheet | | PG_DDR | J2-114 | 4K7, pulled up to DCDCIN | - |
| EN_PSGT | J2-84 | DCDCIN | NC7S08P5X data sheet | | PG_PSGT | J2-82 | External pull-up needed (max. 5.5V), max. sink current 1 mA | TPS74801 data sheet |
| EN_GT_R | J2-95 | GT_DCDC | NC7S08P5X data sheet | | PG_GT_R | J2-91 | External pull-up needed (max. 5.5V), max. sink current 1 mA | TPS74401 data sheet |
| EN_GT_L | J2-79 | GT_DCDC | NC7S08P5X data sheet | | PG_GT_L | J2-97 | External pull-up needed (max. 5.5V), max. sink current 1 mA | TPS74801 data sheet |
| EN_PLL_PWR | J2-77 | 6V | TPS82085SIL data sheet | | PG_PLL_1V8 | J2-80 | External pull-up needed (max. 5.5V), max. sink current 1 mA | TPS82085SIL data sheet |

Table 16: Recommended operation conditions of DC-DC converter control signals.



To avoid any damage to the MPSoC module, check for stabilized on-board voltages in steady state before powering up the MPSoC's I/O bank voltages VCCOx. All I/Os should be tri-stated during power-on sequence.

Core voltages and main supply voltages have to reach stable state and their "Power Good"-signals have to be asserted before other voltages like bank's I/O voltages (VCCOx) can be powered up.

It is important that all PS and PL I/Os are tri-stated at power-on until the "Power Good"-signals are high, meaning that all on-module voltages have become stable and module is properly powered up.

See Xilinx datasheet [DS925](#) for additional information. User should also check related base board documentation when intending base board design for TE0808 SoM.

Voltage Monitor Circuit

The voltages LP_DCDC and LP_0V85 are monitored by the voltage monitor circuit U41, which generates the POR_B reset signal at power-on. A manual reset is also possible by driving the MR-pin (J2-83) to GND. Leave this pin unconnected or connect to VDD (LP_DCDC) when unused.

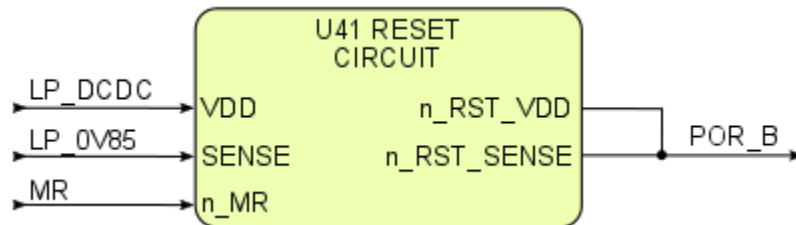


Figure 5: Voltage monitor circuit

Power Rails

| Power Rail Name | B2B J1 Pins | B2B J2 Pins | B2B J3 Pins | Directions | Note |
|-----------------|-------------------------|--|--------------------|------------|--|
| PL_DCIN | 151, 153, 155, 157, 159 | - | - | Input | - |
| DCDCIN | - | 154, 156, 158, 160, 153, 155, 157, 159 | - | Input | - |
| LP_DCDC | - | 138, 140, 142, 144 | - | Input | - |
| PS_BATT | - | 125 | - | Input | - |
| GT_DCDC | - | - | 157, 158, 159, 160 | Input | - |
| PLL_3V3 | - | - | 152 | Input | U5 (programmable PLL) 3.3V nominal input |
| SI_PLL_1V8 | - | - | 151 | Output | Internal voltage level 1.8V nominal output |
| PS_1V8 | - | 99 | 147, 148 | Output | Internal voltage level 1.8V nominal output |
| PL_1V8 | 91, 121 | - | - | Output | Internal voltage level 1.8V nominal output |
| DDR_1V2 | - | 135 | - | Output | Internal voltage level 1.2V nominal output |

Table 17: Power rails of the MPSoC module on accessible connectors.

Bank Voltages

| Bank | Type | Schematic Name / B2B Connector Pins | Voltage | Reference Input Voltage | Voltage Range |
|------|--------|-------------------------------------|---------|-------------------------|---------------|
| 47 | HD | VCCO47, pins J3-43, J3-44 | user | - | max. 3.3V |
| 48 | HD | VCCO48, pins J3-15, J3-16 | user | - | max. 3.3V |
| 64 | HP | VCCO64, J4-58, J4-106 | user | VREF_64, pin J4-88 | max. 1.8V |
| 65 | HP | VCCO65, J4-69, J4-105 | user | VREF_65, pin J4-15 | max. 1.8V |
| 66 | HP | VCCO66, J1-90, J1-120 | user | VREF_66, pin J1-108 | max. 1.8V |
| 500 | MIO | PS_1V8 | 1.8V | - | - |
| 501 | MIO | PS_1V8 | 1.8V | - | - |
| 502 | MIO | PS_1V8 | 1.8V | - | - |
| 503 | CONFIG | PS_1V8 | 1.8V | - | - |

Table 18: Range of MPSoC module's bank voltages.

B2B connectors

5.2 x 7.6 cm UltraSoM+ modules use four Samtec Razor Beam LP Terminal Strip ([ST5](#)) on the bottom side.

- 4x REF-192552-02 (160-pins)
 - ST5 Mates with SS5

5.2 x 7.6 cm UltraSoM+ carrier use four Samtec Razor Beam LP Socket Strip ([SS5](#)) on the top side.

- 4x REF192552-01 (160-pins)
 - SS5 Mates with ST5

Features

- Board-to-Board Connector 160-pins, 80 contacts per row
- Ultrafine .0197" (0.50 mm) pitch
- Narrow body design saves space on board
- Lead style -03.5
- Samtec 28+ Gbps Solution
- Mates with: ST5
- Insulator Material: Liquid Crystal Polymer, schwarz
- Operating Temperature Range: -55°C bis +125°C
- Lead-Free Solderable: Yes
- RoHS Konform: Yes

Connector Stacking height

When using the standard type on baseboard and module, the mating height is 5 mm.

Other mating heights are possible by using connectors with a different height:

| Order number | REF number | Samtec Number | Type | Contribution to stacking height | Comment |
|--------------|---------------|----------------------|---------------------|---------------------------------|------------------------------------|
| 27219 | REF192552-01 | SS5-80-3.50-L-D-K-TR | Baseboard connector | 3.5mm | Standard connector used on carrier |
| 27018 | REF-189545-02 | SS5-80-3.00-L-D-K-TR | Baseboard connector | 3 mm | Assembly option on request |
| 27220 | REF-192552-02 | ST5-80-1.50-L-D-P-TR | Module connector | 1.5 mm | Standard connector used on modules |
| 27017 | REF-189545-01 | ST5-80-1.00-L-D-P-TR | Module connector | 1 mm | Assembly option on request |

Connectors.

The module can be manufactured using other connectors upon request.

Current Rating

Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

Connector Speed Ratings

The connector speed rating depends on the stacking height:

| Stacking height | Speed rating |
|--------------------|----------------|
| 4 mm, Single-Ended | 13GHz/26Gbps |
| 4 mm, Differential | 13.5GHz/27Gbps |
| 5 mm, Single-Ended | 13.5GHz/27Gbps |
| 5 mm, Differential | 20GHz/40 Gbps |

Speed rating.

The SS5/ST5 series board-to-board spacing is currently available in 4mm (0.157"), 4.5mm (0.177") and 5mm (0.197") stack heights.

The data in the reports is applicable only to the 4mm and 5mm board-to-board mated connector stack height.

Manufacturer Documentation

File

Modified

| | |
|--|-------------------------------|
| PDF File hsc-report-sma_st5-ss5-04mm_web.pdf | 30 05, 2017 by Susanne Kunath |
| PDF File hsc-report-sma_st5-ss5-05mm_web.pdf | 30 05, 2017 by Susanne Kunath |
| PDF File REF-192552-01.pdf | 13 11, 2017 by John Hartfiel |
| PDF File REF-192552-02.pdf | 13 11, 2017 by John Hartfiel |
| PDF File ss5.pdf | 13 11, 2017 by John Hartfiel |
| PDF File ss5-st5.pdf | 13 11, 2017 by John Hartfiel |
| PDF File ss5-xx-x.xx-x-d-k-tr-mkt.pdf | 13 11, 2017 by John Hartfiel |
| PDF File st5.pdf | 13 11, 2017 by John Hartfiel |
| PDF File st5-xx-x.xx-x-d-p-tr-mkt.pdf | 13 11, 2017 by John Hartfiel |

[Download All](#)

Variants Currently In Production

| Module Variant | Zynq UltraScale+ MPSoC | DDR4 | Junction Temperature | Operating Temperature Range |
|-----------------------------------|------------------------|------|----------------------|------------------------------|
| TE0808-04-09EG-1EA | XCZU9EG-1FFVC900E | 2GB | 0°C - 100°C | Extended Temperature Range |
| TE0808-04-09EG-1EB | XCZU9EG-1FFVC900E | 4GB | 0°C - 100°C | Extended Temperature Range |
| TE0808-04-09EG-1ED ⁽¹⁾ | XCZU9EG-1FFVC900E | 4GB | 0°C - 100°C | Extended Temperature Range |
| TE0808-04-09EG-2IB | XCZU9EG-2FFVC900I | 4GB | -40°C - 100°C | Industrial Temperature Range |

(1) Note: Lower B2B connector profile, check distance bolt of between module and carrier

Table 19: Differences between variants of Module TE0808-04

Technical Specifications

Absolute Maximum Ratings

| Parameter | Min | Max | Unit | Notes / Reference Document |
|-----------------------|------|-----|------|---|
| PL_DCIN | -0.3 | 4 | V | TPS82085SIL / EN63A0QI data sheet / Limit is LP_DCDC over EN/PG |
| DCDCIN | -0.3 | 4 | V | TPS82085SIL / TPS51206 data sheet / Limit is LP_DCDC over EN/PG |
| LP_DCDC | -0.3 | 4 | V | TPS3106K33DBVR data sheet |
| GT_DCDC | -0.3 | 4 | V | TPS82085SIL data sheet / Limit is LP_DCDC over EN/PG |
| PS_BATT | -0.5 | 2 | V | Xilinx DS925 data sheet |
| PLL_3V3 | -0.5 | 3.8 | V | Si5345/44/42 data sheet |
| VCCO for HD I/O banks | -0.5 | 3.4 | V | Xilinx DS925 data sheet |
| VCCO for HP I/O banks | -0.5 | 2 | V | Xilinx DS925 data sheet |
| VREF | -0.5 | 2 | V | Xilinx DS925 data sheet |

| | | | | |
|---|-------|------------------|----|--|
| I/O input voltage for HD I/O banks | -0.55 | VCCO + 0.55 | V | Xilinx DS925 data sheet |
| I/O input voltage for HP I/O banks | -0.55 | VCCO + 0.55 | V | Xilinx DS925 data sheet |
| PS I/O input voltage (MIO pins) | -0.5 | VCCO_PSIO + 0.55 | V | Xilinx DS925 data sheet, VCCO_PSIO 1.8V nominally |
| Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage | -0.5 | 1.2 | V | Xilinx DS925 data sheet |
| Voltage on input pins of NC7S08P5X 2-Input AND Gate | -0.5 | VCC + 0.5 | V | NC7S08P5X data sheet, see schematic for VCC |
| Voltage on input pins (nMR) of TPS3106K33DBVR Voltage Monitor, U41 | -0.3 | VDD + 0.3 | V | TPS3106 data sheet, VDD = LP_DCDC |
| "Enable"-signals on TPS82085SIL (EN_PLL_PWR, EN_LPD) | -0.3 | 7 | V | TPS82085SIL data sheet |
| Storage temperature (ambient) | -40 | 100 | °C | ROHM Semiconductor SML-P11 Series data sheet |



Assembly variants for higher storage temperature range are available on request.

Recommended Operating Conditions

| Parameter | Min | Max | Unit | Notes / Reference Document |
|--|------|-----------------|------|--|
| PL_DCIN | 3.3 | 3.6 | V | EN63A0QI / TPS82085SIL data sheet / Limit is LP_DCDC over EN/PG |
| DCDCIN | 3.3 | 3.6 | V | TPS82085SIL / TPS51206PSQ data sheet / Limit is LP_DCDC over EN/PG |
| LP_DCDC | 3.3 | 3.6 | V | TPS3106K33DBVR data sheet |
| GT_DCDC | 3.3 | 3.6 | V | TPS82085SIL data sheet/ Limit is LP_DCDC over EN/PG |
| PS_BATT | 1.2 | 1.5 | V | Xilinx DS925 data sheet |
| PLL_3V3 | 3.14 | 3.47 | V | Si5345/44/42 data sheet 3.3V typical |
| VCCO for HD I/O banks | 1.14 | 3.4 | V | Xilinx DS925 data sheet |
| VCCO for HP I/O banks | 0.95 | 1.9 | V | Xilinx DS925 data sheet |
| I/O input voltage for HD I/O banks. | -0.2 | VCCO + 0.2 | V | Xilinx DS925 data sheet |
| I/O input voltage for HP I/O banks | -0.2 | VCCO + 0.2 | V | Xilinx DS925 data sheet |
| PS I/O input voltage (MIO pins) | -0.2 | VCCO_PSIO + 0.2 | V | Xilinx DS925 data sheet, VCCO_PSIO 1.8V nominally |
| Voltage on input pins of NC7S08P5X 2-Input AND Gate | 0 | VCC | V | NC7S08P5X data sheet, see schematic for VCC |
| Voltage on input pin 'MR' of TPS3106K33DBVR Voltage Monitor, U41 | 0 | VDD | V | TPS3106 data sheet, VDD = LP_DCDC |



Please check Xilinx datasheet [DS925](#) for complete list of absolute maximum and recommended operating ratings.

Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial grade: -40°C to +85°C.

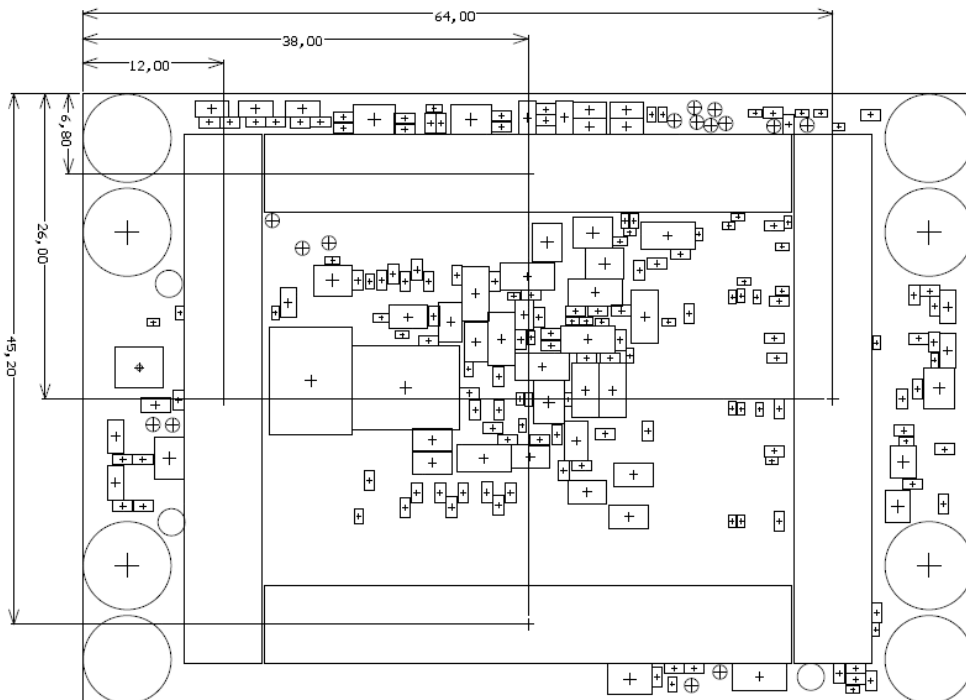
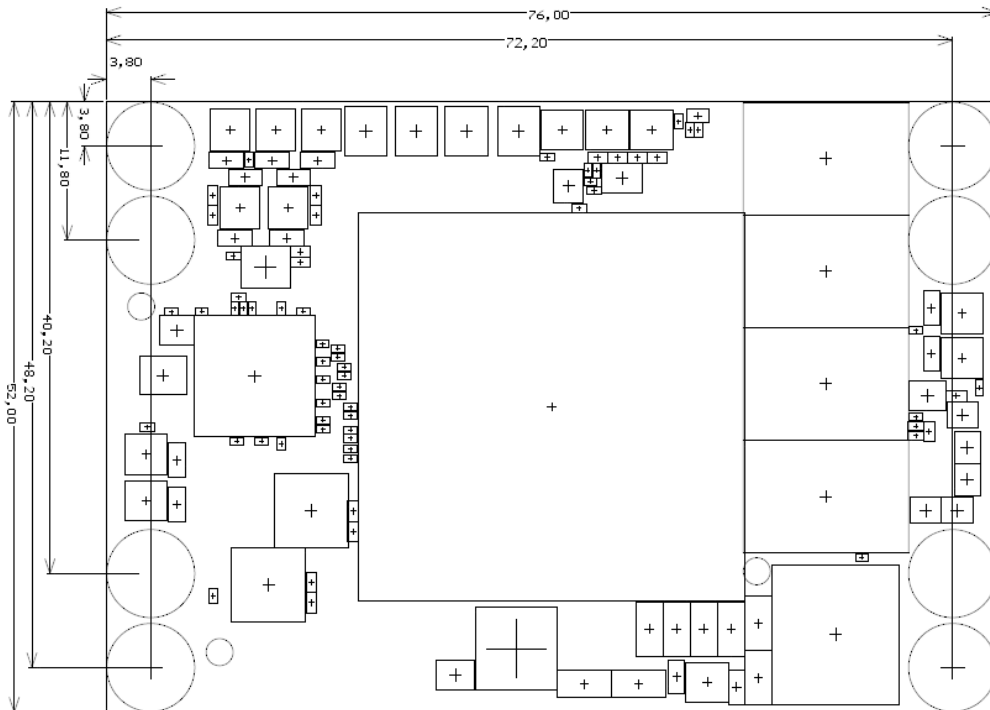
Extended grade: 0°C to +85°C.

The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

Physical Dimensions

- Module size: 52 mm × 76 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 5mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 3mm. Please download the step model for exact numbers

All dimensions are given in millimeters.

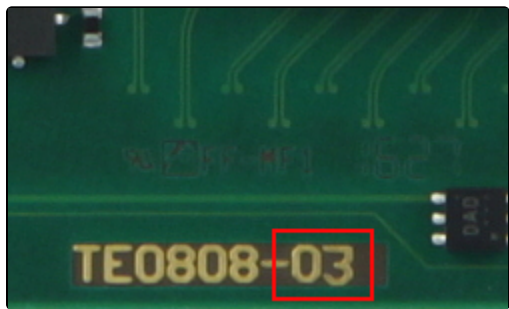


Revision History

Hardware Revision History

| Date | Revision | Notes | Link to PCN | Documentation Link |
|------------|----------|------------------------------|-------------|---------------------------|
| - | 04 | First production silicon | - | TE0808-04 |
| - | 03 | Second ES production release | - | TE0808-03 |
| 2016-03-09 | 02 | First ES production release | - | TE0808-02 |
| - | 01 | Prototypes | - | - |

Hardware revision number is written on the PCB board together with the module model number separated by the dash.



Document Change History

| Date | Revision | Contributors | Description |
|------|----------|--------------|-------------|
|------|----------|--------------|-------------|

| | | | |
|--|--|--|---|
| <p>Error rendering macro 'page-info'</p> <p>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> | <p>Error rendering macro 'page-info'</p> <p>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> | <p>Error rendering macro 'page-info'</p> <p>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> | <ul style="list-style-type: none"> • typo DDR section |
| 2022-09-13 | v.41 | Vadim Yunitski | <ul style="list-style-type: none"> • Updated PG_PL pull-up resistor requirements |
| 2021-09-07 | V.39 | John Hartfiel | <ul style="list-style-type: none"> • Correction Power section |
| 2021-05-17 | v.37 | John Hartfiel | <ul style="list-style-type: none"> • typo correction in DDR section |

| | | | |
|------------|------|-------------------|---|
| 2021-03-11 | v.35 | Antti Lukats | <ul style="list-style-type: none"> • typo correction in PLL_RST • add pin on power rails table • correction MGT Lane assignment • correction MGT CLK assignment |
| 2019-01-27 | v.30 | Martin Rohrmüller | <ul style="list-style-type: none"> • Corrected clock connection to J2 |
| 2018-11-20 | v.29 | John Hartfiel | <ul style="list-style-type: none"> • Notes for power supply |
| 2018-08-27 | v.27 | John Hartfiel | <ul style="list-style-type: none"> • typo correction SI5345 I2C address |
| 2028-06-28 | v.26 | John Hartfiel | <ul style="list-style-type: none"> • typo SI5348 B2B IOs + link correction |
| 2017-11-13 | v.24 | Ali Naseri | <ul style="list-style-type: none"> • updated B2B connector max. current rating per pin |
| 2017-11-13 | v.22 | John Hartfiel | <ul style="list-style-type: none"> • rework B2B section |

| | | | |
|------------|------|---------------------------|---|
| 2017-10-20 | v.21 | Ali Naseri | <ul style="list-style-type: none"> • Update links (pdf, documentation) to revision 4 • ES silicon note removed |
| 2017-08-28 | v.15 | John Hartfiel | <ul style="list-style-type: none"> • Update section: Variants Currently In Production |
| 2017-08-28 | v.14 | Jan Kumann | <ul style="list-style-type: none"> • Block diagram changed. • SPI flash section fixed. • Few smaller improvements. |
| 2017-08-15 | v.12 | Vitali Tsiukala | Changed signals count in the B2B connectors table |
| 2017-08-15 | v.11 | John Hartfiel, Ali Naseri | <ul style="list-style-type: none"> • PCB REV04 Initial release • update boot mode section |
| 2017-02-06 | v.1 | Jan Kumann | Initial document |

Disclaimer

Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

Document Warranty

The material contained in this document is provided "as is" and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method `jdk.proxy279.$Proxy4022#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`