

# TEF1001-REV01 CPLD

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## Overview

Firmware for PCB-Master CPLD with designator U5: LCMX02-1200HC.

## Feature Summary

- Power Management
- Reset Management
- LED Control
- FAN Control
- I2C MUX

## Firmware Revision and supported PCB Revision

See Document Change History

## Product Specification

## Port Description

| Name / opt. VHD Name | Direction | Pin | Description                     |
|----------------------|-----------|-----|---------------------------------|
| 200MHZCLK_EN         | out       | 30  |                                 |
| BUTTON               | in        | 77  | Reset Button                    |
| CPLD_JTAG_TCK        |           | 91  | not accessible as IO            |
| CPLD_JTAG_TDI        |           | 94  | not accessible as IO            |
| CPLD_JTAG_TDO        |           | 95  | not accessible as IO            |
| CPLD_JTAG_TMS        |           | 90  | not accessible as IO            |
| DDR3_SCL             | inout     | 43  | I2C connected to FPGA           |
| DDR3_SDA             | inout     | 42  | I2C connected to FPGA           |
| DONE                 | in        | 18  | FPGA Done                       |
| EN_1V8               | out       | 58  | Power Enable                    |
| EN_3V3FMC            | out       | 60  | Power Enable                    |
| EN_FMC_VADJ          | out       | 51  | Power Enable                    |
| F1PWM                | out       | 98  | FAN                             |
| F1SENSE              | in        | 99  | FAN / <i>currently_not_used</i> |
| FEX_DIR              |           | 19  | <i>/ currently_not_used</i>     |
| FEX0                 | out       | 12  | PERST from PCIe slot            |
| FEX1                 |           | 15  | <i>/ currently_not_used</i>     |
| FEX10                |           | 4   | <i>/ currently_not_used</i>     |
| FEX11                | in        | 10  | User LED                        |
| FEX2                 |           | 13  | <i>/ currently_not_used</i>     |
| FEX3                 |           | 9   | <i>/ currently_not_used</i>     |
| FEX4                 |           | 3   | <i>/ currently_not_used</i>     |
| FEX5                 |           | 7   | <i>/ currently_not_used</i>     |
| FEX6                 |           | 24  | <i>/ currently_not_used</i>     |
| FEX7                 |           | 17  | <i>/ currently_not_used</i>     |
| FEX8                 |           | 21  | <i>/ currently_not_used</i>     |
| FEX9                 |           | 25  | <i>/ currently_not_used</i>     |
| FMC_PG_C2M           |           | 69  | <i>/ currently_not_used</i>     |
| FMC_PG_M2C           |           | 68  | <i>/ currently_not_used</i>     |
| FMC_PRSNT_M2C_L      |           | 70  | <i>/ currently_not_used</i>     |
| FMC_SCL              |           | 49  | I2C connected to FPGA           |
| FMC_SDA              |           | 48  | I2C connected to FPGA           |
| FMC_TCK              |           | 27  | <i>/ currently_not_used</i>     |
| FMC_TDI              |           | 31  | <i>/ currently_not_used</i>     |
| FMC_TDO              |           | 32  | <i>/ currently_not_used</i>     |
| FMC_TMS              |           | 28  | <i>/ currently_not_used</i>     |
| FMC_TRST             |           | 36  | <i>/ currently_not_used</i>     |
| FPGA_IIC_OE          |           | 14  | I2C FPGA                        |
| FPGA_IIC_SCL         |           | 1   | I2C FPGA                        |

|                |       |    |                                     |
|----------------|-------|----|-------------------------------------|
| FPGA_IIC_SDA   |       | 16 | I2C FPGA                            |
| LED1           | out   | 76 | Status LED D1 (green)               |
| LTM_1V_IO0     |       | 86 | Power Good                          |
| LTM_1V_IO1     |       | 88 | Power Good                          |
| LTM_1V5_4V_IO0 |       | 85 | Power Good                          |
| LTM_1V5_4V_IO1 |       | 83 | Power Good                          |
| LTM_1V5_RUN    |       | 74 | / currently_not_used                |
| LTM_4V_RUN     |       | 75 | / currently_not_used                |
| LTM_SCL        |       | 67 | I2C connected to FPGA               |
| LTM_SDA        |       | 66 | I2C connected to FPGA               |
| LTM1_ALERT     |       | 65 | / currently_not_used                |
| LTM2_ALERT     |       | 64 | / currently_not_used                |
| PCIE_RSTB      | in    | 37 | PERST from PCIe card edge connector |
| PG_1V8         | in    | 59 | Power Good                          |
| PG_3V3         | in    | 61 | Power Good                          |
| PG_FMC_VADJ    | in    | 52 | Power Good                          |
| PLL_SCL        | inout | 2  | I2C SI5338                          |
| PLL_SDA        | inout | 8  | I2C SI5338                          |
| PROGRAM_B      | out   | 20 | FPGA PROG_B                         |
| VID0_FMC_VADJ  | out   | 53 | FMC EN5365QI power selection pin    |
| VID1_FMC_VADJ  | out   | 54 | FMC EN5365QI power selection pin    |
| VID2_FMC_VADJ  | out   | 57 | FMC EN5365QI power selection pin    |

## Functional Description

### JTAG

CPLD JTAG is always enabled.

### Power

Power sequence on will be executed over 4 States:

- State 1 IDLE: Wait until LTM\_1V\_IO0 (1V), LTM\_1V\_IO1 (1V) and LTM\_1V5\_4V\_IO1 (4V) is available.
- State 2 PS1: Enables 1V8, 3V3FMC and VADJ. Wait until PG\_1V8 (1.8V), PG\_3V3 (3.3V) and PG\_FMC\_VADJ (FMC VADJ) is available.
- State 3 PS2: Wait until LTM\_1V5\_4V\_IO0 (1.5V) is available
- State 4 RDY: All power on

State machine restart power sequencing, if on of the power good signal are lost.

FMC VADJ is set to 1.8V.

### Reset

PROGRAM\_B is controlled by push button after power up sequencing is ready.

CLK

200MHz CLK is enabled after power up.

I2C

Connect SI5338, LTM and FMC, SODIMM I2C and internal FAN Control to FPGA I2C Bus.

FAN1

I2C Baseaddress: 0x74 (changeable with Firmware update). I2C with 8Bit Register Address with 8Bit Data. I2C CLK currently 20 MHz supported.

Write Access:

| Register Address | Name     | Description                     |
|------------------|----------|---------------------------------|
| 0                | FAN CTRL | Enable FAN1 (Bit7)              |
| 1                | FAN1 PWM | FAN1 PWM (0%-100%, Default 80%) |

Read Access:

| Register Address | Name     | Description                 |
|------------------|----------|-----------------------------|
| 0                | FAN CTRL | FAN Control register        |
| 1                | FAN1 RPS | FAN1 Revolutions per second |

Button

Button is debounced and controls PROG\_B signal from FPGA.

LED

LED is used as Status LED for power management and programming. Status depends on blink sequence.

| Status                           | Blink sequence | Comment                                                    |
|----------------------------------|----------------|------------------------------------------------------------|
| Error - Power IDLE state         | *****          | Reset or Main Power Problem                                |
| Error - Power PS1 state          | ****000        | Periphery Power Problem (1.8V, 3.3V, FMC VADJ)             |
| Error - Power PS2 state          | ***0000        | DDR Bank Power Problem (1.5V)                              |
| Power Ready, FPGA not programmed | **00000        | ~0,7 Hz, duty cycle 3/8                                    |
| --                               | *000000        | ~0,7 Hz, duty cycle 2/8, currently not used                |
| --                               | *0000000       | ~0,7 Hz, duty cycle 1/8, currently not used                |
| User Mode                        | user defined   | Power Ready, FPGA programmed, LED is accessible over FEX11 |

Appx. A: Change History and Legal Notices

# Revision Changes

CPLD REV01 to REV02

- BUGFIX: PCIe Reset
- USER LED accessible
- I2C for SI5338, LTM, FMC, SODIMM
- Add FAN Control over I2C

# Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

| Date | Document Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | CPLD Firmware Revision | Supported PCB Revision | Authors                                                                                                                                                                                                                                                                      | Description                                                                                     |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|
|      | <div>Error rendering macro 'page-info'</div> <div>Ambiguous method overloading for method jdk.<br/>proxy279.\$Proxy4022#hasContentLevel<br/>Permission. Cannot resolve which method to invoke for [null, class java.<br/>lang.String, class com.atlassian.<br/>confluence.pages.Page] due to<br/>overlapping prototypes between:<br/>[interface com.atlassian.confluence.user.<br/>ConfluenceUser, class java.lang.String,<br/>class com.atlassian.confluence.core.<br/>ContentEntityObject] [interface com.<br/>atlassian.user.User, class java.lang.<br/>String, class com.atlassian.confluence.<br/>core.ContentEntityObject]</div> <div> Unknown macro: 'metadata'</div> | REV02                  | REV01                  | <div>Error<br/>render<br/>ing<br/>macro<br/>'page-<br/>info'</div> <div>Ambig<br/>uous<br/>metho<br/>d<br/>overlo<br/>ading<br/>for<br/>metho<br/>d jdk.<br/>proxy2<br/>79.\$Pr<br/>oxy402<br/>2#has<br/>Conten<br/>tLevel<br/>Permis<br/>sion.<br/>Cannot<br/>resolve</div> | <ul style="list-style-type: none"><li>• REV02 finished Firmware Releases (2017-11-28)</li></ul> |

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| 2017-08-06 | v.4 | REV01 | REV01 | John Hartfiel                                                                                                                                                                                                                                                                                                                                       | <ul style="list-style-type: none"><li>• REV01 finished</li></ul>  |
| 2017-05-29 | v.1 | ---   |       | <div></div>                                                                                                                                                                                                                                                                                                                                         | <ul style="list-style-type: none"><li>• Initial release</li></ul> |

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### Error rendering macro 'page-info'

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