TEM0001 TRM

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Overview

The Trenz Electronic TEM0001 is a low cost small-sized FPGA module integrating a Microsemi SmartFusion2 FPGA SoC and 8 MByte Flash memory for configuration and operation.

Key Features

- Microsemi SmartFusion2 SoC FPGA
- 8 MByte SDRAM
- 8 MByte QSPI Flash memory
- 25 MHz system clock and 32.768 KHz auxiliary clock
- JTAG and UART over Micro USB connector
- 1x 3-pin header for Live Probes
- 1x PMOD header providing 8 I/O
- 2x 14-pin headers (2,54 mm pitch) providing 23 I/O

- 9 user LEDs
- 1 user push button
- 3.3V single power supply with on-board voltage regulators
- Size 61.5 x 25 mm

Additional assembly options are available for cost or performance optimization upon request.

Block Diagram

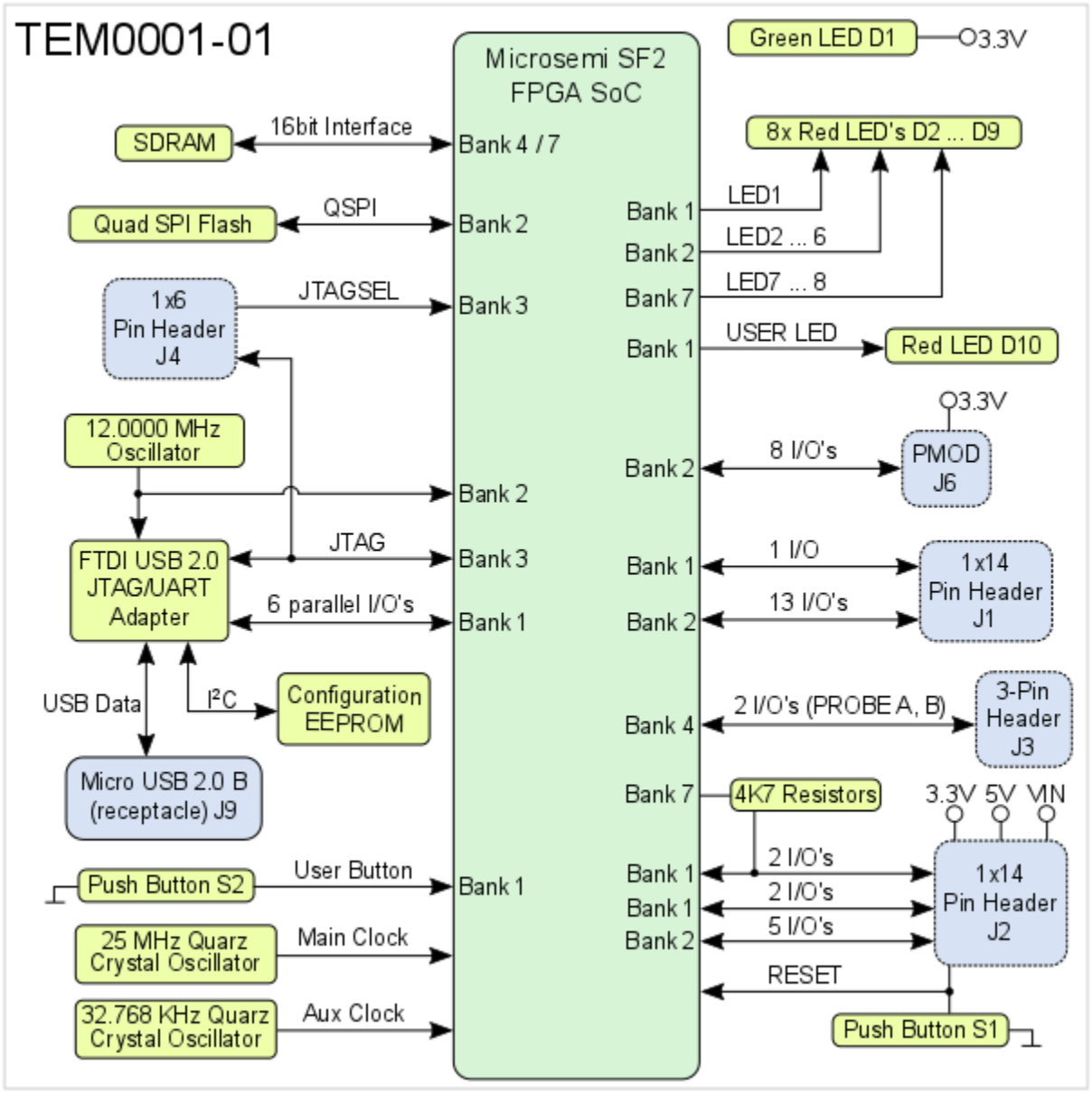

Figure 1: TEM0001-01 block diagram

Main Components

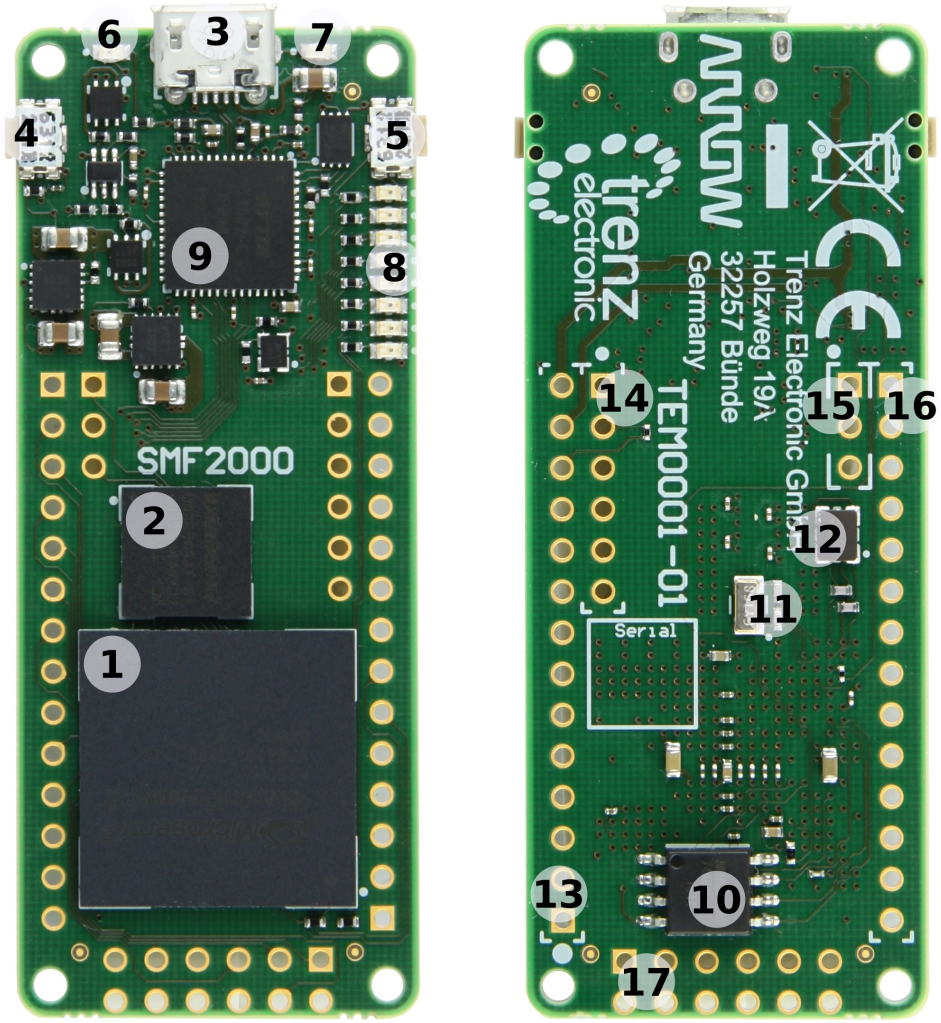

Figure 2: TEM0001-01 FPGA module

1. Microsemi SmartFusion2 FPGA SoC, U5
2. 8 Mbyte SDRAM 166MHz, U2
3. Micro USB2 B socket (receptacle), J9
4. Switch button (reset), S1
5. Switch button (user), S2
6. Red LED (user), D10
7. Green LED (indicating supply voltage), D1
8. 8x red LEDs (user), D2 - D9
9. FTDI USB2 to JTAG/UART interface, U3
10. 8 Mbyte QSPI Flash memory, U1
11. 32.768 KHz auxiliary crystal, Y1
12. 25 MHz main crystal, Y2
13. 1x14 pin header (2.54mm pitch), J2
14. 1x6 pin header (2.54mm pitch), J4
15. 3-pin header (2.54mm pitch), J3

16. 1x14 pin header (2.54mm pitch), J1
17. 2x6 Pmod connector, J6

Initial Delivery State

Storage device name	Content	Notes
SPI Flash OTP area	empty	-
SPI Flash	empty	-
FTDI EEPROM, U9	Programmed	FlashPro identification, should not be changed by customer

Table 1: Initial delivery state of programmable devices on the module

Boot Process

There is are no bootmode selection Microchip SmartFusion2 SoC boots always from internal configuration flash, optionally software code for the Cortex-M or soft CPU can be placed to eNVM.

Signals, Interfaces and Pins

I/Os on Pin Headers and Connectors

I/O signals of the FPGA SoC's I/O banks connected to the board's pin headers and connectors:

Bank	Connector Designator	I/O Signal Count	Bank Voltage	Notes
1	J1	1 I/O's	3.3V	-
1	J2	4 I/O's	3.3V	2 I/O's of bank 1 can be pulled-up to 3.3V (4K7 resistors) with 2 I/O's of Bank 7 or pins can be shared.
2	J1	13 I/O's	3.3V	-
2	J2	5 I/O's	3.3V	-
2	J6	8 /O's	3.3V	Pmod Connector.
3	J4	5 I/O's	3.3V	JTAG interface.
4	J3	2 I/O's	3.3V	I/O's (PROBE A, B) are dedicated to live probes.
7	J2	2 I/O's	3.3V	Those 2 I/O's are dedicated to pull-up 2 I/O's of bank 1 or pins can be shared.

Table 2: General overview of single ended I/O signals connected to pin headers and connectors

FPGA I/O banks

Bank	VCCIO	I/O's Count	Available on Connectors	Notes
1	3.3V	14	5	6 I/O's connected to FTDI chip, 1 I/O used for user button S2, 2 I/O's connected to red user LEDs D2 and D10.
2	3.3V	37	26	6 I/O's user for QSPI Flash, 5 I/O's connected to red user LEDs D3 ... D7.
3	3.3V	5	5	Bank 3 is dedicated to JTAG interface.

4	3.3V	24	2	2 I/O's are dedicated to live probes, all other I/O's are used as memory interface.
7	3.3V	22	2	2 I/O's available on header J2, 2 I/O's connected to red user LEDs D8 and D9, all other I/O's are used as memory interface.

Table 3: General overview of FPGA I/O banks

JTAG Interface

JTAG access to the FPGA SoC device U5 is provided through Micro USB2 B connector J9. The JTAG interface is implemented with FTDI FT2232H USB2 to JTAG/UART bridge IC U3.

Optionally 1x6 male pin header J4 can be fitted on board for access to the JTAG interface on board. The pin assignment of header J4 is shown on table below:

JTAG Signal	Pin on Header J4	Note
TCK	3	-
TDI	5	-
TDO	4	-
TMS	6	-
JTAGSEL	2	can be left open for normal operation

Table 4: optional JTAG header

QSPI Interface

The QSPI interface of the FPGA device is routed to and used by the on-module QSPI flash IC U1:

SD IO Signal Schematic Name	FPGA I/O	Flash IC U1 Pin	Note
F_CS	Bank 2, pin K15	1	QSPI chip select
F_CLK	Bank 2, pin P18	6	QSPI clock
F_DI	Bank 2, pin P19	5	QSPI data
F_DO	Bank 2, pin K16	2	QSPI data
F_D2	Bank 2, pin J18	3	QSPI data
F_D3	Bank 2, pin N19	7	QSPI data

Table 5: QSPI interface signals

Note: On-board SPI Flash is connected to regular FPGA I/O pins, access to it is only possible when using custom SPI flash IP core or via MSS subsystem SPI when it is connected via fabric to those pins. There is no automatic boot from this flash.

On-board Peripherals

Quad SPI Flash Memory

On-module QSPI flash memory (U7) is provided by Winbond Serial Flash Memory W74M64FV with 64 MBit (8 MByte) storage capacity.

SDRAM

The TEM0001 FPGA module is equipped with a Winbond W9864G6JT 64 MBit (8 MByte) SDRAM chip U2.

FTDI FT2232H IC

FTDI FT2232H Channel A works as JTAG interface compatible to Libero tools. Channel B is connected to FPGA pins with direct access to MSS UART peripheral.

The configuration of FTDI FT2232H is pre-programmed to the EEPROM U9 to make it work as FlashPro5 interface for Libero tools.

System Clock Oscillator

The FPGA SoC module has following reference clocking signals provided by on-board oscillators:

Clock Source	Schematic Name	Frequency	Clock Input Destination
MEMS Oscillator, U7	CLK12M	12.0000 MHz	FTDI FT2232 U3, pin 3; FPGA SoC bank 2, pin N16
Crystal Oscillator, Y1	-	32.768 KHz	FPGA SoC U5 auxiliary clock, pins W17/Y17
Quartz Crystal Oscillator, Y2	-	25.000 MHz	FPGA SoC U5 main clock, pins W18/Y18

Table 6: Clock sources overview

On-board LEDs

There are 10 LEDs fitted on the FPGA module board. The LEDs are user configurable to indicate for example any system status.

LED	Color	Signal Schematic Name	FPGA	Notes
D1	Green	-	-	Indicating 3.3V board supply voltage
D2	Red	LED1	E18	user
D3	Red	LED2	R17	user
D4	Red	LED3	R18	user
D5	Red	LED4	T18	user
D6	Red	LED5	U18	user
D7	Red	LED6	R16	user
D8	Red	LED7	E1	user
D9	Red	LED8	D2	user
D10	Red	USER_LED	G17	user

Table 7: LEDs of the module

Push Buttons

The TEM0001 FPGA module is equipped with two push buttons S1 and S2:

Button	Signal Schematic Name	FPGA	Notes
S1	USER_BTN	B19	user configurable
S2	RESET	U17	system reset (reconfiguration)

Table 8: Push buttons of the module

Connectors

All connectors are are for 100mil headers, all connector locations are in 100mil (2.54mm) grid. The module's PCB provides footprints to mount and solder optional pin headers, if those are not factory-fitted on module.

Power and Power-On Sequence

To power-up a module, power supply with minimum current capability of 1A is recommended.

Power Supply

The FPGA module can be power-supplied through Micro USB2 connector J9 with supply voltage 'USB-VBUS' or alternative through pin header J2 with supply voltage 'VIN'.

The TEM0001 module needs one single power supply of 5.0V nominal.

There are following dependencies how the initial voltage of the extern power supply is distributed to the on-board DCDC converters:

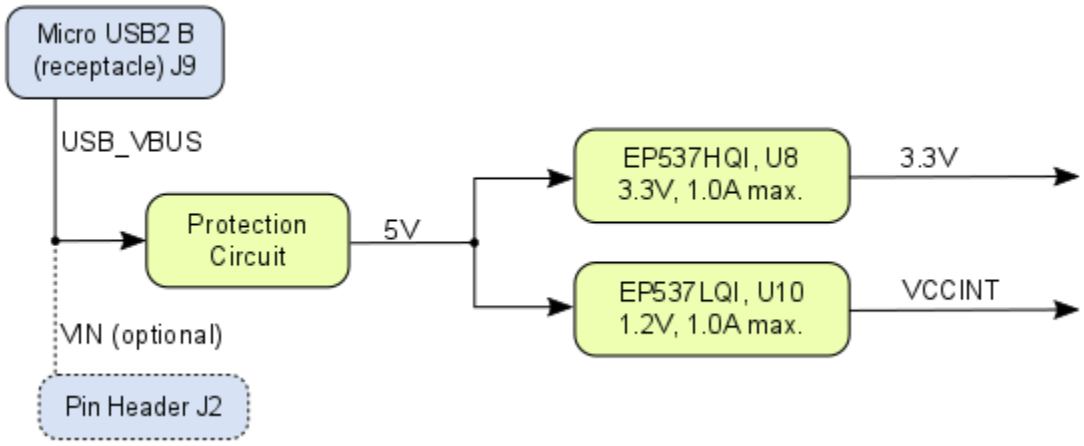

Figure 3: Power Distribution Diagram

Power Consumption

FPGA	Design	Typical Power, 25C ambient
Mircosemi SmartFusion2 FPGA SoC M2S010-VFG400	Not configured	TBD*

Table 9: Module power consumption

*TBD - To Be Determined.

Actual power consumption depends on the FPGA design and ambient temperature.

Power-On Sequence

There is no specific or special power-on sequence, just one single power source is needed.

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference document
VIN supply voltage (5.0V nominal)	-0.3	6.0	V	EP53A7HQI / EP53A7LQI datasheet
I/O Input voltage for FPGA I/O bank	-0.3	3.63	V	Microsemi datasheet DS0128
Storage Temperature	-40	+90	°C	LED R6C-AL1M2VY/3T datasheet

Table 10: Absolute maximum ratings

Recommended Operating Conditions

Parameter	Min	Max	Units	Reference document
VIN supply voltage (5.0V nominal)	4.75	5.25	V	same as USB-VBUS specification
I/O Input voltage for FPGA I/O bank	0	3.45	V	Microsemi datasheet DS0128
Operating temperature range	0	+70	°C	Winbond datasheet W9864G6GT

Table 11: Recommended operating conditions

⚠ Please check Microsemi datasheet DS0128 for complete list of absolute maximum and recommended operating ratings for the FPGA device.

Physical Dimensions

Please note that two different units are used on the figures below, SI system millimeters (mm) and imperial system thousandths of an inch(mil). This is because of the 100mil pin headers used, see also explanation below. To convert mils to millimeters and vice versa use formula 100mil's = 2,54mm.

- Board size: PCB 25mm × 61,5mm. Notice that some parts the are hanging slightly over the edge of the PCB like the the Micro USB2 B connector, which determine the total physical dimensions of the carrier board. Please download the assembly diagram for exact numbers.
- PCB thickness: ca. 1.65mm
- Highest part on the PCB without fitted headers and connectors is the Micro USB2 B connector, which has an approximately hight of 3 mm. Please download the step model for exact numbers.

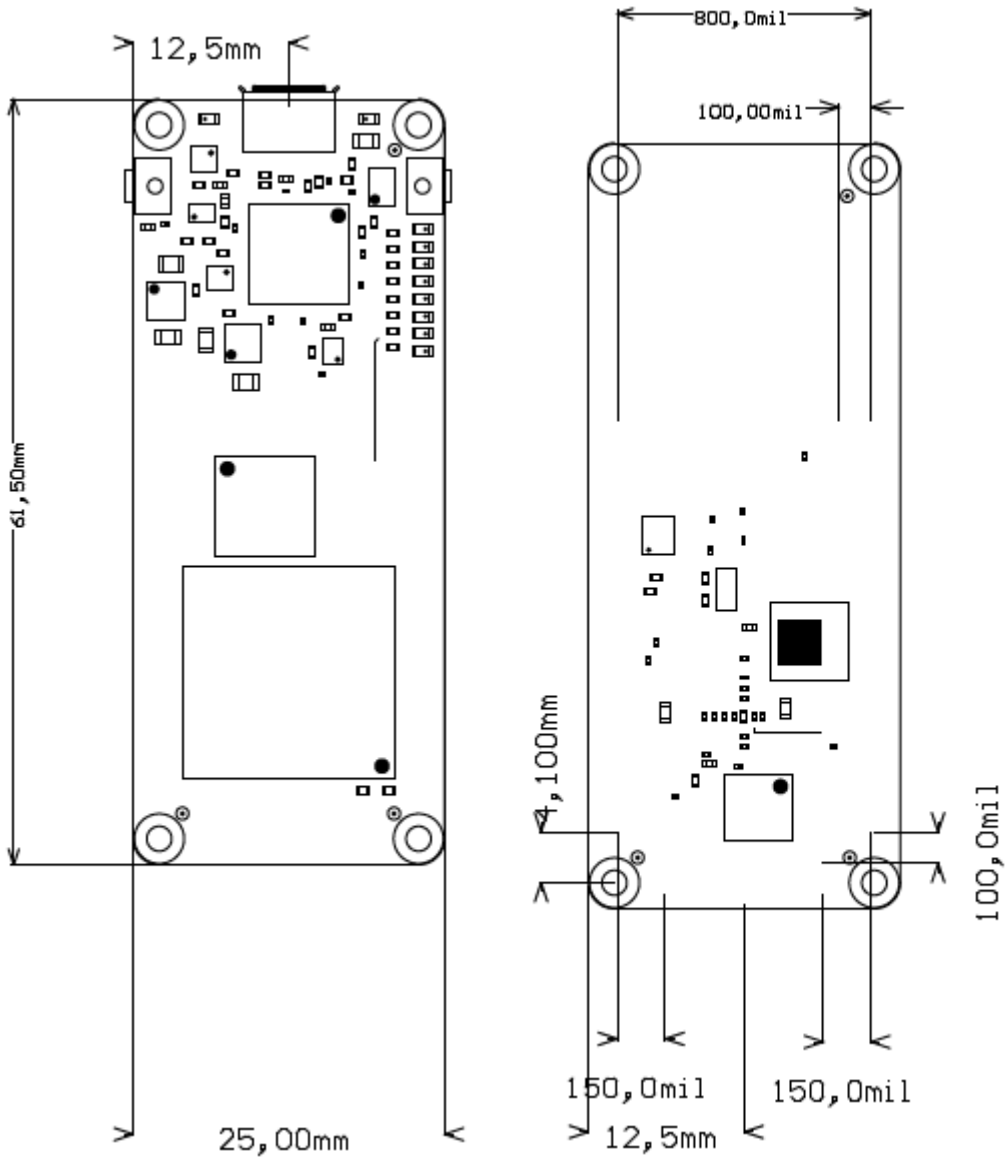

Figure 4: Module physical dimensions drawing

Revision History

Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
-	01	• First Production Release	-	TEM0001-01

Table 12: Module hardware revision history

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.

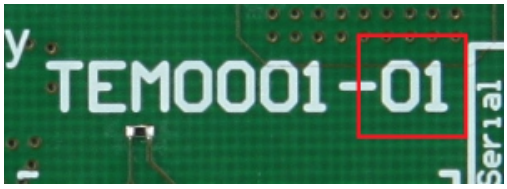

Figure 5: Module hardware revision number

Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] Unknown macro: 'metadata'	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• fixed typographical and other mistakes
11 Dec 2018	v.33	Antti Lukats	• change documentation
2018-04-17	v.31	Ali Naseri	• initial release

Table 13: Document change history

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Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]