TE0784 TRM

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Overview

The Trenz Electronic TE0784 is a high-performance, industrial-grade SoM (System on Module) with industrial temperature range based on Xilinx Zynq-7000 SoC XC7Z045-2FFG900I.

These highly integrated modules with an economical price-performance-ratio have a form-factor of 8,5 x 8,5 cm and are rugged for industrial applications.

All parts cover at least industrial temperature range of -40°C to +85°C. The module operating temperature range depends on customer design and cooling solution. Please contact us for options and for modified PCB-equipping due increasing cost-performance-ratio and prices for large-scale order.

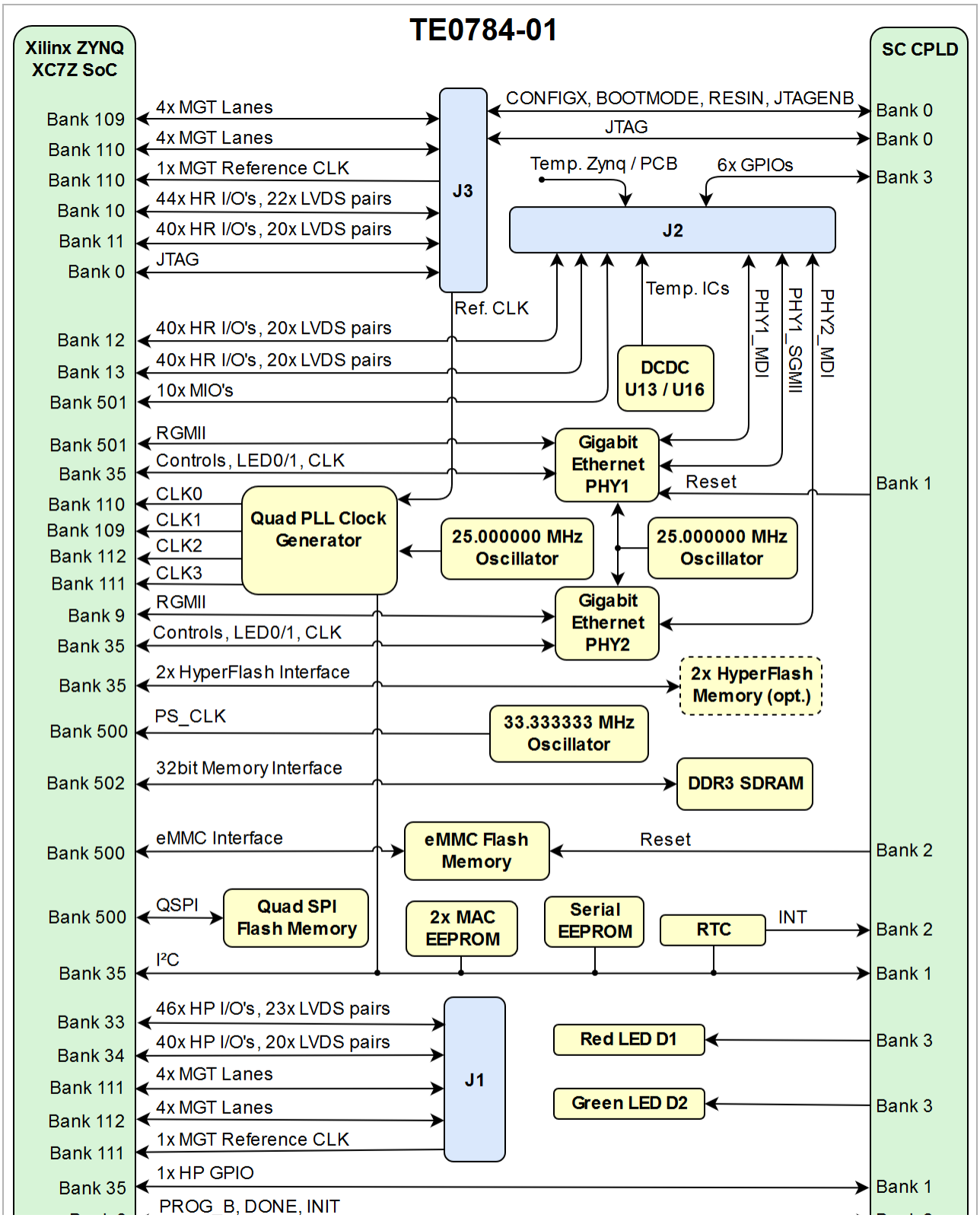
Key Features

- Xilinx Zynq-7000 XC7Z035, XC7Z045 or XC7Z100 SoC
- Rugged for shock and high vibration
- Large number of configurable I/Os are provided via rugged high-speed stacking strips
- Dual ARM Cortex-A9 MPCore
    - 1 GByte RAM (32bit wide DDR3)
    - 32 MByte QSPI Flash memory
    - 2 x Gigabit (10/100/1000 Mbps) Ethernet transceiver PHY
    - 4 GByte eMMC (optional up to 64 GByte)
- 2 x MAC-address EEPROMs
- Optional 2x 64 MByte HyperFLASH or 2x 8 MByte HyperRAM (max 2x 32 MByte HyperRAM)
- Temperature compensated RTC (real-time clock)
- Si5338A programmable quad PLL clock generator for GTX transceiver clocks
- Plug-on module with 3 x 160-pin high-speed strips
    - 16 GTX high-performance transceiver
    - 2x GT transceiver clock inputs
    - 254 FPGA I/O's (125 LVDS pairs)
- On-board high-efficiency switch-mode DC-DC converters
- System management
- eFUSE bit-stream encryption
- AES bit-stream encryption
- Evenly-spread supply pins for good signal integrity
- User LED

Assembly options for cost or performance optimization available upon request.

Additional assembly options are available for cost or performance optimization upon request.

Block Diagram


TE0784-01
Xilinx ZYNQ XC7Z SoC
SC CPLD
Bank 109
Bank 110
Bank 110
Bank 10
Bank 11
Bank 0
Bank 12
Bank 13
Bank 501
Bank 501
Bank 35
Bank 110
Bank 109
Bank 112
Bank 111
Bank 9
Bank 35
Bank 35
Bank 500
Bank 502
Bank 500
Bank 500
Bank 35
Bank 33
Bank 34
Bank 111
Bank 112
Bank 111
Bank 35
4x MGT Lanes
4x MGT Lanes
1x MGT Reference CLK
44x HR I/O's, 22x LVDS pairs
40x HR I/O's, 20x LVDS pairs
JTAG
40x HR I/O's, 20x LVDS pairs
40x HR I/O's, 20x LVDS pairs
10x MIO's
RGMII
Controls, LED0/1, CLK
CLK0
CLK1
CLK2
CLK3
RGMII
Controls, LED0/1, CLK
2x HyperFlash Interface
PS_CLK
32bit Memory Interface
eMMC Interface
QSPI
I²C
46x HP I/O's, 23x LVDS pairs
40x HP I/O's, 20x LVDS pairs
4x MGT Lanes
4x MGT Lanes
1x MGT Reference CLK
1x HP GPIO
PROG_B, DONE, INIT
J3
J1
J2
CONFIGX, BOOTMODE, RESIN, JTAGENB
JTAG
Temp. Zynq / PCB
6x GPIOs
Ref. CLK
Temp. ICs
PHY1_MDI
PHY1_SGMII
PHY2_MDI
DCDC U13 / U16
Gigabit Ethernet PHY1
Gigabit Ethernet PHY2
Reset
Quad PLL Clock Generator
25.000000 MHz Oscillator
25.000000 MHz Oscillator
2x HyperFlash Memory (opt.)
33.333333 MHz Oscillator
DDR3 SDRAM
eMMC Flash Memory
Reset
Quad SPI Flash Memory
2x MAC EEPROM
Serial EEPROM
RTC
INT
Red LED D1
Green LED D2
Bank 0
Bank 0
Bank 3
Bank 1
Bank 2
Bank 2
Bank 1
Bank 3
Bank 3
Bank 1

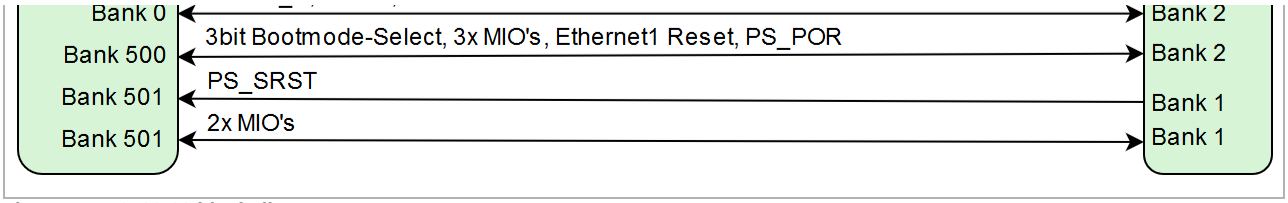


Figure 1: TE0782-02 block diagram

Main Components

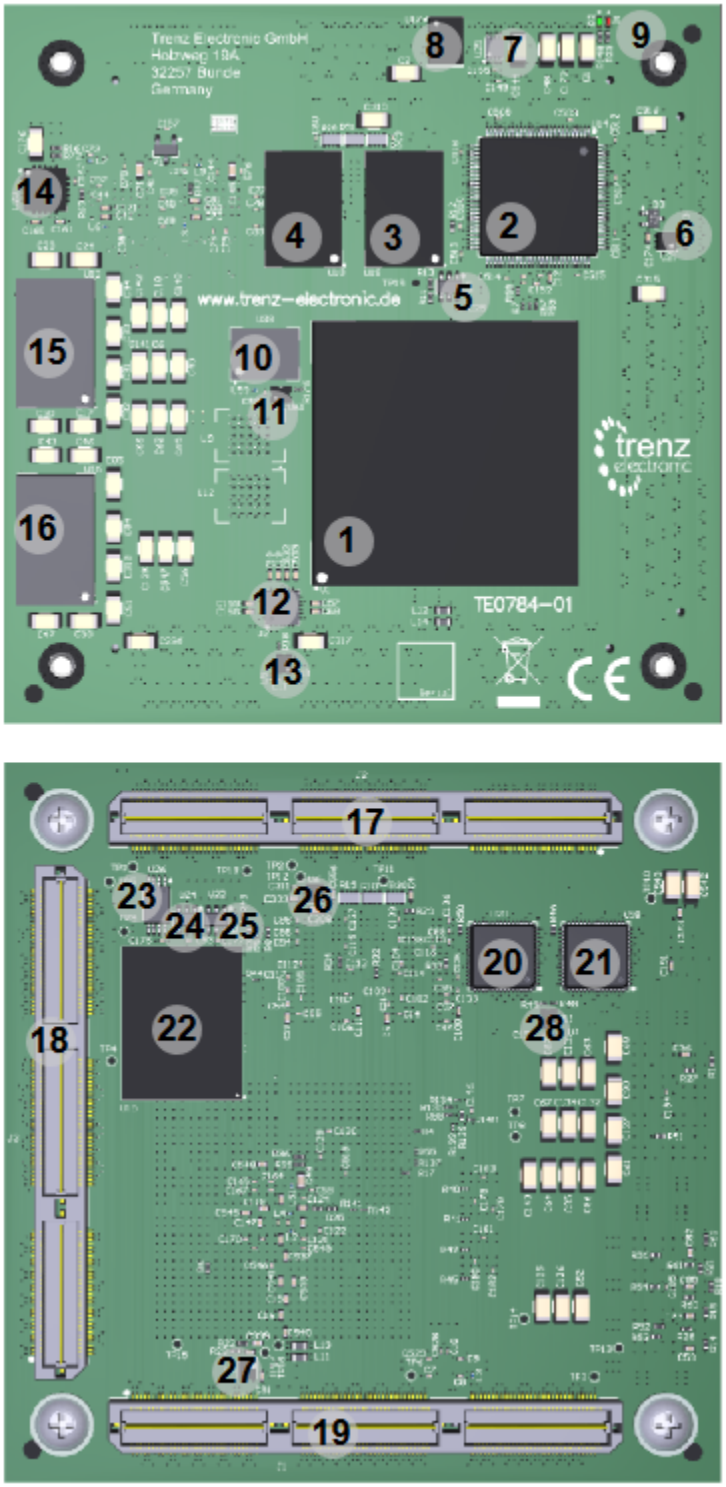


Figure 2: TE0782-02 main components

1. Xilinx Zynq-7000 SoC, U1
2. Lattice Semiconductor MachXO2 1200HC CPLD, U14
3. 4Gbit DDR3L SDRAM, U19
4. 4Gbit DDR3L SDRAM, U10
5. TI TPS3106 voltage monitor circuit, U4
6. TI TPS78018 LDO, U21
7. I²C voltage translator, U25
8. Intersil ISL12020MIRZ Real Time Clock, U17
9. Red LED D1, Green LED D2
10. 32 MByte QSPI Flash memory, U38
11. SiTime SiT8008 33.333333 MHz oscillator, U61
12. SI5338A programmable quad PLL clock generator, U2
13. SiTime SiT8008 25.000000 MHz oscillator, U3
14. TPS74801 LDO @1.5V, U23
15. LT quad 4A PowerSoC DC-DC converter (@1.0V), U13
16. LT quad 4A PowerSoC DC-DC converter (@3.3V, @1,8V, @1.2V_MGT, @1.0V_MGT), U16
17. Samtec ASP-122952-01 160-pin stacking strip (2 rows a 80 positions), J2
18. Samtec ASP-122952-01 160-pin stacking strip (2 rows a 80 positions), J3
19. Samtec ASP-122952-01 160-pin stacking strip (2 rows a 80 positions), J1
20. Marvell Alaska 88E1512 Gigabit Ethernet PHY, 20
21. Marvell Alaska 88E1512 Gigabit Ethernet PHY, U18
22. Micron Technology 4 GByte eMMC, U15
23. Microchip 128Kbit I²C EEPROM, U26
24. Microchip 2Kbit I²C MAC EEPROM, U24
25. Microchip 2Kbit I²C MAC EEPROM, U22
26. TPS51206 DDR reference voltage and termination regulator, U6
27. TPS799 LDO @1.8V_MGT, U5
28. SiTime SiT8008 25.000000 MHz oscillator, U11

Initial Delivery State

Storage device name	Content	Notes
24LC128-I/ST	not programmed	User content
24AA025E48 EEPROM's	User content not programmed	Valid MAC Address from manufacturer
Si5338A OTP Area	not programmed	-
eMMC Flash Memory	Empty, not programmed	Except serial number programmed by flash vendor
SPI Flash OTP Area	Empty, not programmed	Except serial number programmed by flash vendor
SPI Flash Quad Enable bit	Programmed	-
SPI Flash main array	demo design	-
HyperFlash Memory	not programmed	-
eFUSE USER	Not programmed	-
eFUSE Security	Not programmed	-

Table 1: Initial delivery state of programmable devices on the module

Boot Process

4 of the 7 boot mode strapping pins (MIO2 ... MIO8) of the Xilinx Zynq-7000 SoC device are hardware programmed on the board, 3 of them are set by the SC CPLD firmware. The boot strapping pins are evaluated by the Zynq device soon after the 'PS_POR' signal is deasserted to begin the boot process (see section "Boot Mode Pin Settings" of Xilinx manual UG585).

The TE0784 board is programmed in the SC CPLD firmware to boot initially from the on-board QSPI Flash memory U38. See section bootmode in the TE0784 SC CPLD reference Wiki page.

The JTAG interface of the module is provided for storing the data to the QSPI Flash memory through the Zynq-7000 device.

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

Zynq-7000 SoC's I/O banks signals connected to the B2B connectors:

Bank	Type	B2B Connector	I/O Signal Count	Differential	Voltage	Notes
10	HR	J3	44	22	User	Max voltage 3.3V
11	HR	J3	40	20	User	Max voltage 3.3V
12	HR	J2	40	20	User	Max voltage 3.3V
13	HR	J2	40	20	User	Max voltage 3.3V
33	HP	J1	48	23	User	Max voltage 1.8V
34	HP	J1	42	20	User	Max voltage 1.8V

Table 2: General overview of board to board I/O signals

For detailed information about the pin-out, please refer to the Pin-out table.

MGT Lanes

The Xilinx Zynq-7000 SoC used on the TE0784 module has 16 MGT transceiver lanes. All of them are wired directly to B2B connectors J1 and J3. MGT (Multi Gigabit Transceiver) lane consists of one transmit and one receive (TX/RX) differential pairs, four signals total per one MGT lane with data transmission rates up to 12.5Gb/s per lane (Xilinx GTX transceiver). Following table lists lane number, FPGA bank number, transceiver type, signal schematic name, board-to-board pin connection and FPGA pins connection:

Bank	Type	Lane	Signal Name	B2B Pin	FPGA Pin
109	GTX	0	• MGT_RX0_P • MGT_RX0_N • MGT_TX0_P • MGT_TX0_N	• J3-32 • J3-30 • J3-31 • J3-29	• MGTXRXP0_109 • MGTXRXN0_109 • MGTXTXP0_109 • MGTXTXN0_109
		1	• MGT_RX1_P • MGT_RX1_N • MGT_TX1_P • MGT_TX1_N	• J3-28 • J3-26 • J3-27 • J3-25	• MGTXRXP1_109 • MGTXRXN1_109 • MGTXTXP1_109 • MGTXTXN1_109
		2	• MGT_RX2_P • MGT_RX2_N • MGT_TX2_P • MGT_TX2_N	• J3-24 • J3-22 • J3-23 • J3-21	• MGTXRXP2_109 • MGTXRXN2_109 • MGTXTXP2_109 • MGTXTXN2_109

		3	• MGT_RX3_P • MGT_RX3_N • MGT_TX3_P • MGT_TX3_N	• J3-20 • J3-18 • J3-19 • J3-17	• MGTXRXP3_109 • MGTXRXN3_109 • MGTXTXP3_109 • MGTXTXN3_109
110	GTX	0	• MGT_RX4_P • MGT_RX4_N • MGT_TX4_P • MGT_TX4_N	• J3-16 • J3-14 • J3-15 • J3-13	• MGTXRXP0_110 • MGTXRXN0_110 • MGTXTXP0_110 • MGTXTXN0_110
		1	• MGT_RX5_P • MGT_RX5_N • MGT_TX5_P • MGT_TX5_N	• J3-12 • J3-10 • J3-11 • J3-9	• MGTXRXP1_110 • MGTXRXN1_110 • MGTXTXP1_110 • MGTXTXN1_110
		2	• MGT_RX6_P • MGT_RX6_N • MGT_TX6_P • MGT_TX6_N	• J3-8 • J3-6 • J3-7 • J3-5	• MGTXRXP2_110 • MGTXRXN2_110 • MGTXTXP2_110 • MGTXTXN2_110
		3	• MGT_RX7_P • MGT_RX7_N • MGT_TX7_P • MGT_TX7_N	• J3-4 • J3-2 • J3-3 • J3-1	• MGTXRXP3_110 • MGTXRXN3_110 • MGTXTXP3_110 • MGTXTXN3_110
111	GTX	0	• MGT_RX8_P • MGT_RX8_N • MGT_TX8_P • MGT_TX8_N	• J1-1 • J1-3 • J1-2 • J1-4	• MGTXRXP0_111 • MGTXRXN0_111 • MGTXTXP0_111 • MGTXTXN0_111
		1	• MGT_RX9_P • MGT_RX9_N • MGT_TX9_P • MGT_TX9_N	• J1-5 • J1-7 • J1-6 • J1-8	• MGTXRXP1_111 • MGTXRXN1_111 • MGTXTXP1_111 • MGTXTXN1_111
		2	• MGT_RX10_P • MGT_RX10_N • MGT_TX10_P • MGT_TX10_N	• J1-9 • J1-11 • J1-10 • J1-12	• MGTXRXP2_111 • MGTXRXN2_111 • MGTXTXP2_111 • MGTXTXN2_111
		3	• MGT_RX11_P • MGT_RX11_N • MGT_TX11_P • MGT_TX11_N	• J1-13 • J1-15 • J1-14 • J1-16	• MGTXRXP3_111 • MGTXRXN3_111 • MGTXTXP3_111 • MGTXTXN3_111
112	GTX	0	• MGT_RX12_P • MGT_RX12_N • MGT_TX12_P • MGT_TX12_N	• J1-17 • J1-19 • J1-18 • J1-20	• MGTXRXP0_112 • MGTXRXN0_112 • MGTXTXP0_112 • MGTXTXN0_112
		1	• MGT_RX13_P • MGT_RX13_N • MGT_TX13_P • MGT_TX13_N	• J1-21 • J1-23 • J1-22 • J1-24	• MGTXRXP1_112 • MGTXRXN1_112 • MGTXTXP1_112 • MGTXTXN1_112

		2	• MGT_RX14_P • MGT_RX14_N • MGT_TX14_P • MGT_TX14_N	• J1-25 • J1-27 • J1-26 • J1-28	• MGTXRXP2_112 • MGTXRXN2_112 • MGTXTXP2_112 • MGTXTXN2_112
		3	• MGT_RX15_P • MGT_RX15_N • MGT_TX15_P • MGT_TX15_N	• J1-29 • J1-31 • J1-30 • J1-32	• MGTXRXP3_112 • MGTXRXN3_112 • MGTXTXP3_112 • MGTXTXN3_112

Table 3: MGT lanes

There are 2 clock sources for the GTX transceivers. MGT_CLK1 and MGT_CLK4 are connected directly to B2B connector J3 and J1, so the clock can be provided by the carrier board. Clocks MGT_CLK0, MGT_CLK3, MGT_CLK5 and MGT_CLK6 are provided by the on-board clock generator (U2). As there are no capacitive coupling of the data and clock lines that are connected to the connectors, these may be required on the user's PCB depending on the application.

Bank	Type	Clock signal	Source	FPGA Pin	Notes
109	GTX	MGT_CLK3_P	U2, CLK3A	MGTREFCLK1P_109, AF10	Supplied by on-board Si5338A
		MGT_CLK3_N	U2, CLK3B	MGTREFCLK1N_109, AF9	
110	GTX	MGT_CLK0_P	U2, CLK2A	MGTREFCLK0P_110, AA8	Supplied by on-board Si5338A
		MGT_CLK0_N	U2, CLK2B	MGTREFCLK0N_110, AA7	
		MGT_CLK1_N	J3-39	MGTREFCLK1P_110, AC8	Supplied by B2B connector J3
		MGT_CLK1_P	J3-37	MGTREFCLK1N_110, AA7	
111	GTX	MGT_CLK4_N	J1-40	MGTREFCLK0P_111, U8	Supplied by B2B connector J1
		MGT_CLK4_P	J1-38	MGTREFCLK0N_111, U7	
		MGT_CLK5_P	U2, CLK1A	MGTREFCLK1P_111, W8	Supplied by on-board Si5338A
		MGT_CLK5_N	U2, CLK1B	MGTREFCLK1N_111, W7	
112	GTX	MGT_CLK6_P	U2, CLK0A	MGTREFCLK0P_112, N8	Supplied by on-board Si5338A
		MGT_CLK6_N	U2, CLK0B	MGTREFCLK0N_112, N7	

Table 4: MGT reference clock sources

JTAG Interface

JTAG access to the Xilinx Zynq-7000 is provided through B2B connector J3.

JTAG Signal	B2B Connector Pin
TMS	J3-142
TDI	J3-147
TDO	J3-148
TCK	J3-141

Table 5: Zynq JTAG interface signals

JTAG access to the LCMXO2-1200HC System Controller CPLD U14 is provided through B2B connector J3.

JTAG Signal	B2B Connector Pin
M_TMS	J3-82
M_TDI	J3-87
M_TDO	J3-88
M_TCK	J3-81

Table 6: System Controller CPLD JTAG interface signals

Pin J3-136 'JTAGENB' of B2B connector J3 is used to access the JTAG interface of the SC CPLD. Set high to program the System Controller CPLD via JTAG interaface.

System Controller CPLD I/O Pins

Special purpose pins are connected to System Controller CPLD and have following default configuration:

Pin Name	Direction	Function	Default Configuration
BOOTMODE	in	in	signal forwarded to MIO9 and currently used as UART RX line
CONFIGX	in	out	signal forwarded to MIO8 and currently used as UART TX line
RESIN	in	nRESET	external Board Reset
M_TDO	out	CPLD JTAG interface	-
M_TDI	in		
M_TCK	in		
M_TMS	in		
JTAGENB	in	enable JTAG	pull high for programming SC CPLD firmware
I2C_SCL	in / out	I²C data line	I²C bus of board
I2C_SDA	in	I²C clock	
CPLD_IO	in / out	user GPIO	currently not used
ETH1_RESET	out	reset GbE PHY U18	see current SC CPLD firmware
RTC_INT	in	interrupt	interrupt from RTC
PS_SRST	out	Zynq control signal	reset PS of Zynq-7000 SoC
DONE	in		PL configuration completed
PROG_B	out		PL configuration reset signal
INIT	in		Low active FPGA initialization pin or configuration error signal
PS_POR	out		PS power-on reset
BM0/MIO5	out		Bootmode Pins
BM2/MIO4	out		currently configured in SC CPLD firmare to boot from QSPI Flash
BM3/MIO2	out		
MIO8	in	user MIO pins	currently used as UART interface
MIO9	out		

PS_MIO50	in / out		availabe to user
PS_MIO51	in / out		
OTG-RST33 (MIO0)	in / out		
MMC_RST	out	Reset MMC Flash	see current SC CPLD firmware
ETH1-RESET33	in	reset GbE PHY U18	reset signal from Zynq-7000 level shifted to 1.8V
LED1 ... LED2	out	LED status signal	see current CPLD firmware
CPLD_GPIO0 ... CPLD_GPIO5	in / out	user GPIO	currently not used
EN_1V	out	Power control	enable signal DCDC U13 '1V'
PG_1V	in		power good signal DCDC U13 '1V'
EN_1.0V_MGT	out		enable signal DCDC U16 '1.0V_MGT'
PG_1.0V_MGT	in		power good signal DCDC U16 '1.0V_MGT'
EN_1.2V_MGT	out		enable signal DCDC U16 '1.2V_MGT'
PG_1.2V_MGT	in		power good DCDC U16 '1.2V_MGT'
EN_1.8V	out		enable signal DCDC U16 '1.8V'
PG_1.8V	in		power good signal DCDC U16 '1.8V'
EN_3.3V	out		enable signal DCDC U16 '3.3V'
PG_3.3V	in		power good signal DCDC U16 '3.3V'
PG_1V5	in		power good signal DCDC U23 '1.5V'
PS_POR_RST	in		Reset signal from voltage monitor circuit

Table 7: System Controller CPLD special purpose pins.

See also TE0784 CPLD reference Wiki page.

Default PS MIO Mapping

MIO	Function	Connected to
0	user dependent	SC CPLD bank 2
1	QSPI0	SPI Flash-CS
2	QSPI0	SPI Flash-DQ0
3	QSPI0	SPI Flash-DQ1
4	QSPI0	SPI Flash-DQ2
5	QSPI0	SPI Flash-DQ3
6	QSPI0	SPI Flash-SCK
7	Ethernet PHY1 Reset	SC CPLD (used level translator)
8	UART TX	output, muxed to B2B by the SC CPLD
9	UART RX	input, muxed to B2B by the SC CPLD
10	SDIO1 D0	eMMC DAT0
11	SDIO1 CMD	eMMC CMD
12	SDIO1 CLK	eMMC CLK

13	SDIO1 D1	eMMC DAT1
14	SDIO1 D2	eMMC DAT2
15	SDIO1 D3	eMMC DAT3
16..27	ETH0	Ethernet RGMII PHY
28..39	-	not connected
40...45	6x user MIO's (usable as SDIO)	B2B connector J2
49...49	4x user MIO's	B2B connector J2
50...51	2x user MIO's	SC CPLD bank 1
52	ETH0 MDC	-
53	ETH0 MDIO	-

Table 8: Zynq PS MIO mapping

Gigabit Ethernet

The TE0784 is equipped with two Marvell Alaska 88E1512 Gigabit Ethernet PHYs (U18 (ETH1) and U20 (ETH2)). The transceiver PHY of ETH1 is connected to the Zynq PS Ethernet GEM0. The I/O Voltage is fixed at 1.8V for HSTL signaling.

RGMII interface of ETH2 is connected to PL bank 9 of Zynq SoC.

The control lines of both PHYs are connected to PL bank 35.

The reference clock input for both PHYs is supplied from an on board 25MHz oscillator (U11), the 125MHz output clock of both PHYs are connected to PL bank 35.

ETH1 PHY connection:

PHY PIN	Zynq PS / PL	System Controller CPLD	Notes
MDC/MDIO	MIO52, MIO53	-	-
LED0	Bank 35, Pin B12	-	-
LED1	Bank 35, Pin C12	-	-
Interrupt	Bank 35, Pin A15	-	-
CONFIG	Bank 35, Pin F14	-	When pin connected to GND, PHY Address is strapped to 0x00 by default
RESETn	-	Pin 53	ETH1_RESET33 (MIO7) -> SC CPLD -> ETH1_RESET
RGMII	MIO16..MIO27		-
MDI	-	-	on B2B J2 connector

Table 9: General overview of the Gigabit Ethernet1 PHY signals

ETH2 PHY connection:

PHY PIN	Zynq PS / PL	System Controller CPLD	Notes
MDC/MDIO	Bank 35, Pin C17/B17	-	-
LED0	Bank 35, Pin K15	-	-

LED1	Bank 35, Pin B16	-	-
Interrupt	Bank 35, Pin A17	-	-
CONFIG	Bank 35, Pin E15	-	When pin connected to GND, PHY Address is strapped to 0x00 by default
RESETn	Bank 35, Pin B15	-	-
RGMII	Bank 9	-	-
MDI	-	-	on B2B J2 connector

Table 10: General overview of the Gigabit Ethernet2 PHY signals

I2C Interface

The on-board I^2C components are connected to bank 35 pins L15 (I2C_SDA) and L14 (I2C_SCL).

I^2C addresses for on-board components:

Device	IC	Designator	I2C-Address	Notes
EEPROM	24LC128-I/ST	U26	0x53	user data
EEPROM	24AA025E48T-I/OT	U22	0x50	MAC address EEPROM
EEPROM	24AA025E48T-I/OT	U24	0x51	MAC address EEPROM
RTC	ISL12020MIRZ	U17	0x6F	Temperature compensated real time clock
Battery backed RAM	ISL12020MIRZ	U17	0x57	Integrated in RTC
PLL	SI5338A-B-GMR	U2	0x70	-
SC CPLD	LCMXO2-1200HC-4TG100I	U14	user	-

Table 11: Address table of the I^2C bus slave devices

Pin Definitions

Pins with names ending with _VRN and _VRP are connected to Zynq PL HP bank special purpose pins VRN/VRP and can be routed to DCI calibration resistors on the baseboard. Otherwise they are usable as general purpose I/Os.

Bank 35 has 100 ohm DCI calibration resistors installed, it is also possible to "borrow" the DCI calibration from bank 35 for banks 34 and 33. For more detailed information about the DCI check Xilinx documentation.

On-board Peripherals

System Controller CPLD

The System Controller CPLD (U14) is provided by Lattice Semiconductor LCMXO2-1200HC (MachXO2 product family). It is the central system management unit with module specific firmware installed to monitor and control various signals of the FPGA, on-board peripherals, I/O interfaces and module as a whole.

See also TE0784 CPLD reference Wiki page.

eMMC Flash Memory

eMMC Flash memory device (U15) is connected to the Zynq PS MIO bank 500 pins MIO10..MIO15. eMMC chips MTFC4GMVEA-4M IT (Flash NAND-IC 2x 16 Gbit) is used with 4 GByte of memory density.

DDR3L Memory

By default TE0782-02 module has two 16-bit wide IM (Intelligent Memory) IM4G16D3FABG-125I DDR3L SDRAM (DDR3-1600 Speedgrade) chips (U10, U19) arranged into 32-bit wide memory bus providing total of 1 GBytes of on-board RAM.

Quad SPI Flash Memory

Two quad SPI compatible serial bus flash memory for FPGA configuration file storage is provided by Spansion S25FL256SAGBHI20 (U38) with 256 Mbit (32 MByte) memory density. After configuration completes the remaining free memory can be used for application data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths to be used. The maximum data transfer rate depends on the bus width and clock frequency.

Gigabit Ethernet PHYs

On-board Gigabit Ethernet PHYs (U18, U20) are provided by Marvell Alaska 88E1512. The Ethernet PHYs' RGMII interfaces are connected to the Zynq's PS MIO bank 501 and to PL bank 9. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of both PHYs is supplied from an on-board 25.000000 MHz oscillator (U11).

MAC Address EEPROMs

Two Microchip 24AA025E48 serial EEPROMs (U22, U24) contain globally unique 48-bit node address, which are compatible with EUI-48(TM) specification. The devices are organized as two blocks of 128 x 8 Kbit memory. One of the blocks stores the 48-bit node address and is write protected, the other block is available for application use. The MAC address EEPROMS areaccessible over I^2C bus (see also section I²C interface).

Configuration EEPROM

The TE0782 board contains one EEPROM (U26) for configuration and general user purposes. The EEPROMs is provided by Microchip 24LC128-I/ST with 128 KBit memory density, the EEPROM is areaccessible over I^2C bus (see also section I²C interface).

Programmable Clock Generator

There is a Silicon Labs I^2C programmable clock generator Si5338A (U2) chip on-board. It's output frequencies can be programmed using the I^2C bus address 0x70 or 0x71. Default address is 0x70, IN4/I2C_LSB pin must be set to high for address 0x71.

A 25.000000 MHz oscillator (U3) is connected to the pin IN3 and is used to generate the output clocks. The output voltage of the oscillator is provided by the 1.8V power rail, thus making output frequency available as soon as 1.8V is present. All 4 of the Si5338 clock outputs are connected to the MGT banks of the Zynq device. It is possible to use the clocks connected to the GTR bank in the user's logic design. This is achieved by instantiating a IBUFDSGTE buffer in the design.

Once running, the frequency and other parameters can be changed by programming the device using the I^2C bus connected between the FPGA (master) and clock generator (slave). For this, proper I^2C bus logic has to be implemented in FPGA.

Signal	Frequency	Notes
IN1/IN2	user	External clock signal supply from B2B connector J3, pins J3-38 / J3-40
IN3	25.000000 MHz	Fixed input clock signal from reference clock generator SiT8008BI-73-18S-25.000000E (U3)
IN4	-	LSB of the default I^2C address, wired to ground mean address is 0x70
IN5	-	Not connected
IN6	-	Wired to ground
CLK0 A/B	-	reference clock 0 of Bank 112 GTX
CLK1 A/B	-	reference clock 1 of Bank 111 GTX

CLK2 A/B	-	reference clock 0 of Bank 110 GTX
CLK3 A/B	-	reference clock 1 of Bank 109 GTX

Table 12: General overview of the on-board quad clock generator I/O signals

Oscillators

The module has following reference clock signals provided by on-board oscillators and external source from carrier board:

Clock Source	Schematic Name	Frequency	Clock Destination
SiTime SiT8008AI oscillator, U61	PS_CLK	33.333333 MHz	Zynq SoC U1, pin A22
SiTime SiT8008BI oscillator, U21	-	25.000000 MHz	Quad PLL clock generator U2, pin 3
SiTime SiT8008AI oscillator, U7	-	52.000000 MHz	USB2 PHYs U4 and U8, pin 26
SiTime SiT8008BI oscillator, U11	-	25.000000 MHz	GbE PHYs U18 and U20, pin 34

Table 13: Reference clock signals

On-board LEDs

LED	Color	Connected to	Description and Notes
D1	Red	System Controller CPLD U14, bank 3	Exact function is defined by SC CPLD firmware
D2	Green	System Controller CPLD U14, bank 3	

Table 14: On-board LEDs

Power and Power-on Sequence

Power Supply

Power supply with minimum current capability of 4A for system startup is recommended.

Power Consumption

Power Input	Typical Current
VIN	TBD*
C3.3V	TBD*

Table 15: Power consumption

* TBD - To Be Determined soon with reference design setup.

To avoid any damage to the module, check for stabilized on-board voltages should be carried out (i.e. power good and enable signals) before powering up any Zynq's I/O bank voltages VCCO_x. All I/Os should be tri-stated during power-on sequence.

Power Distribution Dependencies

The Trenz TE0784 SoM is equipped with two quad DC-DC voltage regulators to generate required on-board voltage levels 1V, 3.3V, 1.8V, 1.2V_MGT, 1V_MGT. Additional voltage regulators are used to generate voltages 1.5V, VTT, VTTREF and 1.8V_MGT.

The power supply voltage 'C3.3V' of System Controller CPLD of the SoM have to be externally supplied with 3.3V nominal.

There are following dependencies how the initial voltages of the power rails on the B2B connectors are distributed to the on-board DC-DC converters, which power up further DC-DC converters and the particular on-board voltages:

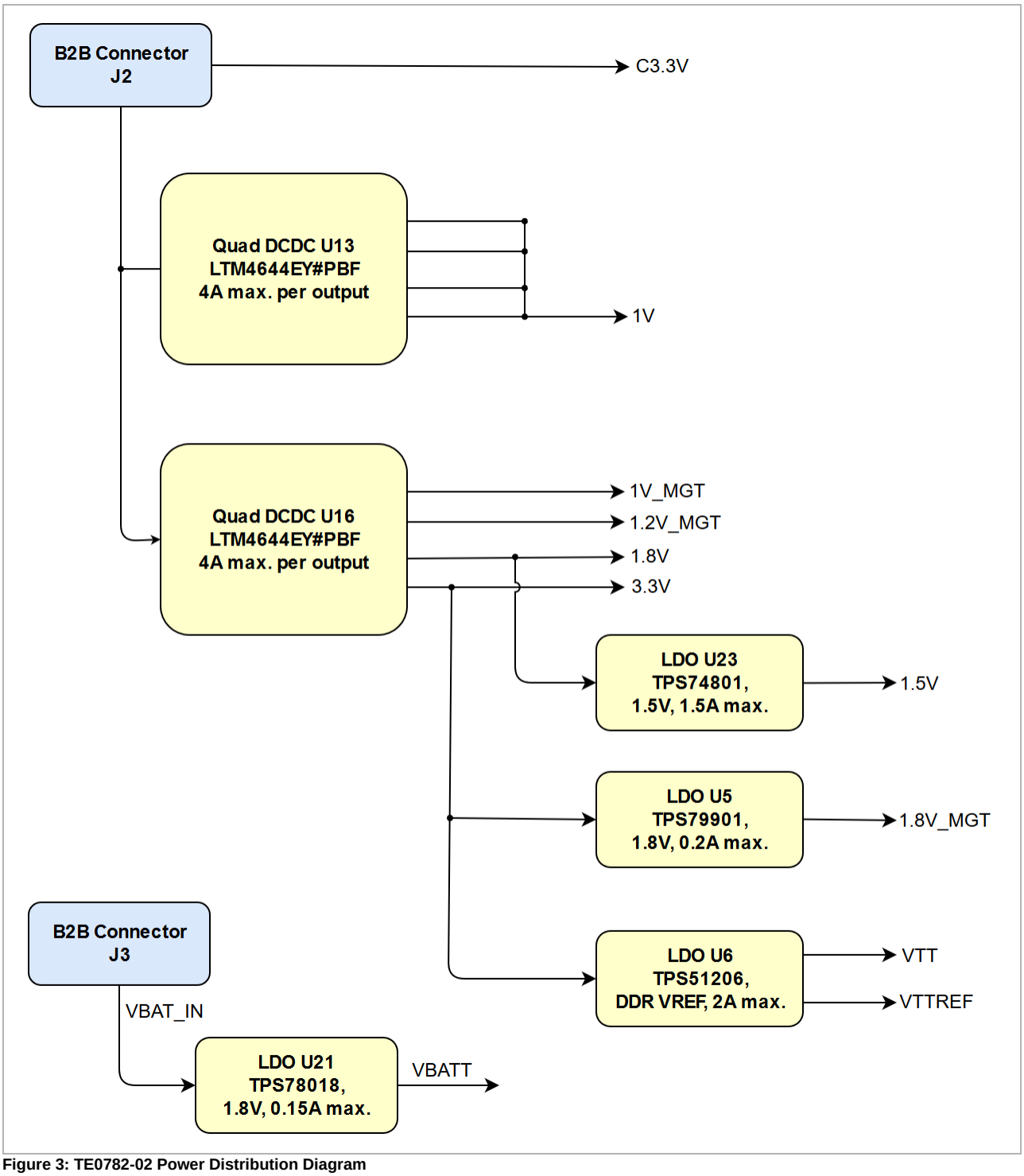


Figure 3: TE0782-02 Power Distribution Diagram

See also Xilinx datasheet DS191 for additional information. User should also check related base board documentation when intending base board design for TE0782 module.

Power-On Sequence

Power-on sequence is handled by the System Controller CPLD using "Power good"-signals from the voltage regulators:

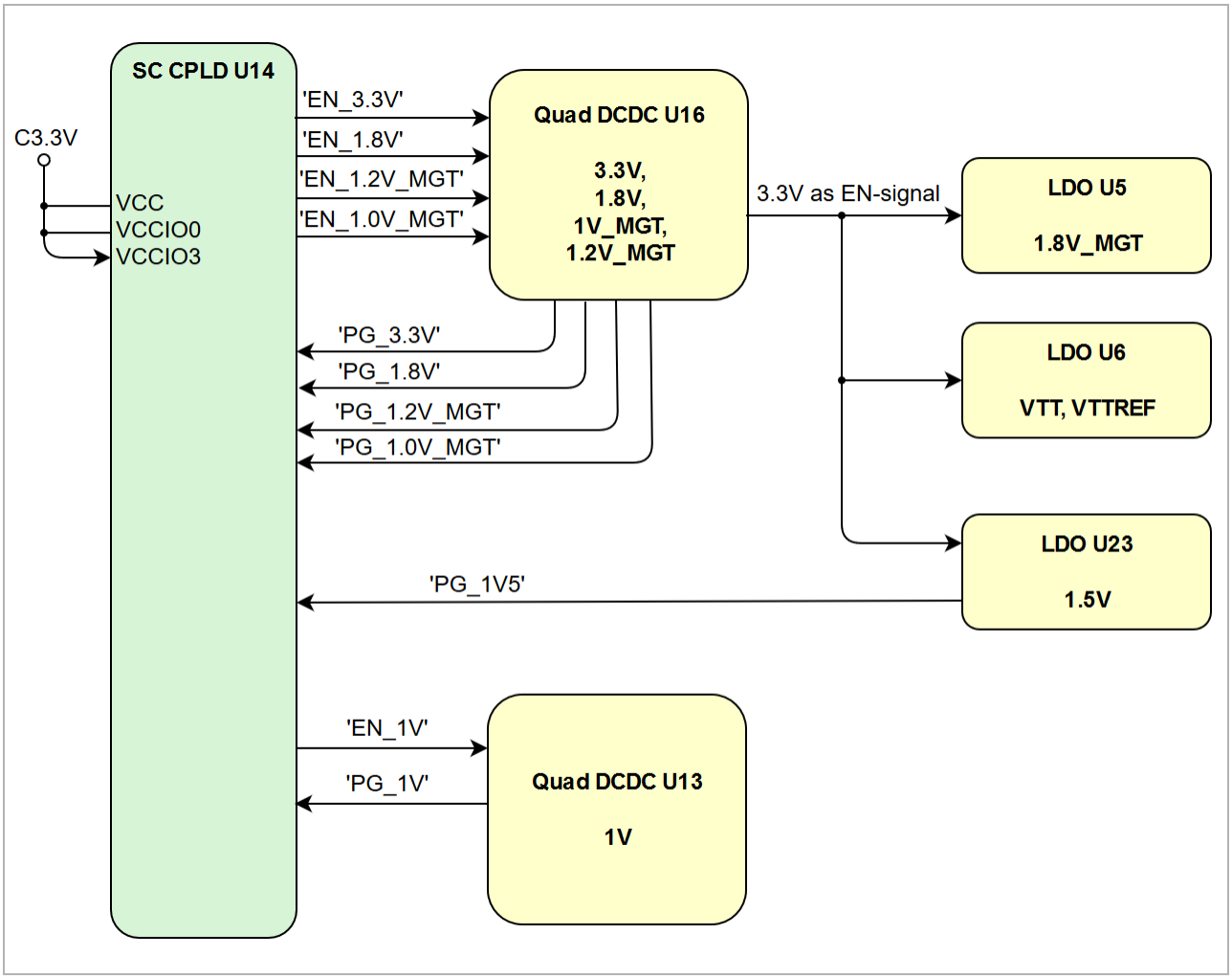


Figure 4: TE0782-02 Power-on Sequence Diagram

Voltage Monitor Circuit

The voltages '1V' and '3.3V' are monitored by the voltage monitor circuit U4, which generates the PS_POR_RST reset signal if monitored voltages have transient interruptions. The reset signal is connected to the SC CPLD U14 and forwarded to the Zynq MIO bank 500 'PS_POR' pin:

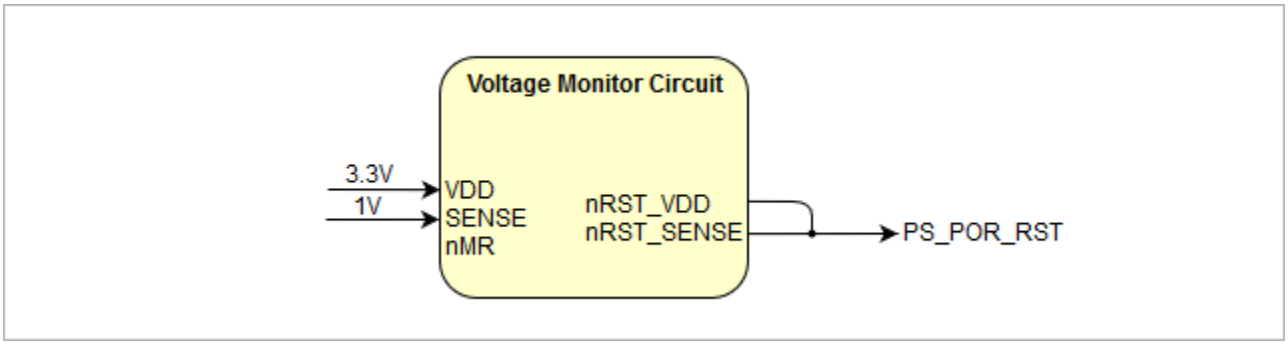


Figure 5: TE0784-01 Voltage Monitor Circuit

Power Rails

Power Rail Name on B2B Connector	J1 Pins	J2 Pins	J3 Pins	Direction	Notes
VIN	-	165, 166, 167, 168	-	Input	external power supply voltage
C3.3V	-	147, 148	-	Input	external 3.3V power supply voltage
3.3V	-	111, 112, 123, 124, 135 136 169, 170, 171, 172	-	Output	internal 3.3V voltage level
1.8V	169, 170, 171, 172	-	-	Output	internal 1.8V voltage level
VCCIO_10	-	-	99, 100	Input	high range I/O bank voltage
VCCIO_11	-	-	159, 160	Input	high range I/O bank voltage
VCCIO_12	-	159, 160	-	Input	high range I/O bank voltage
VCCIO_13	-	99, 100	-	Input	high range I/O bank voltage
VCCIO_33	99, 100	-	-	Input	high performance I/O bank voltage
VCCIO_34	159, 160	-	-	Input	high performance I/O bank voltage
VBAT_IN	-	-	124	Input	backup battery voltage

Table 16: Module power rails

Bank Voltages

Bank	Schematic Name	Voltage	Range	Notes
0	-	3.3 V	-	FPGA configuration
502	-	1.5 V	-	DDR3-RAM port
109 / 110 / 111 / 112	-	1.2 V	-	MGT
500 / 501	-	3.3 V	-	MIO banks
9 (HR)	-	1.8 V	1.2V to 3.3V	ETH2 RGMII
10 (HR)	VCCIO_10	user	1.2V to 3.3V	-
11 (HR)	VCCIO_11	user	1.2V to 3.3V	-
12 (HR)	VCCIO_12	user	1.2V to 3.3V	-
13 (HR)	VCCIO_13	user	1.2V to 3.3V	-
33 (HP)	VCCIO_33	user	1.2V to 1.8V	-

34 (HP)	VCCIO_34	user	1.2V to 1.8V	-
35 (HP)	-	1.8 V	1.2V to 1.8V	Hyper-RAM, Ethernet, I²C

Table 17: Module I/O bank voltages

See Xilinx Zynq-7000 datasheet DS191 for the voltage ranges allowed.

Board to Board Connectors

8.5 x 8.5 SoMs have three Samtec Q Strip Socket on the bottom side.

- Module use 3 x ASP-122952-01 (QTH–090–01–L–D–A) , (180 pins, "60" per bank)
- Carrier use 3 x ASP-122953-01 (QSH–090–01–F–D-A), (180 pins, "60" per bank)

Connector Specifications	Value
Insulator material	Black Liquid Crystal Polymer
Stacking height	5 mm
Contact material	Phosphor-bronze
Plating	Au or Sn over 50 µ" (1.27 µm) Ni
Current rating	2 A per pin (2 pins powered)
Operating temperature range	-55 °C to +125 °C
RoHS compliant	Yes

Connector specifications.

Connector Mating height

When using the same type on baseboard, the mating height is 5mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
	ASP-122953-01	QTH–090–01–L–D–A	5 mm
	ASP-122952-01	QSH–090–01–F–D-A	5 mm

Connectors.

The module can be manufactured using other connectors upon request.

Connector Speed Ratings

The Q Strip connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
5 mm, Single-Ended	9.5 GHz
8 mm, Single-Ended	8.5 GHz
11 mm, Single-Ended	6 GHz
16 mm, Single-Ended	5.5 GHz

20 mm, Single-Ended	3.5 GHz
30 mm, Single-Ended	3 GHz
5 mm, Differential	10.5 GHz / 25Gbit/s
8 mm, Differential	8 GHz
11 mm, Differential	5 GHz
16 mm, Differential	6 GHz
20 mm, Differential	8.5 GHz
30 mm, Differential	1.5 GHz

Speed rating.

Current Rating

Current rating of Samtec Q Strip Socket B2B connectors is 2A per pin (2 adjacent pins powered).

Connector Mechanical Ratings

- Shock: 50 G, 11 ms half Sine
- Vibration: 7.3G random, 2 hours per axis, 3 axes total

Manufacturer Documentation

File	Modified
PDF File qsh.pdf	23 07, 2019 by Pedram Babakhani
PDF File qsh-xxx-01-x-d-xx-footprint.pdf	24 07, 2019 by Pedram Babakhani
PDF File qsh-xxx-01-x-d-xxx-mkt.pdf	24 07, 2019 by Pedram Babakhani
PDF File qth.pdf	23 07, 2019 by Pedram Babakhani
PDF File qth-xxx-xx-x-d-xxx-footprint.pdf	24 07, 2019 by Pedram Babakhani
PDF File qth-xxx-xx-x-d-xxx-mkt.pdf	24 07, 2019 by Pedram Babakhani

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Variants Currently In Production

Trenz shop TE0784 overview page	
English page	German page

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VIN supply voltage	-0.3	15	V	LTM4644 datasheet
C3.3V supply voltage	-0.3	3.6	V	LTM4644 datasheet
VBAT supply voltage	-0.3	6	V	TPS780180 datasheet
PS I/O supply voltage, VCCO_PSIO	-0.5	3.6	V	Xilinx document DS191
PS I/O input voltage	-0.4	VCCO_PSIO + 0.55	V	Xilinx document DS191
HP I/O bank supply voltage, VCCO	-0.5	2.0	V	Xilinx document DS191
HP I/O bank input voltage	-0.55	VCCO + 0.55	V	Xilinx document DS191
HR I/O bank supply voltage, VCCO	-0.5	3.6	V	Xilinx document DS191
HR I/O bank input voltage	-0.55	VCCO + 0.55	V	Xilinx document DS191
Reference Voltage pin	-0.5	2	V	Xilinx document DS191
Differential input voltage	-0.4	2.625	V	Xilinx document DS191
MGT reference clocks absolute input voltage	-0.5	1.32	V	Xilinx document DS191
MGT absolute input voltage	-0.5	1.26	V	Xilinx document DS191
Voltage on SC CPLD pins	-0.5	3.75	V	Lattice Semiconductor MachXO2 datasheet
Storage temperature	-40	+85	°C	See eMMC MTFC4GACAJCN datasheet

Table 18: Module absolute maximum ratings

Recommended Operating Conditions

Parameter	Min	Max	Units	Notes
VIN supply voltage	11.4	12.6	V	LTM4644 datasheet, 12V nominal
C3.3V supply voltage	3.3	3.465	V	LCMXO2-256HC, LTM4644 datasheet
VBAT supply voltage	2.2	5.5	V	TPS780180 datasheet
PS I/O supply voltage, VCCO_PSIO	1.710	3.465	V	Xilinx document DS191
PS I/O input voltage	–0.20	VCCO_PSIO + 0.20	V	Xilinx document DS191
HP I/O banks supply voltage, VCCO	1.14	1.89	V	Xilinx document DS191
HP I/O banks input voltage	-0.20	VCCO + 0.20	V	Xilinx document DS191
HR I/O banks supply voltage, VCCO	1.14	3.465	V	Xilinx document DS191
HR I/O banks input voltage	-0.20	VCCO + 0.20	V	Xilinx document DS191
Differential input voltage	-0.2	2.625	V	Xilinx document DS191
Voltage on SC CPLD pins	-0.3	3.6	V	Lattice Semiconductor MachXO2 datasheet
Operating Temperature Range	-40	85	°C	Xilinx document DS191, industrial grade Zynq temperarure range

Table 19: Recommended operating conditions

Module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

⚠ See Xilinx datasheet DS191 for more information about absolute maximum and recommended operating ratings for the Zynq-7000 chips.

Physical Dimensions

- Module size: 85 mm × 85 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5 mm
- PCB thickness: 1.7 mm

All dimensions are shown in millimeters.

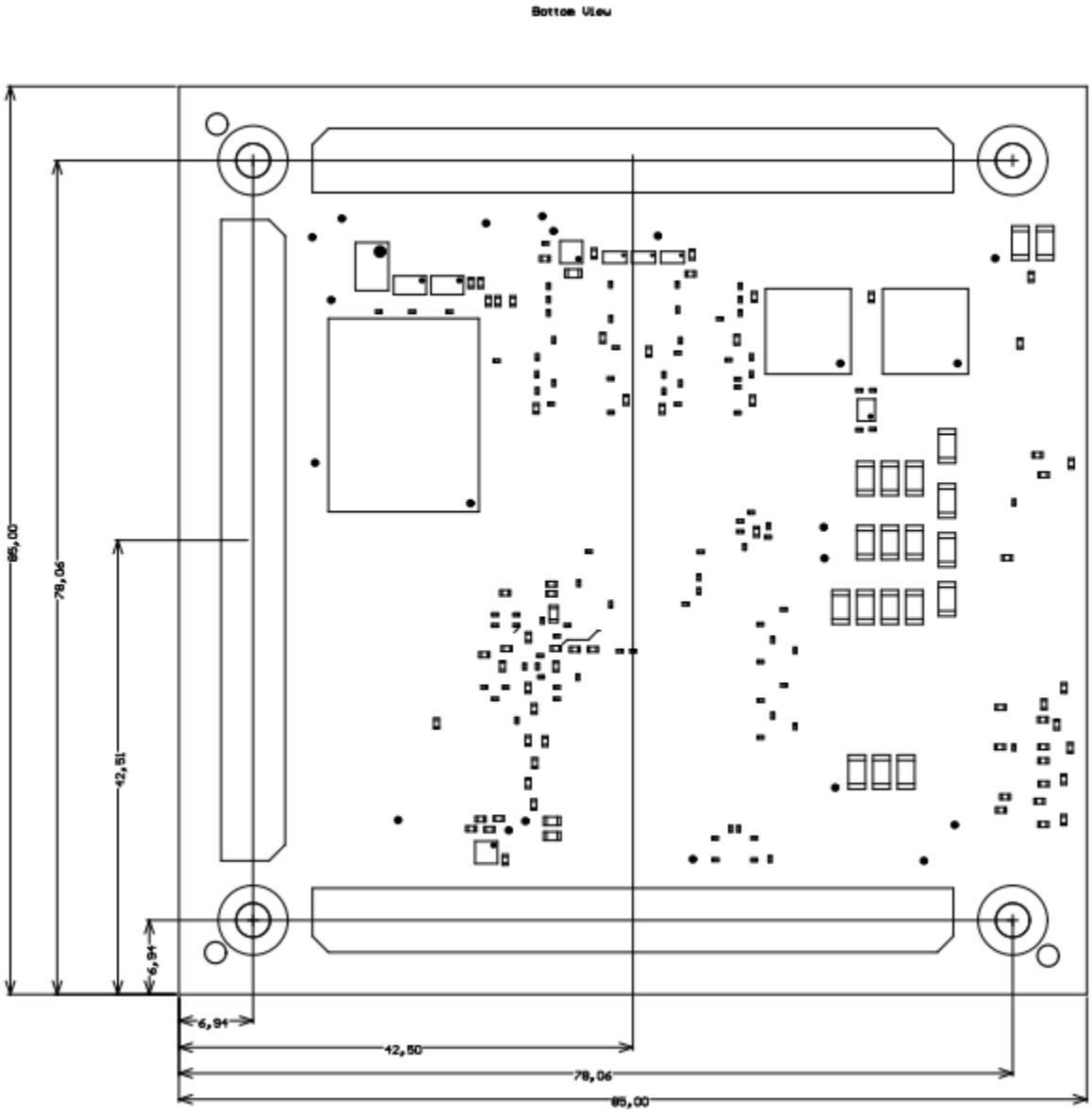

Figure 6: Module physical dimensions drawing

Revision History

Hardware Revision History

Date	Revision	Notes	PCN Link	Documentation Link
-	01	first production release	-	TE0784-01

Table 20: Hardware revision history table

Figure 7: Module hardware revision number

Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• linked B2B
2018-08-07	v.8	Ali Naseri	• Initial release

--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• --

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