TE0820-REV01_REV02 CPLD

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Overview

CPLD Device with designator U21: LCMX02-256HC

Feature Summary

- JTAG routing
- Boot Mode settings
- Power/Status Management

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Bank Power	Description
C_TCK	in	30	3.3VIN	JTAG B2B
C_TDI	in	32	3.3VIN	JTAG B2B
C_TDO	out	1	3.3VIN	JTAG B2B

C_TMS	in	29	3.3VIN	JTAG B2B
EN1	in	27	3.3VIN	Power Enable from B2B Connector (Positive Enable) / Used only for PGOOD feedback
ERR_OUT	in	4	1.8V	PS_ERROR_OUT, see ug1085
ERR_STATUS	in	5	1.8V	PS_ERROR_STATUS, see ug1085 / currently_not_used
JTAGEN	in	26	3.3VIN	Enable JTAG access to CPLD for Firmware update (zero: JTAG routed to module, one: CPLD access)
MODE	in	25	3.3VIN	Boot Mode for Zynq/ZynqMP Devices (Flash or SD)
MODE0	out	12	1.8V	ZynqMP Boot Mode Pin 0
MODE1	out	13	1.8V	ZynqMP Boot Mode Pin 1
MODE2	out	14	1.8V	ZynqMP Boot Mode Pin 2
MODE3	out	16	1.8V	ZynqMP Boot Mode Pin 3
NOSEQ	inout	23	3.3VIN	usage CPLD Variant depends
PGOOD	out	28	3.3VIN	Module Power Good.
PHY_LED1	in	17	1.8V	ETH PHY LED1
TCK	out	9	1.8V	JTAG ZynqMP
TDI	out	8	1.8V	JTAG ZynqMP
TDO	in	10	1.8V	JTAG ZynqMP
TMS	out	11	1.8V	JTAG ZynqMP
X0	out	20	VCCO_65	FPGA IO / Firmware Variant
X1	out	21	VCCO_65	FPGA IO / PHY_LED1

Functional Description

JTAG

JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA can be multiplexed via JTAGEN (logical one for CPLD, logical zero for FPGA) on JM1-89.

Boot Mode

Boot Modes can be selected via B2B Pin Mode. Trenz Electronic provides currently 4 Firmware variants, one for SD/JTAG, one for JTAG/QSPI, one for SD /QSPI and SD/QSPI/JTAG usage.

Mode	JTAG/QSPI-Variant	SD/JTAG-Variant	SD/QSPI (default Firmware)	SD/QSPI/JTAG
low	JTAG	Boot from SD	Boot from SD	JTAG Mode, if NOSEQ* is high otherwise boot from SD
high	Boot from Flash	JTAG	Boot from Flash	JTAG Mode, if NOSEQ* is high otherwise boot from Flash

For other UltraScale+ Boot Modes options custom firmware is needed, see also Table 11.1 Boot Modes from Xilinx UG1085.

A special FSBL is provided on 2017.4 or newer reference designs to write boot image to QSPI with Xilinx tools (Vivado or SDK) on Boot Mode unequal JTAG .

⚠ NOSEQ*: Please check the carrier board documentation, before using the SD/QSPI/JTAG firmware variant on TE0820. In the most cases special carrier CPLD firmware is needed.

Power

PGOOD is EN1 and not ER_OUT. There is no additional power management controlled by CPLD.

Internal pullup is used for detection, ER_OUT IO powered by 1.8V. To detect power status, also B2B 1.8V or 3.3V output is usable.

X0/X1 Pin

Pin	Description
X0*	indicate firmware variant and NOSEQ status
X1	PHY_LED1

*It's recommended to forward this signal to a carrier LED if status check is needed.

Firmware Variant	Blink sequence	Condition
QSPI/JTAG	*ooooooo	if boot mode /= JTAG otherwise const. high if NOSEQ='1' or const low if NOSEQ='0'
JTAG/SD	**oooooo	if boot mode /= JTAG otherwise const. high if NOSEQ='1' or const low if NOSEQ='0'
QSPI/SD	****oooo/********	****oooo if NOSEQ='1' or ******** if NOSEQ='0'
SD/QSPI/JTAG	***ooooo	if boot mode /= JTAG otherwise const. high if NOSEQ='1' or const low if NOSEQ='0'

Appx. A: Change History

Revision Changes

- REV02 to REV03
  - new Boot Mode variants
  - new X0 status blink sequencing
- REV01 to REV02
  - Boot Mode variants
  - X1
  - Remove ERR_STATUS

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV03	REV02, REV01		

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] Unknown macro: 'metadata'			**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.	• Update Port Table • Rename page

atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

				[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	
	v.13	REV03	REV02, REV01		• Revision 03 finished
2018-01-10	v.10	REV02	REV02, REV01	John Hartfiel	• update description - PHY LED correction
2017-08-21	v.9	REV02	REV02, REV01	John Hartfiel	• Revision 02 finished • small text updates
2017-08-17	v.8	REV02	REV02, REV01	John Hartfiel	• Revision 02 working in process • Boot Mode • X1 output

2017-06-08	v.4	REV01	REV01	John Hartfiel	• document style update
2017-03-06	v.2	REV01	REV01	John Hartfiel	• Revision 01 finished
2017-03-06	v.1	REV01	REV01	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke	• Initial release

for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassi

				an. conflu ence. core. Conte ntEntit yObjec t] [interfa ce com. atlassi an. user. User, class java. lang. String, class com. atlassi an. conflu ence. core. Conte ntEntit yObjec t]	
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Appx. B: Legal Notices

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