TE0722 TRM

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Overview

The Trenz Electronic TE0722-02 is a DIPFORTy1 "Soft Propeller" based on the Xilinx Zynq-7000 SoC.

Key Features

- Xilinx Zynq XC7Z010 SoC
- Dual-core ARM A9+ (TE0722-02-07S-1C variant has single-core ARM A9+)
- 16 MByte Quad SPI Flash
- Micro SD Card socket with card detect signal
- 34 I/Os on DIP40 header pins
- System status LED (DONE)
- RGB LED connected to PL I/O
- Green user LED connected to ARM CPU GPIO

- Proximity and ambient light sensor
- DIP40 form factor (size 18 x 51 mm)

Additional assembly options are available for cost or performance optimization upon request.

Block Diagram

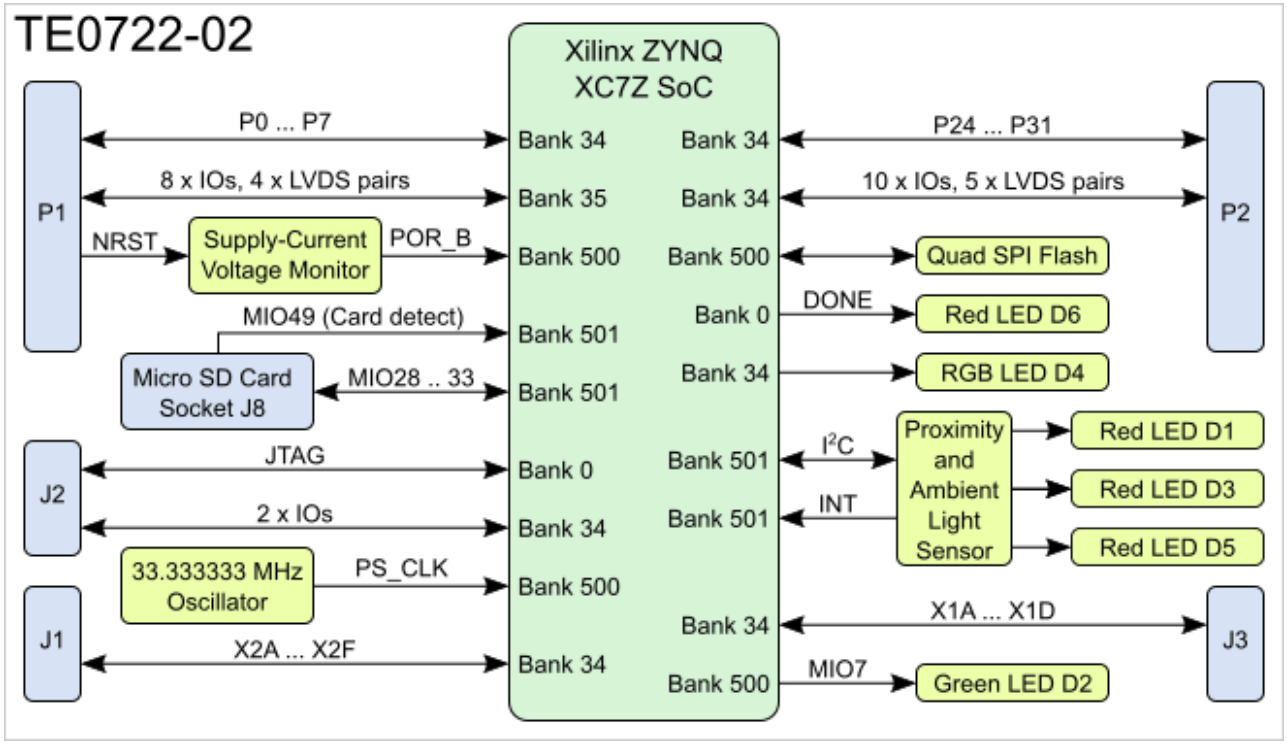

Figure 1: TE022-02 block diagram.

Main Components

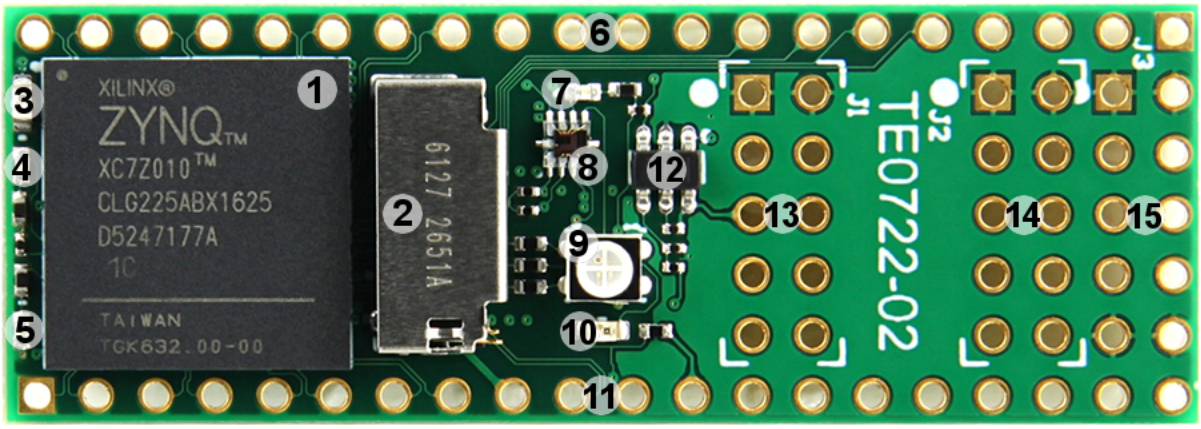

Figure 2: TE0722-02 PCB top side.

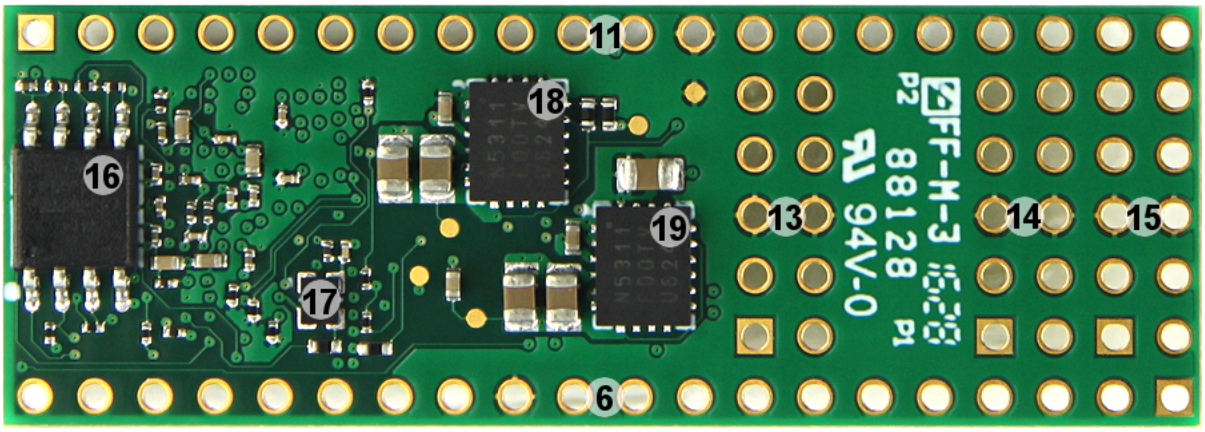

Figure 3: TE0722-02 PCB bottom side.

1. Xilinx Zynq XC7Z010 or Zynq XC7Z007S SoC, U1
2. Micro SD card socket with card detect, J8
3. Red LED, D3
4. Green LED, D2
5. Red LED, D6
6. 20-pin connector placeholder, P1
7. Red LED, D5
8. Proximity/ambient light sensor, U4
9. RGB LED, D4
10. Red LED, D1
11. 20-pin connector placeholder, P2
12. Ultra-low supply-current voltage monitor, U4
13. 2 x 5-pin connector placeholder, J1
14. 2 x 5-pin connector placeholder, J2
15. 2 x 5-pin connector placeholder, J3
16. 16 MByte QSPI Flash memory, U5
17. Low-power programmable oscillator @ 33.333333 MHz, U8
18. 1A PowerSoC DC-DC converter (1.0V), U2
19. 1A PowerSoC DC-DC converter (1.8V), U3

Initial Delivery State

Storage device name	Content	Notes
Quad SPI Flash	Empty	

Table 1: Initial delivery state of programmable devices on the module

Boot Process

The 7 boot mode strapping pins (MIO2 ... MIO8) of the Xiliny Zynq Z-7010 device are hardware programmed on the board. They are evaluated by the Zynq device soon after the 'POR_B'.signal is deasserted to begin the boot process (see section "Boot Mode Pin Settings" of Xilinx manual UG585).

The TE0722 FPGA board is hardware programmed to boot initially from the on-board QSPI Flash memory U5. The JTAG interface of the module is provided for storing the data to the QSPI Flash memory through the Zynq device.

Signals, Interfaces and Pins

I/O Signals on Connectors

Overview of the PL I/O banks signals routed to the external connectors:

Bank	Type	Connector	I/O Signal Count	Voltage	Notes
34	HR	P1	8	3.3V	Signal Schematic names: 'P0' - 'P7'
34	HR	P2	8	3.3V	Signal Schematic names: 'P24' - 'P31'
34	HR	P2	10 single ended I/O's or 5 differential pairs	3.3V	-
34	HR	J1	6	3.3V	Signal Schematic names: 'X2A' - 'X2F'
34	HR	J2	2	3.3V	-
34	HR	J3	4	3.3V	Signal Schematic names: 'X1A' - 'X1D'
35	HR	P1	8 single ended I/O's or 4 differential pairs	3.3V	-

Table 2: Zynq SoC PL I/O signals overview

Zynq SoC I/O Banks

Bank	Type	VCCIO	I/O Signal Count	Available on Connectors	Notes
34	HR	3.3V	41	38	38 user I/O's, 3 I/O's used for controlling the RGB LED D4.
35	HR	3.3V	8	8	8 single ended or 4 differential.
500	PS MIO	3.3V	7	-	6 MIO pins used for QSPI flash memory interface, 1 MIO pin connected to green LED D2.
501	PS MIO	3.3V	10	-	7 MIO pins used for SD Card interface, 3 MIO pins connected to light sensor U4.
0	Config	3.3V	5	-	4 I/O's are dedicated to JTAG interface, 'DONE'-signal is indicated by red LED D6.

Table 3: General overview of Zynq SoC PL/PS I/O banks

JTAG Interface

JTAG access to the Xilinx ZYNQ XC7Z010 SoC is provided through J2 connector:

JTAG Signal	J2 Connector Pin
TCK	4
TDI	9
TDO	10
TMS	8

Table 4: JTAG interface signals

Quad SPI Interface

Quad SPI Flash memory (U5) is connected to the Zynq SoC PS QSPI0 interface via PS MIO bank 500, pins MIO1 ... MIO6:

Zynq SoC's MIO-pin	U5 Pin	Signal Schematic Name

MIO1	1	SPI0-CS
MIO2	5	SPI0-DQ0/M0
MIO3	2	SPI0-DQ1/M1
MIO4	3	SPI0-DQ2/M2
MIO5	7	SPI0-DQ3/M3
MIO6	6	SPI0-SCK

Table 5: Quad SPI interface signals and connections

SD Card Interface

TE0722 board has on-board 3.3V SD Card socket (J8) with card detect switch wired to the Zynq SoC PS MIO bank 501, pins MIO28 .. MIO33 and MIO49.

Zynq SoC's MIO-pin	J8 pin	Signal Schematic Name
MIO28	J8-7	DAT0
MIO29	J8-3	CMD
MIO30	J8-5	CLK
MIO31	J8-8	DAT1
MIO32	J8-1	DAT2
MIO33	J8-2	CD/DAT3
MIO49	J8-G4	Card detect switch

Table 6: SD card interface signals

I²C Interface

I^{2}C interface pins SCL and SDA from the Zynq SoC PS MIO-bank 501 (MIO36, MIO37) are connected to ambient / proximity light sensor (U4).

Zynq SoC's MIO-pin	U4 pin	Signal Schematic Name
MIO36	2	SCL
MIO37	1	SDA

Table 7: Zynq SoC I^{2}C interface signals

Default PS MIO Mapping

MIO-pin	Function	Connector to
MIO1	QSPI	QSPI flash memory, pin 1
MIO2	QSPI	QSPI flash memory, pin 5
MIO3	QSPI	QSPI flash memory, pin 2
MIO4	QSPI	QSPI flash memory, pin 7

MIO5	QSPI	QSPI flash memory, pin 3
MIO6	QSPI	QSPI flash memory, pin 6
MIO7	GPIO	Green LED D2
MIO28	SDIO	SD Card socket. pin J8-5
MIO29	SDIO	SD Card socket. pin J8-3
MIO30	SDIO	SD Card socket. pin J8-7
MIO31	SDIO	SD Card socket. pin J8-8
MIO32	SDIO	SD Card socket. pin J8-1
MIO33	SDIO	SD Card socket. pin J8-2
MIO36	I²C	Ambient / Proximity Light Sensor U4, pin 2
MIO37	I²C	Ambient / Proximity Light Sensor U4, pin 1
MIO39	GPIO	Ambient / Proximity Light Sensor U4, Interrupt pin 4
MIO49	GPIO	SD Card socket card detect pin J8-G4

Table 8: Default mapping of Zynq PS MIO-bank pins

On-board Peripherals

Quad SPI Flash Memory

On-board QSPI flash memory (U5) is provided by Cypress Semiconductor Serial Flash Memory S25FL127SABMFV101 with 128 MBit (16 MByte) storage capacity. This non volatile memory is used to store initial configuration data. Besides initial configuration data, remaining free flash memory can be used for user application and data storage.

Proximity and Ambient Light Sensor

The TE0722-02 Zynq SoC board is equipped with the Si1143 infrared proximity and ambient light sensor. On-board three red LEDs D1, D3 and D5 are connected to the light sensor to use the proximity sensing functionality. For more details and how to configure and use this chip, refer to the Si1141/42/43 data sheet.

Oscillator

The Zynq SoC board one reference clocking signal as system clock provided by on-board oscillator U8:

Clock Source	Frequency	Clock Input Destination
SiTime SiT8008AI Oscillator, U8	33.333333 MHz	Zynq PS Bank 500, pin C7

Table 9: Clock sources overview

On-board LEDs

There are 6 LEDs fitted on the Zynq SoC board. The LEDs are user configurable to indicate for example any system status.

LED	Color	Connected to	Signal Schematic Name	Description and Notes

D1	Red	Light sensor U4, pin 6	-	Proximity sensing functionality of light sensor U4
D2	Green	Zynq PS bank 500	MIO7	user configurable
D3	Red	Light sensor U4, pin 9	-	Proximity sensing functionality of light sensor U4
D4	RGB	Zynq PL bank 34, pins J15, L14, K12	RGB_R, U1, RGB_G, U1, RGB_B, U1	user configurable
D5	Red	Light sensor U4, pin 7	-	Proximity sensing functionality of light sensor U4
D6	Green	Zynq config bank 0	DONE	Reflects inverted DONE signal. ON when FPGA is not configured, OFF as soon as PL configuration is finished.

Table 10: LEDs of the board

Connectors

All connectors are for 100mil (2.54mm pitch) headers, all connector locations are in 100mil grid. The module's PCB provides footprints to mount and solder optional pin headers, if those are not factory-fitted on module.

Power and Power-On Sequence

To power-up a module, power supply with minimum current capability of 1A is recommended.

Power Supply

TE0722-02 needs one single power supply with nominal of 3.3V at all variants. Following diagram shows the dependencies of the power supply:

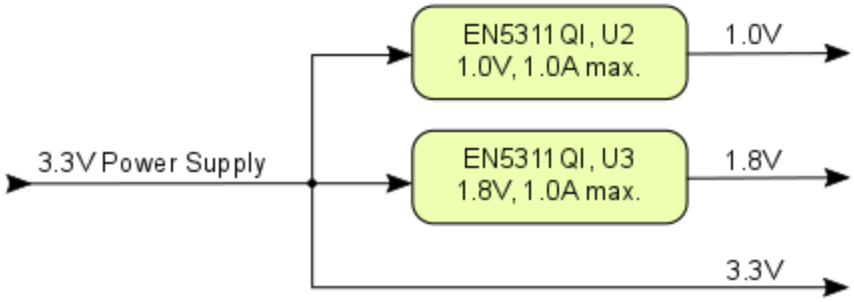

Figure 4: Module power supply dependencies

Power Consumption

Board Variant	FPGA	Design	Typical Power, 25°C ambient
TE0722-02I	XC7Z010-1CLG225I	Not configured	TBD*
TE0722-02	XC7Z010-1CLG225C	Not configured	TBD*
TE0722-02-07S-1C	XC7Z007S-1CLG225C	Not configured	TBD*

Table 11: Module power consumption

*TBD - To Be Determined.

The maximum power consumption of the module mainly depends on the design running on the Zynq SoC's FPGA and ambient temperature.

Xilinx provide a power estimator excel sheets to calculate power consumption. It is also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power-On Sequence

There is no specific or special power-on sequence, single power source is needed as 3.3V as power supply voltage.

Voltage Monitor Circuit

The voltages 1.0V (core voltage) and 3.3V are monitored by the voltage monitor circuit U6, which generates the POR_B reset signal at power-on. A manual reset is also possible by driving the connector pin P1-10 ('NRST') to GND. Leave this pin unconnected or connect to VDD (3.3V) when unused.

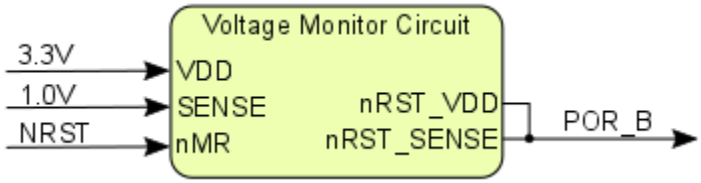

Figure 5: Voltage monitor circuit

Power Rails

Power Rail Name	J1 Pins	J2 Pins	J3 Pins	P1 Pin	P2 Pin	Direction	Notes
3.3V	5, 6	5, 6	5, 6	12	12	Input	3.3V power supply voltage

Table 12: Board power rails

Bank Voltages

Bank	Bank I/O Voltage VCCO	Voltage Range
0 (config)	3.3V	fixed
500 (MIO)	3.3V	fixed
501 (MIO)	3.3V	fixed
34 (HR)	3.3V	fixed
35 (HR)	3.3V	fixed

Table 13: Board bank voltages

Variants Currently in Production

Board Variant	Xilinx Zynq SoC	ARM Cores	PL Cells	LUTs	Flip-Flops	Block RAM	DSP Slices	Zynq SoC Operating Temp.	Temp. Range
TE0722-02I	XC7Z010-1CLG225I	A9+ Dual-core	28K	17,6K	35,2K	2.1 MBytes	80	–40°C to +100°C	Industrial

TE0722-02	XC7Z010-1CLG225C	A9+ Dual-core	28K	17,6K	35,2K	2.1 MBytes	80	0°C to +85°C	Commercial
TE0722-02-07S-1C	XC7Z007S-1CLG225C	A9+ Single-core	23K	14,4K	28,8K	1.8 MBytes	66	0°C to +85°C	Commercial

Table 14: Board variants

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference Document
3.3 supply voltage	-0.3	3.6	V	EN5311QI datasheet / Xilinx datasheet DS187
HR PL I/O banks input voltage (VCCIO single ended)	-0.4	VCCO + 0.55	V	Xilinx datasheet DS187 (VCCO 3.3V nominal)
Storage temperature	-40	+85	°C	Silicon Labs Si1141/42/43 datasheet.

Table 15: Board absolute maximum ratings

Recommended Operating Conditions

Parameter	Min	Max	Units	Reference Document
3.3 supply voltage	3.3	3.465	V	Xilinx datasheet DS187
HR PL I/O banks input voltage (VCCIO single ended)	-0.20	VCCO + 0.20	V	Xilinx datasheet DS187 (VCCO 3.3V nominal)
Operating Temperature Commercial (Variant TE0722-02 and TE0722-02-07S-1C)	0	+85	°C	Xilinx datasheet DS190
Operating Temperature Industrial (Variant TE0722-02I)	-40	+85		Xilinx datasheet DS190

Table 16: Board recommended operating condition

⚠ Please check Xilinx datasheet DS187 for complete list of absolute maximum and recommended operating ratings for the Zynq-7 device.

Physical Dimensions

- Module size: 17.9 mm × 51 mm. Please download the assembly diagram for exact numbers.
- PCB thickness: 1.65 mm.
- Highest part on PCB approx. 4 mm. Please download the step model for exact numbers.

All dimensions are given in millimeters.

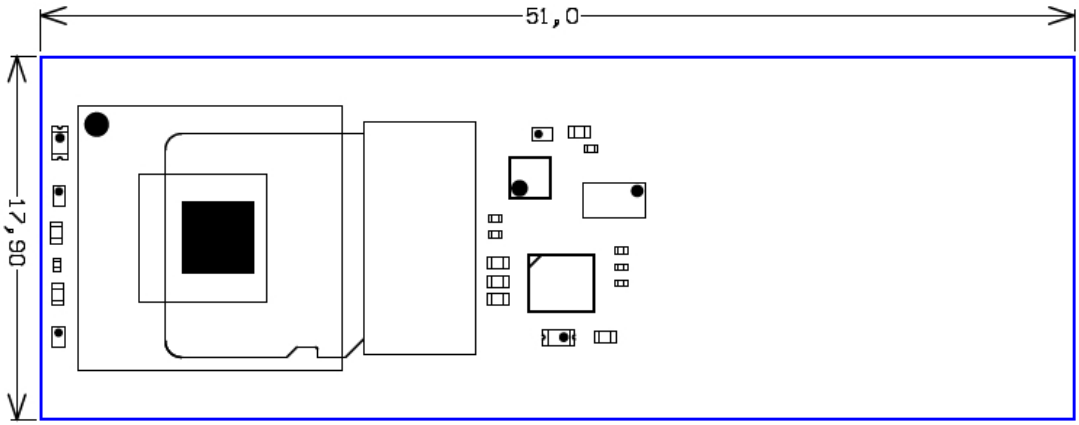

Figure 6: Board physical dimensions

Revision History

Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
-	02	-	-	TE0722-02
-	01	First production release	-	-

Table 17: Board hardware revision history

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.

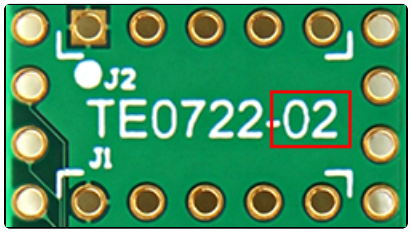

Figure 7: TE0722 module hardware revision number

Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	Unknown macro: 'metadata'	Ali Naseri, Jan Kumann	• First TRM Release

Table 18: Document change history

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]