

TE0714 TRM

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Table of Contents

- [Overview](#)
 - [Key Features](#)
 - [Block Diagram](#)
 - [Main Components](#)
 - [Initial Delivery State](#)
 - [Control Signals](#)
- [Signals, Interfaces and Pins](#)
 - [JTAG Interface](#)
 - [Board to Board \(B2B\) I/Os](#)
- [On-board Peripherals](#)
 - [Quad SPI Flash](#)
 - [On-board LED](#)
 - [Clock](#)
- [Power and Power-On Sequence](#)
 - [Power Consumption](#)
 - [Power Distribution Dependencies](#)
 - [Power-On Sequence](#)
 - [Power Rails](#)
 - [Bank Voltages](#)
- [Board to Board Connectors](#)
 - [Connector Speed Ratings](#)
 - [Current Rating](#)
 - [Connector Mechanical Ratings](#)
 - [Manufacturer Documentation](#)
- [Technical Specifications](#)
 - [Absolute Maximum Ratings](#)
 - [Recommended Operating Conditions](#)
 - [Physical Dimensions](#)
- [Variants Currently In Production](#)
- [Revision History](#)
 - [Hardware Revision History](#)
 - [Document Change History](#)
- [Disclaimer](#)
 - [Data Privacy](#)
 - [Document Warranty](#)
 - [Limitation of Liability](#)
 - [Copyright Notice](#)
 - [Technology Licenses](#)
 - [Environmental Protection](#)
 - [REACH, RoHS and WEEE](#)

Overview

The Trenz Electronic TE0714 is an industrial-grade SoM (System on Module) based on Xilinx Artix-7, 16 MByte Flash memory and powerful switching mode power supplies for all on-board voltages. A large number of configurable I/O's is provided via rugged high-speed stacking strips. TE0714 is the smallest module with transceiver (3 x 4 cm).

Refer to <http://trenz.org/te0714-info> for the current online version of this manual and other available documentation.

Key Features

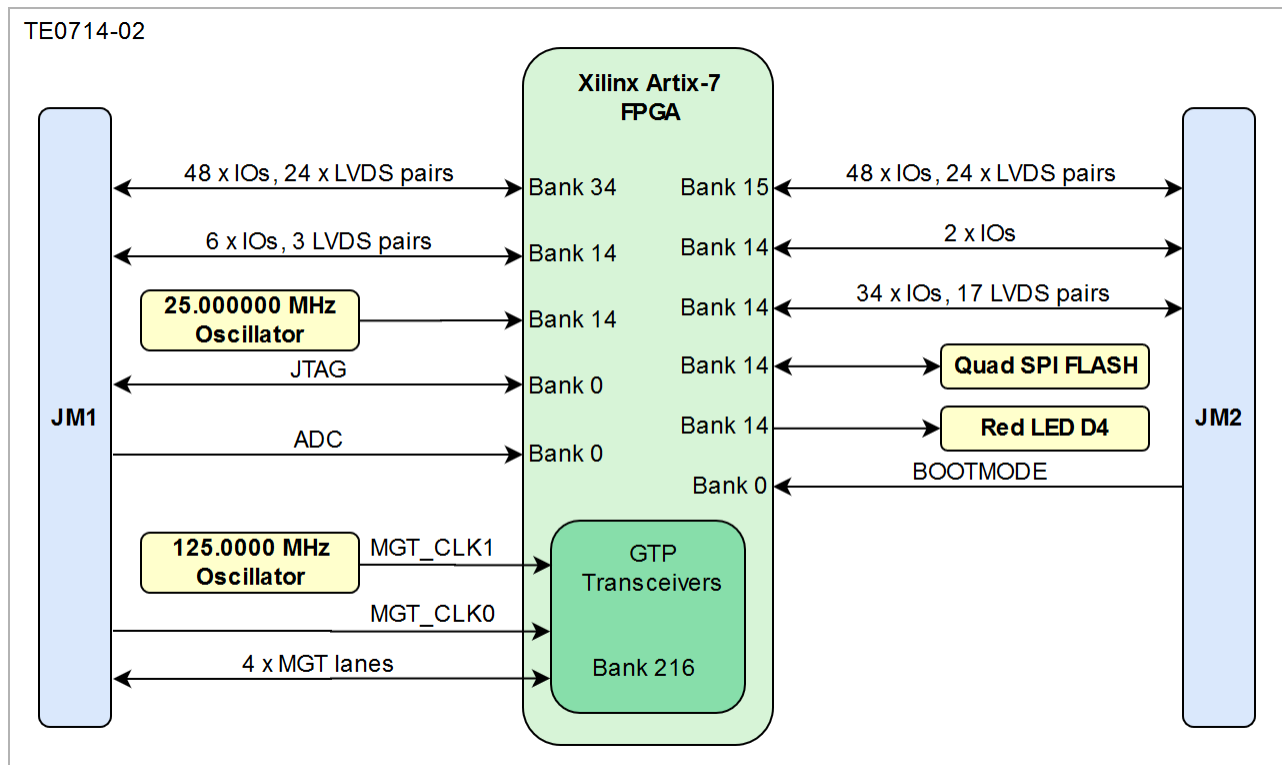
- Xilinx Artix-7 FPGA (A15T, A35T, A50T)
- Rugged for shock and high vibration

- 16 MByte QSPI Flash memory
- Differential MEMS oscillator for MGT clocking
- MEMS oscillator for PL clocks (Optional)
- Plug-on module with 2 x 100-pin high-speed hermaphroditic strips
 - 138 FPGA I/O's (Max 68 differential)
 - 5 IO's (QSPI or user I/O's)
 - XADC analog input
 - 4 GTP (high-performance transceiver) lanes
 - GT reference clock inputs
 - Optimized I/O and power pins for good signal integrity
- On-board high-efficiency DC-DC converters
- Power supply for all on-board components
- eFUSE bit-stream encryption (AES)
- One user configurable LED

Different configurations for cost and performance optimization available upon request. Available options are:

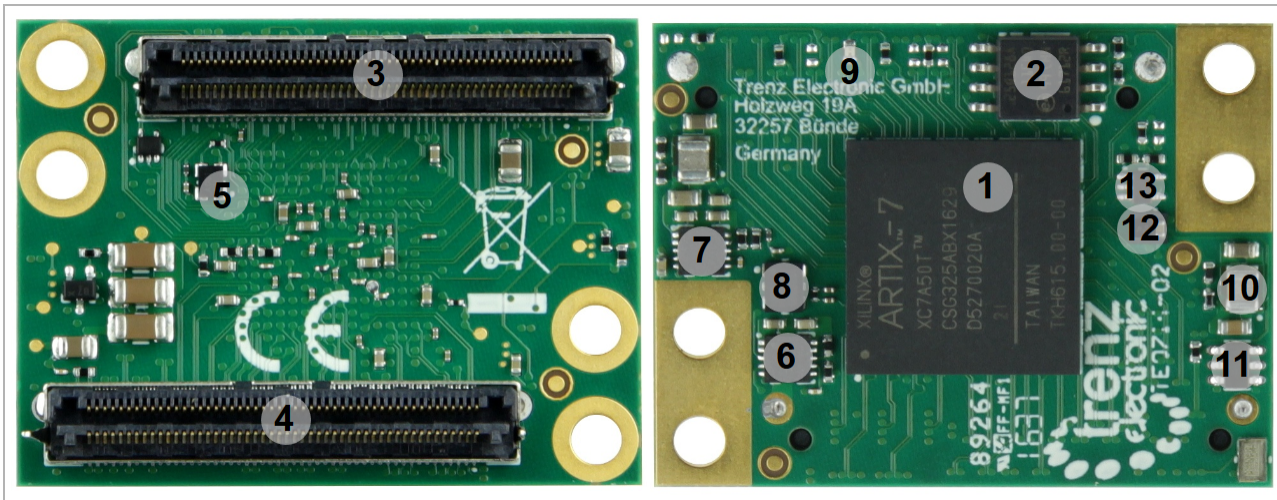
- FPGA Type (A15T, A35T, A50T), temperature grade
- GT clock frequency (or none if not implemented)
- PL clock frequency and precision (or none if not implemented)
- Config and B14 bank Voltage: 1.8V or 3.3V
- SPI Flash type (or none if not implemented)
- LED Color (or none if not implemented)
- PUDC Pin strapping (pull high or pull down)
- GT power enable pin strapping (default power enabled or disabled)

Block Diagram



TE0714 block diagram

Main Components



TE0714 main components

1. Xilinx Artix-7 FPGA (XC7A series), U4
2. 16 MByte SPI Flash, U7
3. B2B connector Samtec Razor Beam™ LSHM-150, JM2
4. B2B connector Samtec Razor Beam™ LSHM-150, JM1
5. 25 MHz oscillator, U8
6. Single output low-dropout linear regulator (1.2V_MGT), U6
7. Single output low-dropout linear regulator (1.0V_MGT), U5
8. Low-jitter precision LVDS 125 MHz oscillator (GT Clock), U2
9. Red indication LED, D4
10. Step-down DC-DC converter (1.0V), U1
11. PFET load switch with configurable slew rate (3.3V), Q1
12. Low-power step-down DC-DC converter (1.8V), U3
13. Voltage detector for circuit initialization and timing supervision, U23

Initial Delivery State

| Storage device name | Content | Notes |
|---------------------------|-----------------------|---|
| SPI Flash OTP Area | Empty, not programmed | Except serial number programmed by flash vendor |
| SPI Flash Quad Enable bit | Programmed | |
| SPI Flash main array | demo design | |
| eFUSE USER | Not programmed | |
| eFUSE Security | Not programmed | |


Initial delivery state of programmable devices on the module.

Control Signals

Boot process is controlled by signals on the board to board (B2B) connector.

| Signal | Direction | Signal State | Description |
|----------|-----------|---------------|--|
| BOOTMODE | input | high or open | Master SPI, x4 Mode |
| | | low or ground | Slave SelectMAP |
| PROG_B | input | pulsed low | Clear FPGA configuration (falling edge) and initiate a new configuration sequenz (next rising edge). |
| DONE | output | high | Completion of configuration sequence. |

Boot signals.



SPI FPGA pins D02 and D03 have no pull-ups on the module, so with PUDC=High option, those pins are floating if there are no pull-ups on baseboard. As those pins have SPI RESET function when Quad mode is not enabled, it is mandatory to either add pull-ups on user baseboard or program the Quad Enable bit in Flash nonvolatile status register.

Signals, Interfaces and Pins

JTAG Interface

JTAG access to the Xilinx Artix-7 FPGA device is provided through connector JM1.

| Signal Name | B2B Pin |
|-------------|---------|
| TCK | JM1:89 |
| TDI | JM1:85 |
| TDO | JM1:87 |
| TMS | JM1:91 |

JTAG signals.

Board to Board (B2B) I/Os

FPGA bank number and number of I/O signals connected to the B2B connector:

| FPGA Bank | B2B Connector | I/O Signal Count | Voltage Level | Notes |
|-----------|---------------|------------------|----------------------|-----------------------------|
| 14 | JM1 | 6 | VCCIO_0 | |
| 14 | JM2 | 36 | VCCIO_0 | NB! 17 LVDS pairs possible. |
| 15 | JM2 | 48 | VCCIO15 | Supplied by the baseboard. |
| 34 | JM1 | 48 | VCCIO34 | Supplied by the baseboard. |
| 216 | JM1 | 16 | MGT_AVCC MGT_AVTT | 4 x GTP lanes. |

B2B I/Os

Please refer to the [Pin-out](#) tables page for additional information.

On-board Peripherals

Quad SPI Flash

On-board SPI flash memory S25FL127S (U7) is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the bus width and clock frequency used.



SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash. By default this bit is set to high at the manufacturing plant.

On-board LED

There is one LED on TE0714 module.

| LED | Color | FPGA | Notes |
|-----|-------|------|-------------------|
| D4 | Red | K18 | User programmable |

LED connection.

Clock

| Clock | Default Frequency | IC | FPGA | Notes |
|----------|-------------------|----|-------|---|
| CLK25MHz | 25 MHz | U8 | T14 | Frequency depends on the module variant. Output is compatible to 3.3V and 1.8V I/O standard of the FPGA bank. |
| MGT_CLK | 125MHz | U2 | B6/B5 | Frequency depends on the module variant |

Clock signals.

Power and Power-On Sequence

To power-up a module, power supply with minimum current capability of 1A is recommended.

TE0714 needs one single power supply with nominal of 3.3V.

Power Consumption

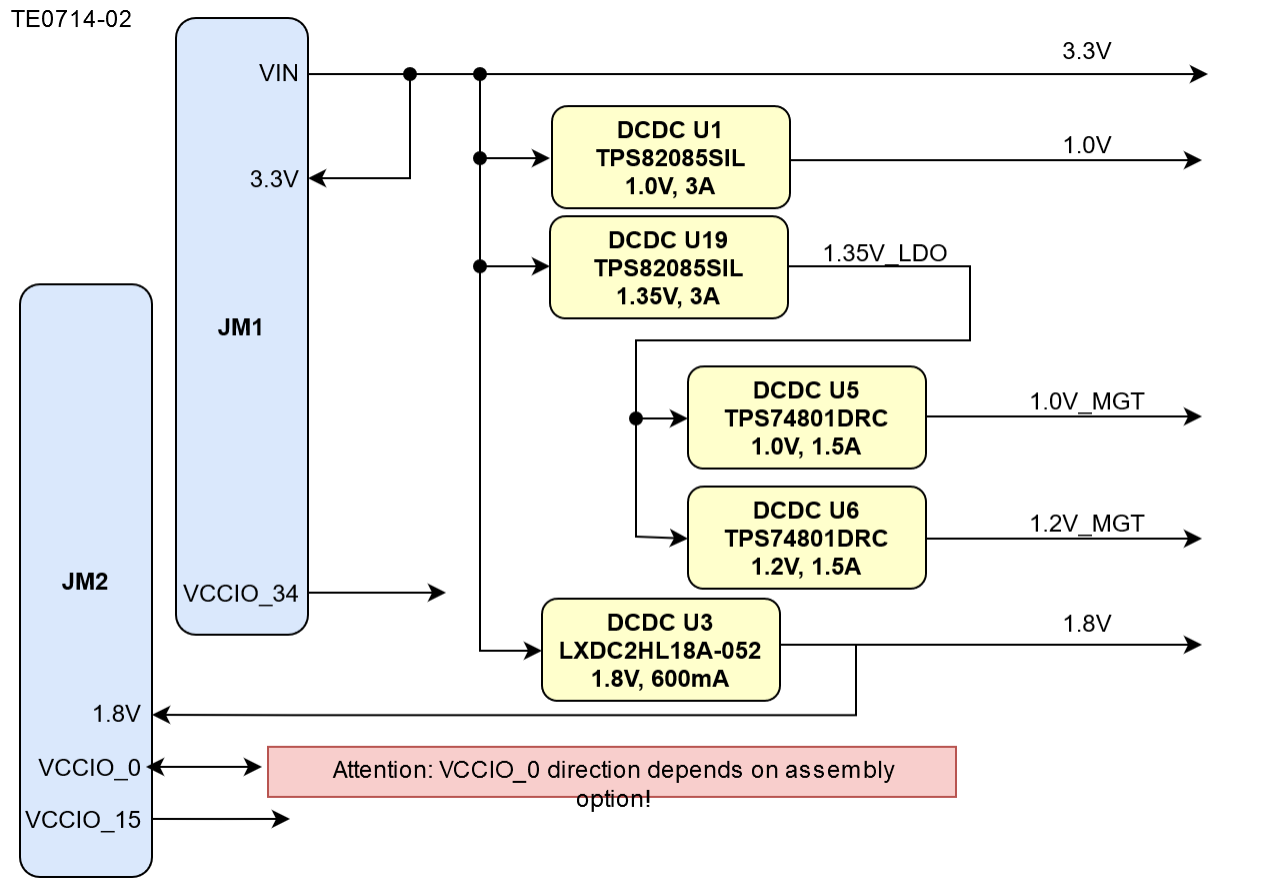
| Test Condition (25 °C ambient) | VIN Current mA | Notes |
|---|----------------|-------|
| TE0714-35, TEBT0714, empty design, GT not enabled | 110mA | |

Power Consumption

Actual power consumption depends on the FPGA design and ambient temperature.

Power Distribution Dependencies

TE0714-02

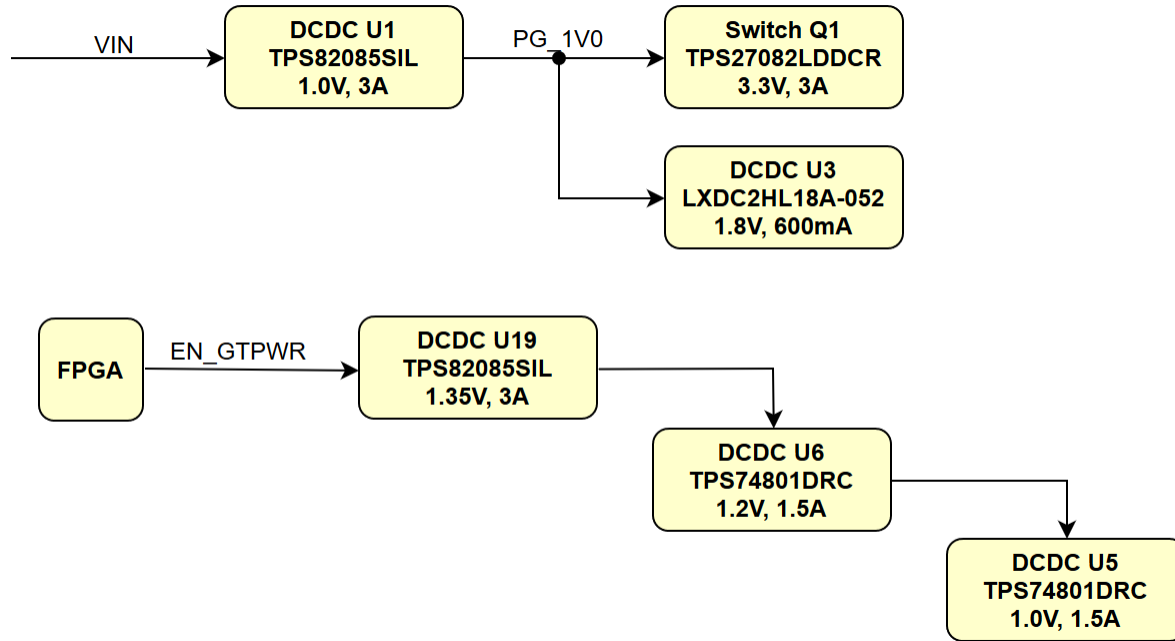


Power Distribution

Power-On Sequence

There is no specific or special power-on sequence, single power source is needed as VIN, rest of the sequence is automatic.

TE0714-02



Power-On Sequence

Power Rails

| Voltages on B2B-Connector | B2B JM1-Pin | B2B JM2-Pin | Direction | Note |
|---------------------------|-------------|-------------|-----------|-----------------------------|
| VIN | 98, 100 | - | input | supply voltage |
| VCCIO_0 | - | 54 | input | high range bank voltage |
| VCCIO_15 | - | 53 | input | high range bank voltage |
| VCCIO_34 | 62 | - | input | high range bank voltage |
| 3.3V | 84 | - | output | internal 3.3V voltage level |
| 1.8V | - | 17 | output | internal 1.8V voltage level |

Power Rails

Bank Voltages

| Bank | Voltage | Notes |
|------------------|--------------|---|
| 0 Config and B14 | 1.8V or 3.3V | Depends on module assembly variant. See R21, R22 and R27 assembly option* |
| 15 | User | Supplied from baseboard via B2B connector, max 3.3V |
| 34 | User | Supplied from baseboard via B2B connector, max 3.3V |

- *R21 assembled: 3.3V and B2B is output if R27 is assembled
- *R22 assembled 1.8V and B2B is output if R27 is assembled

- *R21 and R22 **not** assembled , B2B is input and carrier defines voltage pay attention on assembled flash!

Bank Voltages

Board to Board Connectors



These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

3 x 4 modules use two [Samtec Razor Beam LSHM connectors](#) on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row).

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height.

| Order number | Connector on baseboard | compatible to | Mating height |
|--------------|-----------------------------|-----------------------------|---------------|
| 23836 | REF-189016-01 | LSHM-150-02.5-L-DV-A-S-K-TR | 6.5 mm |
| | LSHM-150-03.0-L-DV-A-S-K-TR | LSHM-150-03.0-L-DV-A-S-K-TR | 7.0 mm |
| 23838 | REF-189016-02 | LSHM-150-04.0-L-DV-A-S-K-TR | 8.0 mm |
| | LSHM-150-06.0-L-DV-A-S-K-TR | LSHM-150-06.0-L-DV-A-S-K-TR | 10.0mm |

Connectors.

The module can be manufactured using other connectors upon request.

Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

| Stacking height | Speed rating |
|---------------------|--------------------|
| 12 mm, Single-Ended | 7.5 GHz / 15 Gbps |
| 12 mm, Differential | 6.5 GHz / 13 Gbps |
| 5 mm, Single-Ended | 11.5 GHz / 23 Gbps |
| 5 mm, Differential | 7.0 GHz / 14 Gbps |

Speed rating.

Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

Manufacturer Documentation

File

Modified

| | |
|---|----------------------------------|
| PDF File hsc-report_lshm-lshm-05mm_web.pdf | 18 09, 2018 by Martin Rohrmüller |
| PDF File lshm_dv.pdf | 18 09, 2018 by Martin Rohrmüller |
| PDF File LSHM-1XX-XX.X-X-DV-A-X-X-TR-FOOTPRINT(1).pdf | 18 09, 2018 by Martin Rohrmüller |
| PDF File LSHM-1XX-XX.X-XX-DV-A-X-X-TR-MKT.pdf | 18 09, 2018 by Martin Rohrmüller |
| PDF File REF-189016-01.pdf | 18 09, 2018 by Martin Rohrmüller |
| PDF File REF-189016-02.pdf | 18 09, 2018 by Martin Rohrmüller |
| PDF File TC0923--2523_report_Rev_2_qua.pdf | 18 09, 2018 by Martin Rohrmüller |
| PDF File tc0929--2611_qua(1).pdf | 18 09, 2018 by Martin Rohrmüller |

[Download All](#)

Technical Specifications

Absolute Maximum Ratings

| Parameter | Min | Max | Units | Reference Document |
|--------------------------------------|------|---------------|-------|--|
| VIN supply voltage | -0.1 | 6.0 | V | - |
| HR I/O banks supply voltage (VCCO) | -0.5 | 3.6 | V | Xilinx datasheet DS181 |
| HR I/O banks input voltage | -0.4 | VCCO + 0.55 | V | Xilinx datasheet DS181 |
| GTP transceivers Tx/Rx input voltage | -0.5 | 1.26 | V | Xilinx datasheet DS181 |
| Voltage on module JTAG pins | -0.4 | VCCO_0 + 0.55 | V | Xilinx datasheet DS181 |
| Storage temperature | -40 | +100 | °C | - |

Module absolute maximum ratings.

Recommended Operating Conditions

This TRM is generic for all variants.

Variants of modules are described here: [Article Number Information](#)

Modules with commercial temperature grade are equipped with components that cover at least the range of 0°C to 75°C

Modules with extended temperature grade are equipped with components that cover at least the range of 0°C to 85°C

Modules with industrial temperature grade are equipped with components that cover at least the range of -40°C to 85°C

The actual operating temperature range will depend on the FPGA / SoC design / usage and cooling and other variables.

| Parameter | Min | Max | Units | Reference Document |
|------------------------------------|-------|-------|-------|--|
| VIN supply voltage | 3.135 | 3.45 | V | - |
| HR I/O banks supply voltage (VCCO) | 1.14 | 3.465 | V | Xilinx datasheet DS181 |

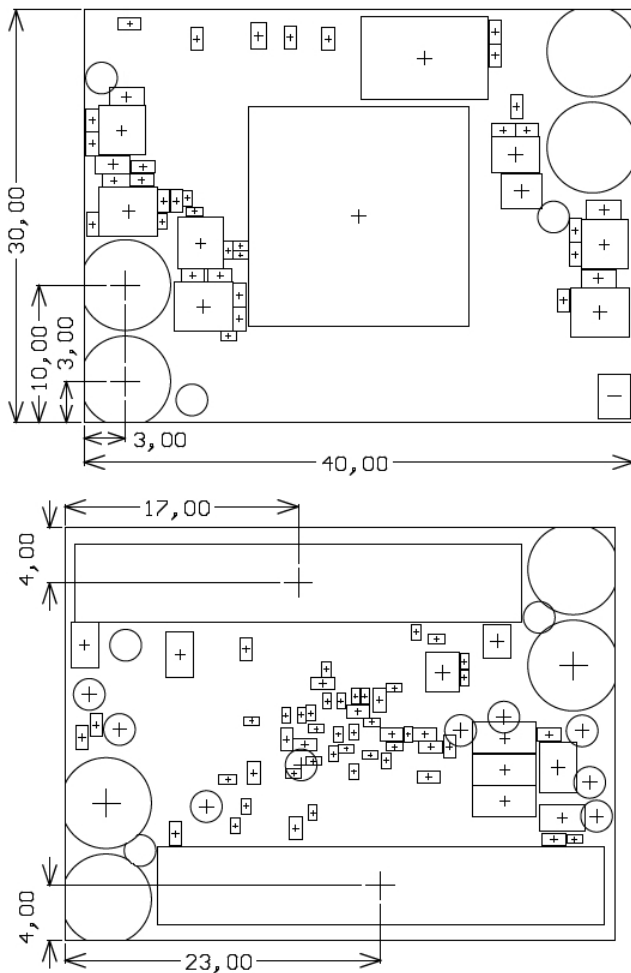
| | | | | |
|-----------------------------|-------|--------------|---|--|
| HR I/O banks input voltage | -0.20 | VCCO + 0.20V | V | Xilinx datasheet DS181 |
| Voltage on module JTAG pins | 0 | VCCO_0 + 5% | V | Xilinx datasheet DS181 |

Recommended Operating Conditions

Physical Dimensions

- Module size: 40 mm x 30 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8 mm
- PCB thickness: 1.6 mm
- Highest part on PCB: approximately 2.5 mm. Please download the step model for exact numbers.

All dimensions are shown in mm. Additional sketches, drawings and schematics can be found [here](#).




Physical dimensions drawing

Variants Currently In Production

Trenz shop TE0714 overview page

| | |
|------------------------------|-----------------------------|
| English page | German page |
|------------------------------|-----------------------------|

Trenz Electronic Shop Overview



On REV 01 JM2 Pin 54 was connected to GND. When R27 is not populated, REV 02 is backwards compatible to REV 01. When R27 is set, check your baseboard to not connect this pin to GND. For all new baseboards JM2.54 should be used as VCCIO output (it will then be 1.8V or 3.3V depending the voltage settings on the module).

Revision History

Hardware Revision History

| Date | Revision | PCN | Documentation Link | Note |
|------------|----------|------------------------------|---------------------------|---------------------|
| 2016-08-04 | 02 | PCN-20160815 | TE0714-02 | VCCIO0 added to B2B |
| | 01 | - | TE0714-01 | - |

Hardware Revision History

Hardware revision number is printed on the PCB board next to the module model number separated by the dash.



Document Change History

| Date | Revision | Authors | Description |
|------|----------|---------|-------------|
|------|----------|---------|-------------|

| | | | |
|--|--|--|--|
| <p>Error rendering macro 'page-info'</p> <p>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> | <p>Error rendering macro 'page-info'</p> <p>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> | <p>Error rendering macro 'page-info'</p> <p>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> | <ul style="list-style-type: none"> Updated storage temperature. |
| 2021-04-07 | v59 | Thomas Steffens | <ul style="list-style-type: none"> changed operating conditions |
| 2019-03-04 | v55 | John Hartfiel | <ul style="list-style-type: none"> Restore and modify v. 50 Correction max IO count on key features Change history table typo correction |

| | | | |
|------------|------|-------------------|--|
| 2019-01-07 | v.50 | John Hartfiel | <ul style="list-style-type: none"> • Updated to TRM version 2.2 • Style modifications |
| 2018-09-19 | v.48 | Martin Rohrmüller | <ul style="list-style-type: none"> • Updated to TRM version 2.1 • Updated B2B Connectors • Style modifications |
| 2018-09-17 | v.38 | Martin Rohrmüller | <ul style="list-style-type: none"> • Added power rail section • Added Rev 02 Flash PCN • Corrected table headings |
| 2018-09-17 | v.36 | Martin Rohrmüller | <ul style="list-style-type: none"> • Update to TRM version 2.0 with DrawIO Figures • Added Figure Power Distribution |
| 2018-04-04 | v.35 | Martin Rohrmüller | Corrected clock net designator in table. |
| 2017-05-28 | v.27 | Jan Kumann | <ul style="list-style-type: none"> • Board-to-Board I/O section added. • New physical dimensions images. • Documents sections rearranged. |

| | | | |
|------------|------|-------------------------------------|---|
| 2017-03-20 | v.26 | John Hartfiel | <ul style="list-style-type: none"> Notes on Clocking section. |
| 2017-01-27 | v.25 | Jan Kumann | <ul style="list-style-type: none"> New block diagram. |
| 2016-12-01 | v.17 | Jan Kumann | <ul style="list-style-type: none"> Changes in the document structure, few corrections. |
| 2016-11-18 | v.14 | Thorsten Trenz, Emmanuel Vassilakis | <ul style="list-style-type: none"> Hardware revision 02 specific changes. |
| 2016-06-01 | v.9 | Antti Lukats | <ul style="list-style-type: none"> Initial version. |

| | | | |
|----|-----|--|----|
| -- | all | <div><p>Error rendering macro 'page-info'</p><p>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p></div> | -- |
|----|-----|--|----|

Document change history

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REACH, RoHS and WEEE

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Ambiguous method overloading for method `jdk.proxy279.$Proxy4022#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`