TE0841 CPLD

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Overview

Firmware for PCB CPLD with designator U18. CPLD Device in Chain: LCMX02-256HC

Feature Summary

- Reset Management
- JTAG
- Power Management
- PUD_C
- LED

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Bank Power	Description
CPLD_IO / XIO	in	17	1.8V	FPGA Bank 45 P28

DONE	in	13	1.8V	FPGA Configuration DONE_0 Pin
EN_PL	out	20	3.3V	Enable module power
F_TCK / C_TCK	out	8	1.8V	JTAG to FPGA
F_TDI / C_TDI	out	10	1.8V	JTAG to FPGA
F_TDO / C_TDO	in	11	1.8V	JTAG to FPGA
F_TMS / C_TMS	out	9	1.8V	JTAG to FPGA
INIT_B	in	16	1.8V	FPGA INIT_B
JTAGMODE	in	26	3.3V	Enable JTAG access to CPLD for Firmware update (zero: JTAG routed to FPGA, one: CPLD access)
/ LED1	out	4	3.3V	green LED D1
N.C. / dummy	out	5	3.3V	dummy pin
nRST_SC0 / RESIN	in	21	3.3V	B2B Reset_N
PROG_B	out	12	1.8V	FPGA Configuration PROGRAM_B_0 Pin
PUDC_B	out	14	1.8V	FPGA PUDC_B
SC1		23	3.3V	B2B JM1-32 / 4x5 Boot MODE Pin / currently_not_used
SC2	inout	25	3.3V	B2B JM1-30 / 4x5 PGOOD Pin
SC3	in	27	3.3V	B2B JM1-28 / 4x5 Power Enable Pin
SC4		28	3.3V	B2B JM1-7 / 4x5 No Sequencing Pin / currently_not_used
TCK / M_TCK	in	30	3.3V	JTAG from B2B connector
TDI / M_TDI	in	32	3.3V	JTAG from B2B connector
TDO / M_TDO	out	1	3.3V	JTAG from B2B connector
TMS / M_TMS	in	29	3.3V	JTAG from B2B connector

Functional Description

JTAG

JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA can be multiplexed via JTAGEN (logical one for CPLD, logical zero for FPGA).

Power

EN_PL is set constant one.

SC2 (PGOOD) is zero conditions:

1. B2B SC3(EN1) is zero
2. PROG_B is zero, but B2B nRST_SC0 and B2B SC3(EN1) are set high. In this case PROG_B is not set high with CPLD pullup, so 1.8V is missing on CPLD IO Bank is missing.

Reset

PROG_B is set to zero if SC3(EN1) is zero or nRST_SC0 is zero, otherwise high impedance. Internal Pullup on PROG_B CPLD is enabled.

PUD_C

PUD_C is set to zero. Internal Pullup on power up, see UG570

LED

Green LED D1.

Blink Sequence	Priority	Description
********	1	B2B Reset is set to low
*****ooo	2	EN1 (power enable) is low
****oooo	3	Power problem (use PROG_B pullup to check 1.8V)
***ooooo	4	INIT_B low (CRC or IDCODE error, see UG570)
*ooooooo	5	Done is low (FPGA not programmed, see UG570)
User Defined	6	XIO is connected to LED

Appx. A: Change History and Legal Notices

Revision Changes

REV01 to REV02

- Add 4x5 Module control IOs
- Rework Power
- Rework LED

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV02	REV01, REV02	Error rendering macro 'page-info' Ambiguous method	CPLD REV02 finished, Firmware released 2018-06-05

Error rendering macro 'page-info'

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14 Mar 2018	v.3	REV01	REV01	John Hartfiel	CPLD REV01 , Firmware released 2016-11-02
2018-03-14	v.1	REV01	REV01	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk. proxy244.$Proxy3572#hasConte	Initial release

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