TE0711 CPLD

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Overview

Firmware for PCB CPLD with designator U4. CPLD Device in Chain: LCMX02-256HC

Feature Summary

- JTAG routing
- Reset
- LED sequencing
- USER IO
- I2C Interface

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name	Direction	Pin	Pullup/down	Bank Power	Description
DONE	in	13	NONE	LVCMOS33	FPGA DONE signal
EN_SC3	in	16	UP	LVCMOS33	B2B Enable Pin - low active
F_TCK	out	28	-	LVCMOS33	JTAG FPGA
F_TDI	out	27	-	LVCMOS33	JTAG FPGA
F_TDO	in	23	-	LVCMOS33	JTAG FPGA
F_TMS	out	25	-	LVCMOS33	JTAG FPGA
JTAGSEL	in	26	NONE	LVCMOS33	Enable JTAG access to CPLD for Firmware update ('0' : JTAG routed to FPGA, '1' : JTAG routed to CPLD)
MODE_SC1	in	11	UP	LVCMOS33	B2B Boot Mode Pin - currently_not_used
NOSEQ_SC4	in	12	UP	LVCMOS33	B2B NOSEQ Pin
nRST_SC0	in	8	UP	LVCMOS33	B2B Reset - low active
PG_ALL	in	10	UP	LVCMOS33	Power good - low active, from power monitor

PROG_B	out	17	NONE	LVCMOS33	FPGA PROG_B Reset
EN_1V	out	5	NONE	LVCMOS33	Power disable (U1), Module has external pullup
STAT_SC2	out	14	UP	LVCMOS33	B2B PGOOD
SYSLED4	out	9	NONE	LVCMOS33	Green LED D4
TCK_SC7	in	30	-	LVCMOS33	JTAG B2B
TDI_SC6	in	32	-	LVCMOS33	JTAG B2B
TDO_SC5	out	1	-	LVCMOS33	JTAG B2B
TMS_SC8	in	29	-	LVCMOS33	JTAG B2B
UFL	out	4	NONE	LVCMOS33	J1 (Ultra Small Sufrace Mount Coax)
UI_CLK	out	20	UP	LVCMOS18	FPGA Bank 16 Pin B8, I2C CLOCK Pin
UIO	in	21	UP	LVCMOS18	FPGA Bank 16 Pin D10, dual-purpose, I2C DATA Pin or input for UFL

Functional Description

JTAG

JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA can be multiplexed via *JTA GEN* (logical one for CPLD, logical zero for FPGA) on JM1-89.

Reset

PROG_B is triggered by *nRST_SC0* or *PG_ALL* or *EN_SC3* after power on delay.

Power

STAT_SC2 (Power Good) is '0' when *PROG_B* is '0', else high impedance.

EN_1V is high impedance. Pulled up externally. It activates the power regulators.

USER IO

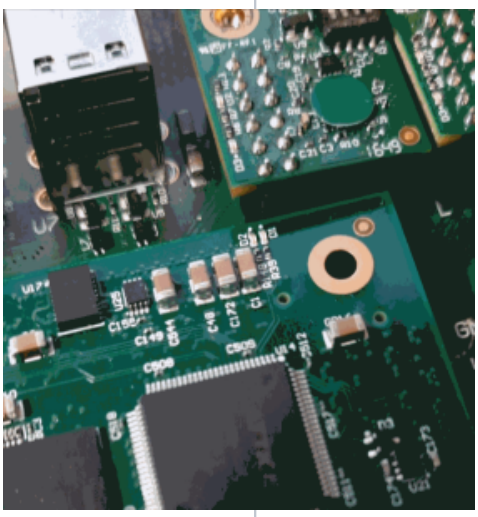
MODE_SC1 is connected to a I2C Register bit. GPIO_input(18). Its state can be read from FPGA side over I2C.

UIO is connected to *UFL* but also serves as the I2C data pin.

LED

Green LED D4 (*SYSLED4*) shows a certain blinking pattern in case one of the status signals is active, otherwise it can be controlled via I2C from FPGA side.

Blink sequence	Priority	Condition	Description

******** 	highest	nRST_SC0 = LOW (low active)	external reset from carrier is pressed
*******o			blink sequence not used
******oo			blink sequence not used
*****ooo		PG_ALL is zero	One of the power rails of the internal Voltages DCDCs is down
****oooo		EN_SC3 is zero	B2B enable Pin is active (low active), coming from the carrier
***ooooo			blink sequence not used
**oooooo			blink sequence not used
*ooooooo 		DONE = '0'	FPGA not programmed. No design on QSPI Flash?

continuously ON	lowest	software controlled command via I2C Interface. GPIO_output(1) and GPIO_output(0) high	Set bit GPIO_output(0) high to control the LED with GPIO_output(1). Both high to make it shine.
continuously OFF			If none of the above condition is met

I2C Interface

This subsystem provides 2 x 32-bit (segmented in eight 8-bit) of general purpose parallel input and output (I/O) expansion for the I2C bus protocol. Address of this I2C device is 0x20. This module contains eight 8-bit registers for reading and writing (GPIO_input[7:0] to GPIO_input[31:24] and GPIO_output[7:0] to GPIO_output[31:24]) separately with address 0x00 to 0x03. These registers can be accessed with I2C commands on a standalone application running on the Microblaze. Refer to the Hello World example application from the TE0711 reference design (test board).

Four registers can be read and four can be written.

GPIO_input(7 downto 0)	readable	0x00	contains the CPLD Firmware Revision (not the PCB revision)
GPIO_input(15 downto 8)	readable	0x01	empty
GPIO_input(23 downto 16)	readable	0x02	contains: NOSEQ_SC4 state in bit 16. STAT_SC2 in bit 17. MODE_SC1 in bit 18.
GPIO_input(31 downto 24)	readable	0x03	empty
GPIO_output(7 downto 0)	writeable	0x00	Bit 0 to 1 are mapped to SYSLED4. Write '1' to both of them to turn on the LED D4.
GPIO_output(15 downto 8)	writeable	0x01	not mapped
GPIO_output(23 downto 16)	writeable	0x02	Bit 16 is mapped to NOSEQ_SC4 if no reset ocurrs
GPIO_output(31 downto 24)	writeable	0x03	not mapped

Appx. A: Change History and Legal Notices

Revision Changes

changes Firmware REV01(old version) to REV02:

- Signals are renamed according to the schematic.
- NOSEQ pin is added.
- STAT_SC2(PGOOD) pulled up.
- JTAG signals timing corrected.
- LED function changed. Different blinking pattern for critical signal states
- MODE_SC1 is written to to I2C Interface Register GPIO_input(18)
- I2C to GPIO slave added

- CPLD_REVISION as generic parameter added
- NOSEQ_SC4 and STAT_SC2 defined as INOUT
- Pulled up or pulled down ports was controlled according to CPLD IO standardization.
- UIO and UI_CLK pins defined as I2C pins. Added PullUps for I2C. UIO and ULF functions can be used as in REV01.

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description	Firmware Release
Error r **ge-info'** Ambigu	**Error rendering macro 'page-info'** ding for method jdk.proxy241.$Proxy3496#h Ambiguous method overloading for method jdk.pr	REV02	REV02	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.pr	REV02, Firmware released 2024-01-22 **Error rendering macro 'page-info'** mission. Cannot resolve which method to invoke for [null, class java.lang.String, class Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPe	SC-PGM-TE0711-02_SC0711-02_20240123.zip
2018-03-15	v.3	REV01	REV01	John Hartfiel	REV01 , Firmware released 2015-04-17	
2018-03-15	v.1	REV01	REV01	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPe	Initial release	
	All			**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPe		

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]