TEB0911 TRM

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Overview

The Trenz Electronic TEB0911 UltraRack+ board is integrating a Xilinx Zynq UltraScale+ MPSoC with 4 GByte Flash memory for configuration and operation, DDR4-SDRAM SO-DIMM socket with 64-bit wide data bus, 22 MGT lanes and powerful switch-mode power supplies for all on-board voltages. The TEB0911 board exposes the pins of the Zynq MPSoC to accessible connectors and provides a whole range of on-board components to test and evaluate the Zynq UltraScale+ MPSoC and for developing purposes. The board is capable to be fitted to a enclosure, whereby on the enclosure's rear and front panel, I/O's, LVDS-pairs and MGT lanes are accessible through 6 on-board FMC connectors and other standard high-speed interfaces, namely USB3, SFP+, SSD, GbE, etc.

Key Features

- Zynq UltraScale+ MPSoC
  - ZU6,ZU9 or ZU15 on 1156 Pin Package
- 64bit DDR4 SODIMM (PS connected)
- M2 PCIe SSD (1-Lane)
- eMMC (bootable)
- Dual QSPI Flash (bootable)
- System Controller(LCMXO2-7000HC)
  - Power Sequencing
  - IO Expander
- Configurable PLLs
- GTH/GTP Reference CLKs

Front Panel

- 4 x FMC
  - 4 GTH per FMC
  - 68 ZynqMP PL IO per FMC
- DisplayPort (2-Lanes)
- RJ34 ETH + Dual USB3 Combo
- Dual Stack SFP+
- SD (bootable)
- Status LEDs

Back Panel

- 2 x FMC
  - 4/2 GTH
  - 12 ZynqMP PL IO per FMC
  - 56 SC IO per FMC
- USB JTAG/UART ZynqMP
- USB JTAG/GPIO FMC
- CAN FD (DB9 Connector)
- SMA (external CLK)
- 5polig 24V power connector

Additional assembly options are available for cost or performance optimization upon request.

Block Diagram

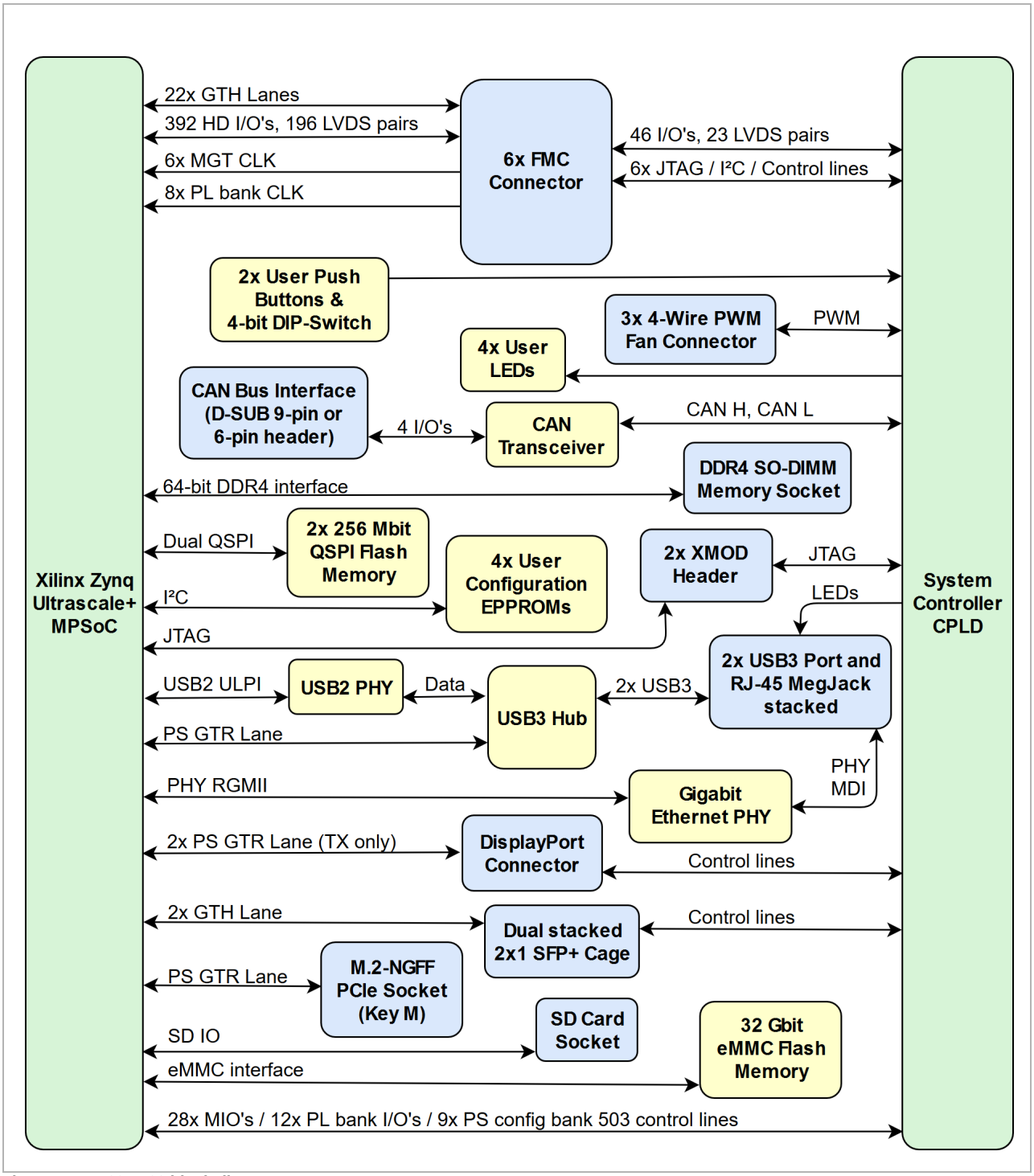


Figure 1: TEB0911-03 block diagram

Main Components

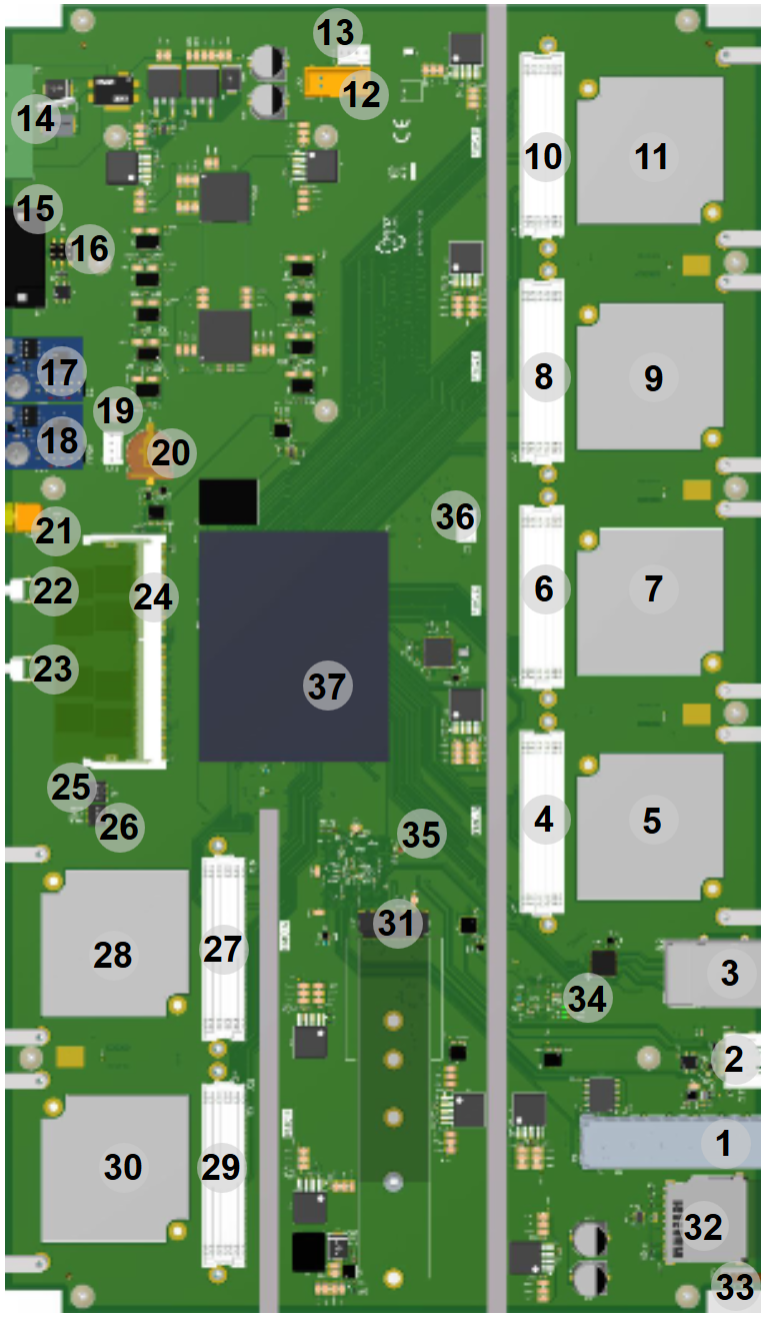


Figure 2: TEB0911-03 main components

1. SFP+ 2x1 cage with integrated LED light pipes, J9
2. DisplayPort connector, J12
3. USB3 A 2x , RJ45 1x (stacked), J13
4. FMC connector (FMC B), J4
5. FMC B cooling fan, M2
6. FMC connector (FMC C), J8

7. FMC C cooling fan, M3
8. FMC connector (FMC D), J7
9. FMC D cooling fan, M4
10. FMC connector (FMC E), J6
11. FMC E cooling fan, M5
12. I²C programming header of on-board PLL clock generator U17, J22
13. 4-Wire PWM fan connector, J23
14. Main Power Jack 24V, J1
15. CAN bus D-SUB 9-pin male connector, J3
16. CAN bus 6-pin header male, J15
17. XMOD JTAG header for access to System Controller CPLD, J35
18. XMOD JTAG header for access to Zynq MPSoC, J24
19. 4-Wire PWM fan connector, J33
20. Battery Holder CR1220, B1
21. SMA coaxial connector (PLL Si5345A U17 clock input), J25
22. Push Button, S1
23. Push Button, S2
24. DDR4 SO-DIMM socket, U3
25. 4-bit DIP-switch, S4
26. 4-bit DIP-switch, S3
27. FMC connector (FMC A), J10
28. FMC A cooling fan, M1
29. FMC connector (FMC F), J21
30. FMC F cooling fan, M6
31. NGFF M.2 PCIe socket (Key M), U2
32. SD Card socket, J11
33. User LEDs (3x green, 1x red) with LED light pipe, D13 ... D16
34. Green LEDs dedicated to USB3 hub U4, D17 ... D19
35. Red LED indicating FPGAs 'DONE' signal, D6
36. 4-Wire PWM fan connector, J2
37. Xilinx Zynq Ultrascale+ MPSoC, U1

Initial Delivery State

Storage device name	Content	Notes
User configuration EEPROMs (1x Microchip 24LC128-I/ST, 3x Microchip 24AA025E48T-I/OT)	Empty	Not programmed
USB3 HUB Configuration EEPROM (Microchip 24LC128-I/ST)	Empty	Not programmed
Si5338A programmable PLL NVM OTP	Empty	Not programmed
Si5345A programmable PLL NVM OTP	Empty	Not programmed
eMMC Flash memory	Empty	Not programmed
2x QSPI Flash memory	Empty	Not programmed

Table 1: Initial delivery state of programmable devices on the module

Boot Process

For the boot process prior to powering up the board settings must be done via DIP-Switch S3-3 and S3-4. Four boot modes can be selected:

S3-3 (SC_SW1)	S3-4 (SC_SW2)	MIO Location	Description	Notes
OFF	OFF	MIO[43:38]	SD1 Boot Mode (SD-Card on J11)	Supports SD 2.0
OFF	ON	MIO[29:26]	PJTAG0	PS JTAG connection 0 option
ON	OFF	MIO[12:0]	QSPI32	32-bit addressing, configured with dual on-board QSPI Flash Memory
ON	ON	-	JTAG	Dedicated PS interface

Table 2: Available boot modes of the on-board Zynq MPSoC

Refer also to the documentation of the SC CPLD firmware of the TEB0911 board, section 'boot mode'.

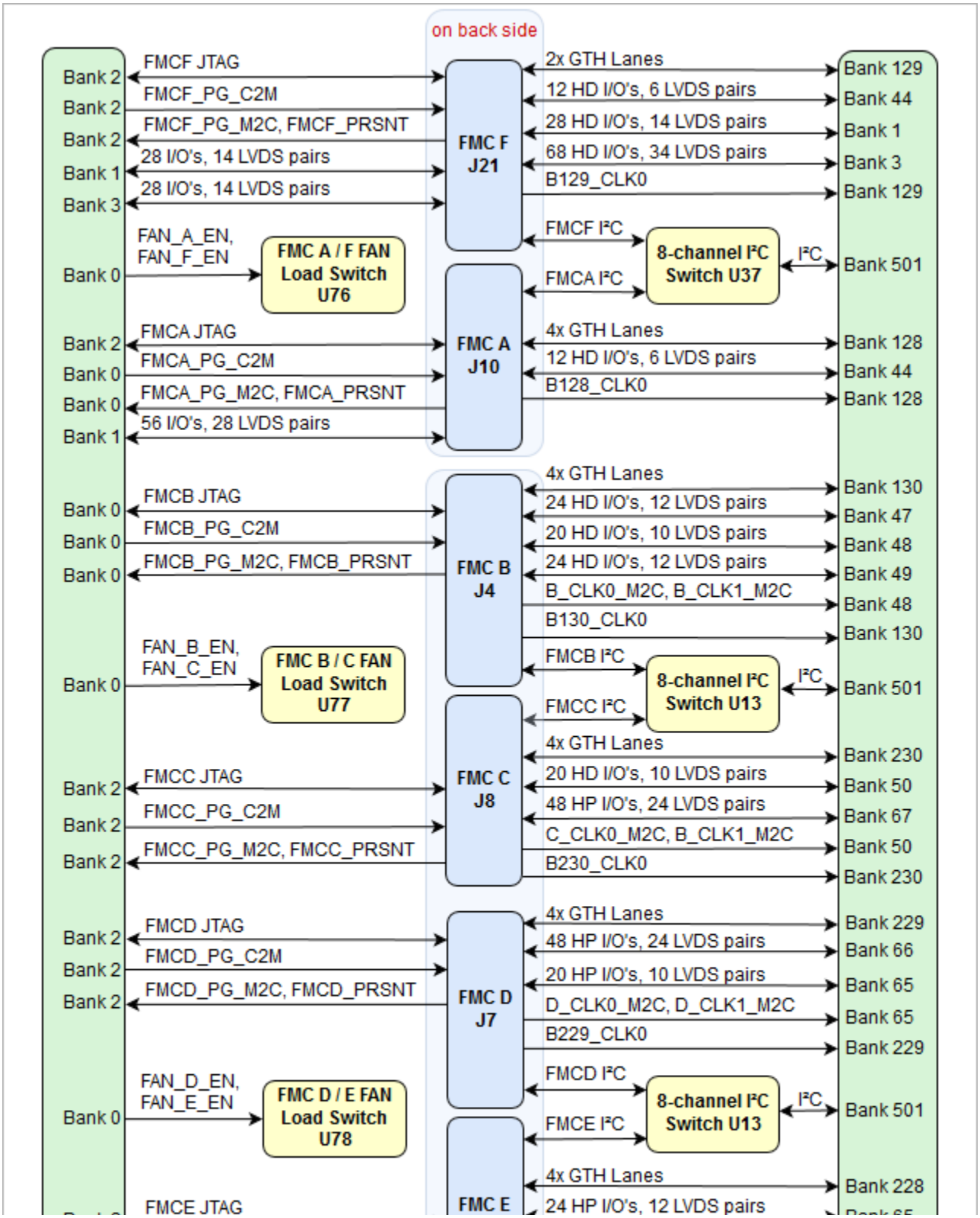
Signals, Interfaces and Pins

FMC Connectors

The TEB0911 Ultrarack+ offers 6 FMC (FPGA Mezzanine Card) connectors which provides as an ANSI/VITA 57.1 standard a modular interface to the MPSoCs FPGA and exposes numerous of its I/O pins and MGT lanes for use by other mezzanine modules and expansion cards.

The connector supports single ended and differential signaling as the I/O's are routed from the FPGA banks as LVDS-pairs to the FMC connector.

Following diagram gives an overview of the FMC connectors and their connections to the Zynq Ultrascale+ MPSoC and the System Controller CPLD U27:


on back side
FMC F J21
FMC A J10
FMC B J4
FMC C J8
FMC D J7
FMC E
FMCF JTAG
FMCF_PG_C2M
FMCF_PG_M2C, FMCF_PRSNT
28 I/O's, 14 LVDS pairs
28 I/O's, 14 LVDS pairs
2x GTH Lanes
12 HD I/O's, 6 LVDS pairs
28 HD I/O's, 14 LVDS pairs
68 HD I/O's, 34 LVDS pairs
B129_CLK0
Bank 2
Bank 2
Bank 2
Bank 1
Bank 3
Bank 129
Bank 44
Bank 1
Bank 3
Bank 129
FAN_A_EN, FAN_F_EN
FMC A / F FAN Load Switch U76
Bank 0
FMCF I²C
FMCA I²C
8-channel I²C Switch U37
I²C
Bank 501
FMCA JTAG
FMCA_PG_C2M
FMCA_PG_M2C, FMCA_PRSNT
56 I/O's, 28 LVDS pairs
4x GTH Lanes
12 HD I/O's, 6 LVDS pairs
B128_CLK0
Bank 2
Bank 0
Bank 0
Bank 1
Bank 128
Bank 44
Bank 128
FMCB JTAG
FMCB_PG_C2M
FMCB_PG_M2C, FMCB_PRSNT
4x GTH Lanes
24 HD I/O's, 12 LVDS pairs
20 HD I/O's, 10 LVDS pairs
24 HD I/O's, 12 LVDS pairs
B_CLK0_M2C, B_CLK1_M2C
B130_CLK0
Bank 0
Bank 0
Bank 0
Bank 130
Bank 47
Bank 48
Bank 49
Bank 48
Bank 130
FAN_B_EN, FAN_C_EN
FMC B / C FAN Load Switch U77
Bank 0
FMCB I²C
FMCC I²C
8-channel I²C Switch U13
I²C
Bank 501
FMCC JTAG
FMCC_PG_C2M
FMCC_PG_M2C, FMCC_PRSNT
4x GTH Lanes
20 HD I/O's, 10 LVDS pairs
48 HP I/O's, 24 LVDS pairs
C_CLK0_M2C, B_CLK1_M2C
B230_CLK0
Bank 2
Bank 2
Bank 2
Bank 230
Bank 50
Bank 67
Bank 50
Bank 230
FMCD JTAG
FMCD_PG_C2M
FMCD_PG_M2C, FMCD_PRSNT
4x GTH Lanes
48 HP I/O's, 24 LVDS pairs
20 HP I/O's, 10 LVDS pairs
D_CLK0_M2C, D_CLK1_M2C
B229_CLK0
Bank 2
Bank 2
Bank 2
Bank 229
Bank 66
Bank 65
Bank 65
Bank 229
FAN_D_EN, FAN_E_EN
FMC D / E FAN Load Switch U78
Bank 0
FMCD I²C
FMCE I²C
8-channel I²C Switch U13
I²C
Bank 501
FMCE JTAG
4x GTH Lanes
24 HP I/O's, 12 LVDS pairs
Bank 228

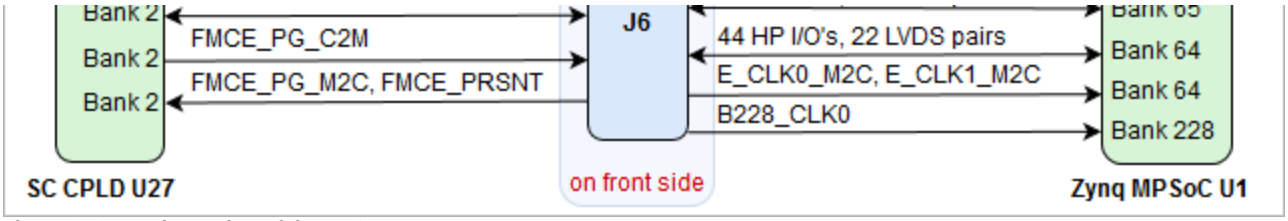


Figure 3: General overview of the FMC connectors

Following tables contains information about the interfaces, I/O's, clock and VCCIO sources available on the FMC connectors A - F:

1. FMC A
2. FMC B
3. FMC C
4. FMC D
5. FMC E
6. FMC F

FMC A

FMC A Interfaces:

FMC	Interfaces	I/O Signal Count	LVDS-pairs count	Connected to	VCCO bank Voltage	Notes
J10 (FMC A)	I/O	12	6	Bank 44 HD	FMCAF_1V8	-
		56	28	SC CPLD U27 Bank 1	FMCAF_1V8	-
	I²C	2	-	I²C-Switch U37	-	Muxed to MIO Bank 501 I²C Inteface
	JTAG	4	-	SC CPLD U27 Bank 2	3.3VSB	-
	MGT	-	8 (4 x RX/TX)	Bank 128 GTH	-	4x MGT lanes
	Clock Input	-	1	Bank 128 GTH	-	1x Reference clock input to MGT bank
	Control Signals	3	-	SC CPLD U27 Bank 0	3.3VSB	'FMCA_PG_C2M', 'FMCA_PG_M2C', 'FMCA_PRSNT'

Table 3: FMC A connector interfaces

FMC A MGT Lanes:

FMC	MGT Lane	Bank	Type	Signal Schematic Name	FMC Connector Pin	FPGA Pin
J10 (FMC A)	0	128	GTH	• B128_RX0_P • B128_RX0_N • B128_TX0_P • B128_TX0_N	J10-C6 J10-C7 J10-C2 J10-C3	MGTHRXP0_128, T33 MGTHRXN0_128, T34 MGTHTXP0_128, T29 MGTHTXN0_128, T30

	1	128	GTH	• B128_RX1_P • B128_RX1_N • B128_TX1_P • B128_TX1_N	J10-A2 J10-A3 J10-A22 J10-A23	MGTHRXP1_128, P33 MGTHRXN1_128, P34 MGTHTXP1_128, R31 MGTHTXN1_128, R32
	2	128	GTH	• B128_RX2_P • B128_RX2_N • B128_TX2_P • B128_TX2_N	J10-A6 J10-A7 J10-A26 J10-A27	MGTHRXP2_128, N31 MGTHRXN2_128, N32 MGTHTXP2_128, P29 MGTHTXN2_128, P30
	3	128	GTH	• B128_RX3_P • B128_RX3_N • B128_TX3_P • B128_TX3_N	J10-A10 J10-A11 J10-A30 J10-A31	MGTHRXP3_128, M33 MGTHRXN3_128, M34 MGTHTXP3_128, M29 MGTHTXN3_128, M30

Table 4: FMC A connector MGT lanes

FMC A Clock Signals:

FMC	Signal Schematic Name	Bank	FMC Connector Pin	FPGA Pin	Notes
J10 (FMC A)	• B128_CLK0_P • B128_CLK0_N	128	J10-D4 J10-D5	MGTREFCLK0P_128, R27 MGTREFCLK0N_128, R28	Supplied by attached module

Table 5: FMC A connector clock signal input

FMC A VCC/VCCIO:

FMC	Available VCC/VCCIO	FMC Connector Pin	Source	Notes
J10 (FMC A)	FMCA_3V3	J10-D36 J10-D38 J10-D40 J10-C39	DCDC U32, max. cur.: 5A	Enable by SC CPLD U27, bank 2, pin Y18 Signal: 'EN_A_3V3'
	3V3SB	J10-D32	DCDC U50, max. cur.: 1A	not dedicated for FMC connectors
	12V_FMC_AF	J10-C35 J10-C37	DCDC U51, max. cur.: 5A	-
	FMCAF_1V8	J10-H40 J10-G39 J10-F40 J10-E39	DCDC U39, max. cur.: 5A	Enable by SC CPLD U27, bank 2, pin W19 Signal: 'EN_AF_1V8'

Table 6: FMC A connector available VCC/VCCIO

FMC A Cooling Fan:

FMC	Fan Designator	Enable Signal	Notes
J10 (FMC A)	M1	Enable by SC CPLD U27, bank 2, pin Y19 Signal: 'FAN_A_EN'	-

Table 7: FMC A connector cooling fan

FMC F

FMC F Interfaces:

FMC	Interfaces	I/O Signal Count	LVDS-pairs count	Connected to	VCCO bank Voltage	Notes
J21 (FMC F)	I/O	12	6	Bank 44 HD	FMCAF_1V8	-
		28	14	SC CPLD U27 Bank 1	FMCAF_1V8	-
		28	14	SC CPLD U27 Bank 3	FMCAF_1V8	-
	I²C	2	-	I²C-Switch U37	-	Muxed to MIO Bank 501 I²C Inteface
	JTAG	4	-	SC CPLD U27 Bank 2	3.3VSB	-
	MGT	-	4 (2 x RX/TX)	Bank 129 GTH	-	2x MGT lanes
	Clock Input	-	1	Bank 129 GTH	-	1x Reference clock input to MGT bank
	Control Signals	3	-	SC CPLD U27 Bank 2	3.3VSB	'FMCF_PG_C2M', 'FMCF_PG_M2C', 'FMCF_PRSNT'

Table 8: FMC F connector interface

FMC F MGT Lanes:

FMC	MGT Lane	Bank	Type	Signal Schematic Name	FMC Connector Pin	FPGA Pin
J21 (FMC F)	0	129	GTH	• B129_RX0_P • B129_RX0_N • B129_TX0_P • B129_TX0_N	J21-C6 J21-C7 J21-C2 J21-C3	MGTHRXP0_129, L31 MGTHRXN0_129, L32 MGTHTXP0_129, K29 MGTHTXN0_129, K30
	1	129	GTH	• B129_RX1_P • B129_RX1_N • B129_TX1_P • B129_TX1_N	J21-A2 J21-A3 J21-A22 J21-A23	MGTHRXP1_129, K33 MGTHRXN1_129, K34 MGTHTXP1_129, J31 MGTHTXN1_129, J32

Table 9: FMC F connector MGT lanes

FMC F Clock Signals:

FMC	Signal Schematic Name	Bank	FMC Connector Pin	FPGA Pin	Notes
J21 (FMC F)	• B129_CLK0_P • B129_CLK0_N	129	J21-D4 J21-D5	MGTREFCLK0P_129, L27 MGTREFCLK0N_129, L28	Supplied by attached module

Table 10: FMC F connector clock signal input

FMC F VCC/VCCIO:

FMC	Available VCC/VCCIO	FMC Connector Pin	Source	Notes

J21 (FMC F)	FMCF_3V3	J21-D36 J21-D38 J21-D40 J21-C39	DCDC U42, max. cur.: 5A	Enable by SC CPLD U27, bank 2, pin Y10 Signal: 'EN_F_3V3'
	3V3SB	J21-D32	DCDC U50, max. cur.: 1A	not dedicated for FMC connectors
	12V_FMC_AF	J21-C35 J21-C37	DCDC U51, max. cur.: 5A	-
	FMCAF_1V8	J21-H40 J21-G39 J21-F40 J21-E39	DCDC U39, max. cur.: 5A	Enable by SC CPLD U27, bank 2, pin W19 Signal: 'EN_AF_1V8'

Table 11: FMC F connector available VCC/VCCIO

FMC F Cooling Fan:

FMC	Fan Designator	Enable Signal	Notes
J21 (FMC F)	M6	Enable by SC CPLD U27, bank 2, pin W18 Signal: 'FAN_F_EN'	-

Table 12: FMC F connector cooling fan

FMC B

FMC B Interfaces:

FMC	Interfaces	I/O Signal Count	LVDS-pairs count	Connected to	VCCO bank Voltage	Notes
J4 (FMC B)	I/O	24	12	Bank 47 HD	FMCBC_1V8	-
		20	10	Bank 48 HD	FMCBC_1V8	-
		24	12	Bank 49 HD	FMCBC_1V8	-
	I²C	2	-	I²C-Switch U13	-	Muxed to MIO Bank 501 I²C Inteface
	JTAG	4	-	SC CPLD U27 Bank 0	3.3VSB	-
	MGT	-	8 (4 x RX/TX)	Bank 130 GTH	-	4x MGT lanes
	Clock Input	-	2	Bank 48 HD	-	2x Reference clock inputs to PL bank
		-	1	Bank 130 GTH	-	1x Reference clock input to MGT bank
	Control Signals	3	-	SC CPLD U27 Bank 0	3.3VSB	'FMCB_PG_C2M', 'FMCB_PG_M2C', 'FMCB_PRSNT'

Table 13: FMC B connector interfaces

FMC B MGT Lanes:

FMC	MGT Lane	Bank	Type	Signal Schematic Name	FMC Connector Pin	FPGA Pin

J4 (FMC B)	3	130	GTH	• B130_RX3_P • B130_RX3_N • B130_TX3_P • B130_TX3_N	J4-C6 J4-C7 J4-C2 J4-C3	MGTHRXP3_130, B33 MGTHRXN3_130, B34 MGTHTXP3_130, A31 MGTHTXN3_130, A32
	2	130	GTH	• B130_RX2_P • B130_RX2_N • B130_TX2_P • B130_TX2_N	J4-A2 J4-A3 J4-A22 J4-A23	MGTHRXP2_130, C31 MGTHRXN2_130, C32 MGTHTXP2_130, B29 MGTHTXN2_130, B30
	1	130	GTH	• B130_RX1_P • B130_RX1_N • B130_TX1_P • B130_TX1_N	J4-A6 J4-A7 J4-A26 J4-A27	MGTHRXP1_130, D33 MGTHRXN1_130, D34 MGTHTXP1_130, D29 MGTHTXN1_130, D30
	0	130	GTH	• B130_RX0_P • B130_RX0_N • B130_TX0_P • B130_TX0_N	J4-A10 J4-A11 J4-A30 J4-A31	MGTHRXP0_130, E31 MGTHRXN0_130, E32 MGTHTXP0_130, F29 MGTHTXN0_130, F30

Table 14: FMC B connector MGT lanes

FMC B Clock Signals:

FMC	Signal Schematic Name	Bank	FMC Connector Pin	FPGA Pin	Notes
J4 (FMC B)	• B130_CLK0_P • B130_CLK0_N	130	J4-D4 J4-D5	MGTREFCLK0P_130, G27 MGTREFCLK0N_130, G28	Supplied by attached module
	• B_CLK0_M2C_P • B_CLK0_M2C_N	48 HD	J4-H4 J4-H5	IO_L6P_HDGC_48, F17 IO_L6N_HDGC_48, F18	Supplied by attached module
	• B_CLK1_M2C_P • B_CLK1_M2C_N	48 HD	J4-G2 J4-G3	IO_L5P_HDGC_48, G18 IO_L5N_HDGC_48, G19	Supplied by attached module

Table 15: FMC B connector clock signal input

FMC B VCC/VCCIO:

FMC	Available VCC/VCCIO	FMC Connector Pin	Source	Notes
J4 (FMC B)	FMCB_3V3	J4-D36 J4-D38 J4-D40 J4-C39	DCDC U33, max. cur.: 5A	Enable by SC CPLD U27, bank 0, pin G11 Signal: 'EN_B_3V3'
	3V3SB	J4-D32	DCDC U50, max. cur.: 1A	not dedicated for FMC connectors
	12V	J4-C35 J4-C37	DCDC U82, max. cur.: 8A	not dedicated for FMC connectors
	FMCBC_1V8	J4-H40 J4-G39 J4-F40 J4-E39	DCDC U40, max. cur.: 5A	Enable by SC CPLD U27, bank 0, pin A3 Signal: 'EN_BC_1V8'

Table 16: FMC B connector available VCC/VCCIO

FMC B Cooling Fan:

FMC	Fan Designator	Enable Signal	Notes
J4 (FMC B)	M2	Enable by SC CPLD U27, bank 0, pin A2 Signal: 'FAN_B_EN'	-

Table 17: FMC B connector cooling fan

FMC C

FMC C Interfaces:

FMC	Interfaces	I/O Signal Count	LVDS-pairs count	Connected to	VCCO bank Voltage	Notes
J8 (FMC C)	I/O	20	10	Bank 50 HD	FMCBC_1V8	-
		48	24	Bank 67 HP	FMCBC_1V8	-
	I²C	2	-	I²C-Switch U13	-	Muxed to MIO Bank 501 I²C Inteface
	JTAG	4	-	SC CPLD U27 Bank 2	3.3VSB	-
	MGT	-	8 (4 x RX/TX)	Bank 230 GTH	-	4x MGT lanes
	Clock Input	-	2	Bank 50 HD	-	2x Reference clock inputs to PL bank
		-	1	Bank 230 GTH	-	1x Reference clock input to MGT bank
	Control Signals	3	-	SC CPLD U27 Bank 2	3.3VSB	'FMCC_PG_C2M', 'FMCC_PG_M2C', 'FMCC_PRSNT'

Table 18: FMC C connector interfaces

FMC C MGT Lanes:

FMC	MGT Lane	Bank	Type	Signal Schematic Name	FMC Connector Pin	FPGA Pin
J8 (FMC C)	3	230	GTH	• B230_RX3_P • B230_RX3_N • B230_TX3_P • B230_TX3_N	J8-C6 J8-C7 J8-C2 J8-C3	MGTHRXP3_230, A4 MGTHRXN3_230, A3 MGTHTXP3_230, A8 MGTHTXN3_230, A7
	2	230	GTH	• B230_RX2_P • B230_RX2_N • B230_TX2_P • B230_TX2_N	J8-A2 J8-A3 J8-A22 J8-A23	MGTHRXP2_230, B2 MGTHRXN2_230, B1 MGTHTXP2_230, B6 MGTHTXN2_230, B5
	1	230	GTH	• B230_RX1_P • B230_RX1_N • B230_TX1_P • B230_TX1_N	J8-A6 J8-A7 J8-A26 J8-A27	MGTHRXP1_230, C4 MGTHRXN1_230, C3 MGTHTXP1_230, D6 MGTHTXN1_230, D5

	0	230	GTH	• B230_RX0_P • B230_RX0_N • B230_TX0_P • B230_TX0_N	J8-A10 J8-A11 J8-A30 J8-A31	MGTHRXP0_230, D2 MGTHRXN0_230, D1 MGTHTXP0_230, E4 MGTHTXN0_230, E3

Table 19: FMC C connector MGT lanes

FMC C Clock Signals:

FMC	Signal Schematic Name	Bank	FMC Connector Pin	FPGA Pin	Notes
J8 (FMC C)	• B230_CLK0_P • B230_CLK0_N	230	J8-D4 J8-D5	MGTREFCLK0P_230, C8 MGTREFCLK0N_230, C7	Supplied by attached module
	• C_CLK0_M2C_P • C_CLK0_M2C_N	50 HD	J8-H4 J8-H5	IO_L7P_HDGC_50, J12 IO_L7N_HDGC_50, H12	Supplied by attached module
	• C_CLK1_M2C_P • C_CLK1_M2C_N	50 HD	J8-G2 J8-G3	IO_L8P_HDGC_50, H13 IO_L8N_HDGC_50, G13	Supplied by attached module

Table 20: FMC C connector clock signal input

FMC C VCC/VCCIO:

FMC	Available VCC/VCCIO	FMC Connector Pin	Source	Notes
J8 (FMC C)	FMCC_3V3	J8-D36 J8-D38 J8-D40 J8-C39	DCDC U34, max. cur.: 5A	Enable by SC CPLD U27, bank 0, pin E11 Signal: 'EN_C_3V3'
	3V3SB	J8-D32	DCDC U50, max. cur.: 1A	not dedicated for FMC connectors
	12V	J8-C35 J8-C37	DCDC U82, max. cur.: 8A	not dedicated for FMC connectors
	FMCBC_1V8	J8-H40 J8-G39 J8-F40 J8-E39	DCDC U40, max. cur.: 5A	Enable by SC CPLD U27, bank 0, pin A3 Signal: 'EN_BC_1V8'

Table 21: FMC C connector available VCC/VCCIO

FMC C Cooling Fan:

FMC	Fan Designator	Enable Signal	Notes
J8 (FMC C)	M3	Enable by SC CPLD U27, bank 0, pin B3 Signal: 'FAN_C_EN'	-

Table 22: FMC C connector cooling fan

FMC D

FMC D Interfaces:

FMC	Interfaces	I/O Signal Count	LVDS-pairs count	Connected to	VCCO bank Voltage	Notes
J7 (FMC D)	I/O	20	10	Bank 65 HP	FMCDE_1V8	-
		48	24	Bank 66 HP	FMCDE_1V8	-
	I²C	2	-	I²C-Switch U13	-	Muxed to MIO Bank 501 I²C Inteface
	JTAG	4	-	SC CPLD U27 Bank 2	3.3VSB	-
	MGT	-	8 (4 x RX/TX)	Bank 229 GTH	-	4x MGT lanes
	Clock Input	-	2	Bank 65 HP	-	2x Reference clock inputs to PL bank
		-	1	Bank 229 GTH	-	1x Reference clock input to MGT bank
	Control Signals	3	-	SC CPLD U27 Bank 2	3.3VSB	'FMCD_PG_C2M', 'FMCD_PG_M2C', 'FMCD_PRSNT'

Table 23: FMC D connector interfaces

FMC D MGT Lanes:

FMC	MGT Lane	Bank	Type	Signal Schematic Name	FMC Connector Pin	FPGA Pin
J7 (FMC D)	3	229	GTH	• B229_RX3_P • B229_RX3_N • B229_TX3_P • B229_TX3_N	J7-C6 J7-C7 J7-C2 J7-C3	MGTHRXP3_229, F2 MGTHRXN3_229, F1 MGTHTXP3_229, F6 MGTHTXN3_229, F5
	2	229	GTH	• B229_RX2_P • B229_RX2_N • B229_TX2_P • B229_TX2_N	J7-A2 J7-A3 J7-A22 J7-A23	MGTHRXP2_229, H2 MGTHRXN2_229, H1 MGTHTXP2_229, G4 MGTHTXN2_229, G3
	1	229	GTH	• B229_RX1_P • B229_RX1_N • B229_TX1_P • B229_TX1_N	J7-A6 J7-A7 J7-A26 J7-A27	MGTHRXP1_229, J4 MGTHRXN1_229, J3 MGTHTXP1_229, H6 MGTHTXN1_229, H5
	0	229	GTH	• B229_RX0_P • B229_RX0_N • B229_TX0_P • B229_TX0_N	J7-A10 J7-A11 J7-A30 J7-A31	MGTHRXP0_229, K2 MGTHRXN0_229, K1 MGTHTXP0_229, K6 MGTHTXN0_229, K5

Table 24: FMC D connector MGT lanes

FMC D Clock Signals:

FMC	Signal Schematic Name	Bank	FMC Connector Pin	FPGA Pin	Notes
J7 (FMC D)	• B229_CLK0_P • B229_CLK0_N	229	J7-D4 J7-D5	MGTREFCLK0P_229, G8 MGTREFCLK0N_229, G7	Supplied by attached module

	• D_CLK0_M2C_P • D_CLK0_M2C_N	65 HP	J7-H4 J7-H5	IO_L14P_T2L_N2_GC_65, AG5 IO_L14N_T2L_N3_GC_65, AG4	Supplied by attached module
	• D_CLK1_M2C_P • D_CLK1_M2C_N	65 HP	J7-G2 J7-G3	IO_L13P_T2L_N0_GC_QBC_65, AE5 IO_L13N_T2L_N1_GC_QBC_65, AF5	Supplied by attached module

Table 25: FMC D connector clock signal input

FMC D VCC/VCCIO:

FMC	Available VCC/VCCIO	FMC Connector Pin	Source	Notes
J7 (FMC D)	FMCD_3V3	J7-D36 J7-D38 J7-D40 J7-C39	DCDC U35, max. cur.: 5A	Enable by SC CPLD U27, bank 0, pin F8 Signal: 'EN_D_3V3'
	3V3SB	J7-D32	DCDC U50, max. cur.: 1A	not dedicated for FMC connectors
	12V	J7-C35 J7-C37	DCDC U82, max. cur.: 8A	not dedicated for FMC connectors
	FMCDE_1V8	J7-H40 J7-G39 J7-F40 J7-E39	DCDC U41, max. cur.: 5A	Enable by SC CPLD U27, bank 0, pin C5 Signal: 'EN_DE_1V8'

Table 26: FMC D connector available VCC/VCCIO

FMC D Cooling Fan:

FMC	Fan Designator	Enable Signal	Notes
J7 (FMC D)	M4	Enable by SC CPLD U27, bank 0, pin D7 Signal: 'FAN_D_EN'	-

Table 27: FMC D connector cooling fan

FMC E

FMC E Interfaces:

FMC	Interfaces	I/O Signal Count	LVDS-pairs count	Connected to	VCCO bank Voltage	Notes
J6 (FMC E)	I/O	24	12	Bank 65 HP	FMCDE_1V8	-
		44	22	Bank 64 HP	FMCDE_1V8	-
	I²C	2	-	I²C-Switch U13	-	Muxed to MIO Bank 501 I²C Inteface
	JTAG	4	-	SC CPLD U27 Bank 2	3.3VSB	-
	MGT	-	8 (4 x RX/TX)	Bank 228 GTH	-	4x MGT lanes
	Clock Input	-	2	Bank 64 HP	-	2x Reference clock inputs to PL bank
		-	1	Bank 228 GTH	-	1x Reference clock input to MGT bank

	Control Signals	3	-	SC CPLD U27 Bank 2	3.3VSB	'FMCE_PG_C2M', 'FMCE_PG_M2C', 'FMCE_PRSNT'

Table 28: FMC E connector interfaces

FMC E MGT Lanes:

FMC	MGT Lane	Bank	Type	Signal Schematic Name	FMC Connector Pin	FPGA Pin
J6 (FMC E)	3	228	GTH	• B228_RX3_P • B228_RX3_N • B228_TX3_P • B228_TX3_N	J6-C6 J6-C7 J6-C2 J6-C3	MGTHRXP3_228, L4 MGTHRXN3_228, L3 MGTHTXP3_228, M6 MGTHTXN3_228, M5
	2	228	GTH	• B228_RX2_P • B228_RX2_N • B228_TX2_P • B228_TX2_N	J6-A2 J6-A3 J6-A22 J6-A23	MGTHRXP2_228, M2 MGTHRXN2_228, M1 MGTHTXP2_228, N4 MGTHTXN2_228, N3
	1	228	GTH	• B228_RX1_P • B228_RX1_N • B228_TX1_P • B228_TX1_N	J6-A6 J6-A7 J6-A26 J6-A27	MGTHRXP1_228, P2 MGTHRXN1_228, P1 MGTHTXP1_228, P6 MGTHTXN1_228, P5
	0	228	GTH	• B228_RX0_P • B228_RX0_N • B228_TX0_P • B228_TX0_N	J6-A10 J6-A11 J6-A30 J6-A31	MGTHRXP0_228, T2 MGTHRXN0_228, T1 MGTHTXP0_228, R4 MGTHTXN0_228, R3

Table 29: FMC E connector MGT lanes

FMC E Clock Signals:

FMC	Signal Schematic Name	Bank	FMC Connector Pin	FPGA Pin	Notes
J6 (FMC E)	• B228_CLK0_P • B228_CLK0_N	228	J6-D4 J6-D5	MGTREFCLK0P_228, L8 MGTREFCLK0N_228, L7	Supplied by attached module
	• E_CLK0_M2C_P • E_CLK0_M2C_N	64 HP	J6-H4 J6-H5	IO_L12P_T1U_N10_GC_64, AL8 IO_L12N_T1U_N11_GC_64, AL7	Supplied by attached module
	• E_CLK1_M2C_P • E_CLK1_M2C_N	64 HP	J6-G2 J6-G3	IO_L11P_T1U_N8_GC_64, AK8 IO_L11N_T1U_N9_GC_64, AK7	Supplied by attached module

Table 30: FMC E connector clock signal input

FMC E VCC/VCCIO:

FMC	Available VCC/VCCIO	FMC Connector Pin	Source	Notes

J6 (FMC E)	FMCE_3V3	J6-D36 J6-D38 J6-D40 J6-C39	DCDC U36, max. cur.: 5A	Enable by SC CPLD U27, bank 0, pin E8 Signal: 'EN_E_3V3'
	3V3SB	J6-D32	DCDC U50, max. cur.: 1A	not dedicated for FMC connectors
	12V	J6-C35 J6-C37	DCDC U82, max. cur.: 8A	not dedicated for FMC connectors
	FMCDE_1V8	J6-H40 J6-G39 J6-F40 J6-E39	DCDC U41, max. cur.: 5A	Enable by SC CPLD U27, bank 0, pin C5 Signal: 'EN_DE_1V8'

Table 31: FMC E connector available VCC/VCCIO

FMC E Cooling Fan:

FMC	Fan Designator	Enable Signal	Notes
J6 (FMC E)	M5	Enable by SC CPLD U27, bank 0, pin D6 Signal: 'FAN_E_EN'	-

Table 32: FMC E connector cooling fan

XMOD JTAG Interface

JTAG access to the Zynq MPSoC and SC CPLD is provided through XMOD header J24 and J35:

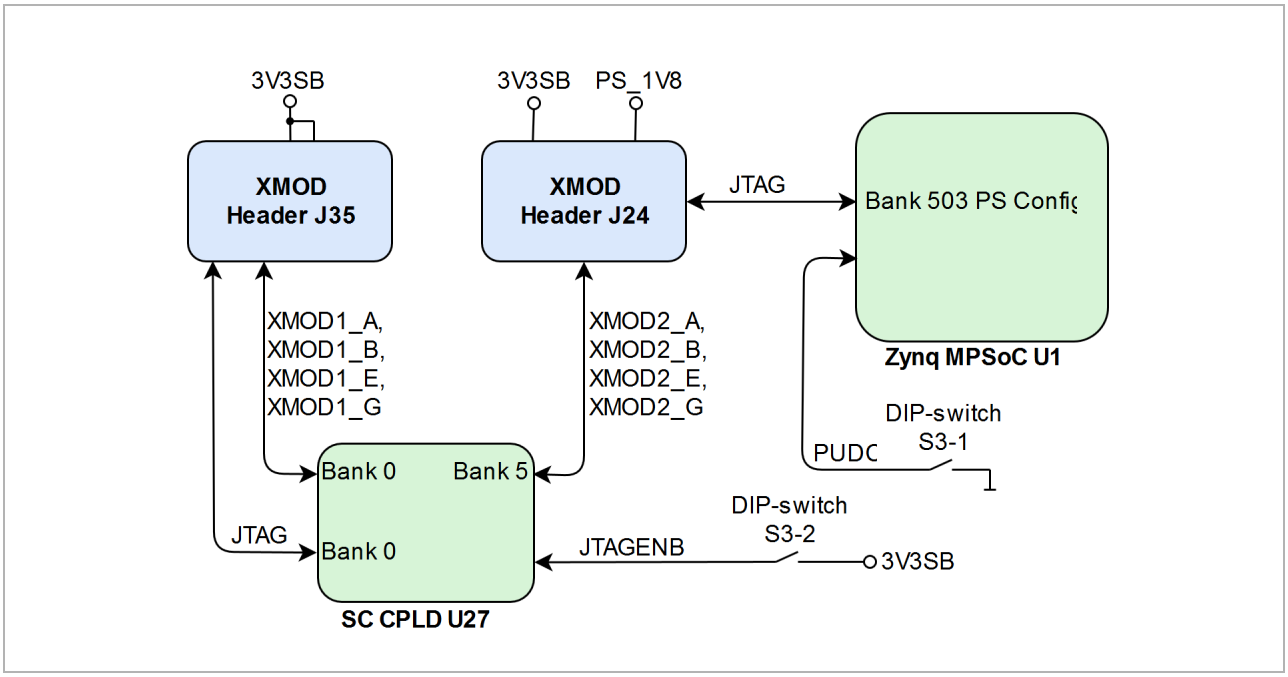


Figure 4: XMOD header J24 and J35

Signal Assignment of XMOD header J24 and J35

Connector	Interface	Signal Schematic Name	XMOD Header Pin	Connected to	VCCIO	VCC
XMOD Header J24	JTAG	• F_TCK	J24-4	Bank 503 PS Config, Pin R25	PS_1V8	3V3SB
		• F_TDI	J24-10	Bank 503 PS Config, Pin U25		
		• F_TDO	J24-8	Bank 503 PS Config, Pin T25		
		• F_TMS	J24-12	Bank 503 PS Config, Pin R24		
	GPIO/ UART	• XMOD2_A	J24-3	SC CPLD U27, bank 5, Pin K7		
		• XMOD2_B	J24-7	SC CPLD U27, bank 5, Pin K6		
		• XMOD2_E	J24-9	SC CPLD U27, bank 5, Pin H7		
		• XMOD2_G	J24-11	SC CPLD U27, bank 5, Pin H6		
XMOD Header J35	JTAG	• C_TCK	J35-4	SC CPLD U27, bank 0, Pin A8	3V3SB	
		• C_TDI	J35-10	SC CPLD U27, bank 0, Pin C7		
		• C_TDO	J35-8	SC CPLD U27, bank 0, Pin A6		
		• C_TMS	J35-12	SC CPLD U27, bank 0, Pin C9		
	GPIO/ UART	• XMOD1_A	J35-3	SC CPLD U27, bank 0, Pin B19		
		• XMOD1_B	J35-9	SC CPLD U27, bank 0, Pin A17		
		• XMOD1_E	J35-7	SC CPLD U27, bank 0, Pin C17		
		• XMOD1_G	J35-11	SC CPLD U27, bank 0, Pin A18		

Table 33: XMOD interface signals

The JTAG interfaces of the TEB0911 UltraRack board can accessed with the XMOD-FT2232H adapter-board TE0790. The on-board devices Zynq MPSoC U1 and SC CPLD U27 can be programmed via USB2.0 interface of the TE0790 programmer.

XMOD-Header J24 is designated to program the Zynq Ultrascale+ MPSoC via USB interface, the 4 GPIO/UART pins (XMOD2_A/B/E/G) of this header are routed to the System Controller CPLD U27.

XMOD-Header J35 is designated to program the System Controller CPLD U27 via USB interface, the 4 GPIO/UART pins (XMOD1_A/B/E/G) of this header are also routed to the System Controller CPLD U27.
To program the System Controller CPLD, the JTAG interface of this devices have to be activated by DIP-switch S3-2. J35 JTAG is used for FMC JTAG, is JTAGENB is low (see CPLD Firmware).

When using XMOD FTDI JTAG Adapter TE0790, the adapter-board's VCC and VCCIO on both headers J24 and J35 will be sourced by the on-board supply voltages. Set the XMOD DIP-switch with the setting:

XMOD DIP-switches	Position
Switch 1	ON
Switch 2	OFF
Switch 3	OFF
Switch 4	OFF

Table 34: XMOD adapter board DIP-switch positions for voltage configuration

> ⚠ Use Xilinx compatible TE0790 adapter board (designation TE-0790-xx without 'L') to program the Xilinx Zynq devices.
>
> The TE0790 adapter board's CPLD have to be configured with the **Standard** variant of the firmware. Refer to the TE0790 Resources Site for further information and firmware download.

Gigabit Ethernet Interface

On-board Gigabit Ethernet PHY is provided with Marvell Alaska 88E1512 IC U20. The Ethernet PHY RGMII interface is connected to the Zynq MPSoC Ethernet interface of the PS MIO bank 502. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from the on-board 25.000000 MHz oscillator U21. The LEDs of the RJ-45 MegJack J13 are connected to the System Controller CPLD bank 2, pins Y12, Y13 and Y14.

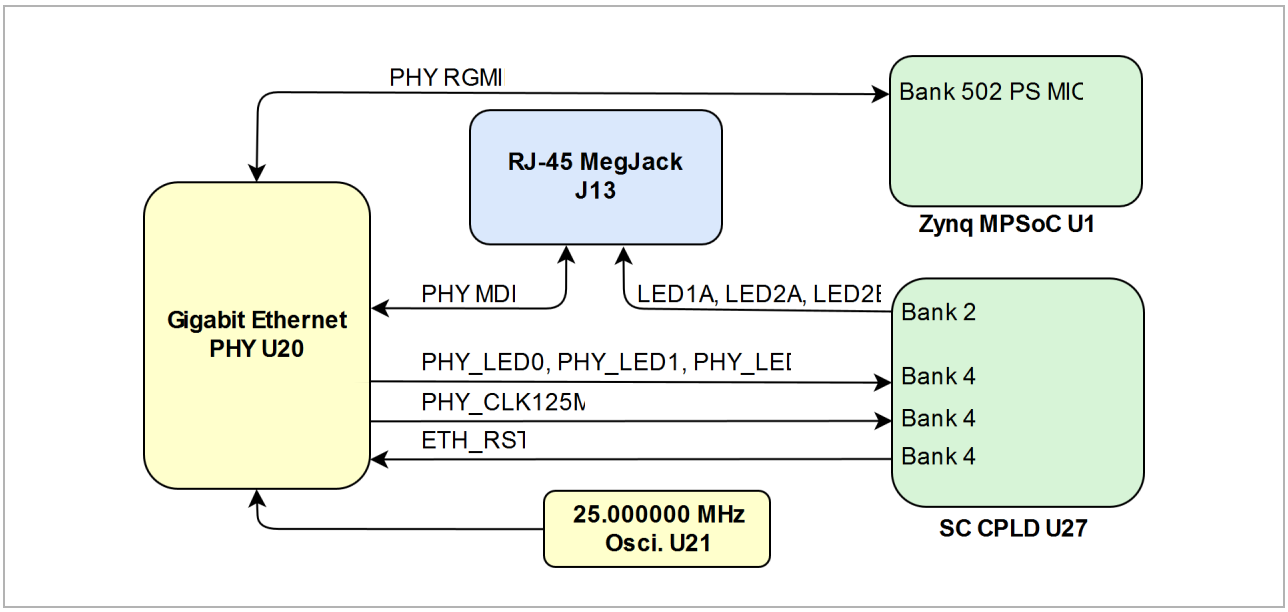


Figure 5: Gigabit Ethernet interface

Following table describes the signals and control lines of the Gigabit Ethernet interface of the board:

PHY Pin	Connected to	Notes
MDC/MDIO	PS bank 502 MIO76, MIO77	-
PHY LED0..2	SC CPLD U27, bank 4, pin L5, L1, K1	see schematic for details, forwarded to RJ45 GbE MagJack J7
PHY_CLK125M	SC CPLD U27, bank 4, pin K2	125 MHz Ethernet PHY clock out
CONFIG	pulled up to PS_1V8	Configuration of PHY address LSB and VDDO level
RESETn	SC CPLD U27, bank 4, pin L6	Active low reset line
RGMII	PS bank 502 MIO64 ... MIO75	Reduced Gigabit Media Independent Interface
SGMII	-	Serial Gigabit Media Independent Interface
MDI	RJ45 GbE MagJack J13	Media Dependent Interface

Table 35: Ethernet PHY interface connections

USB3 Interface

On the TEB0911 board two USB3 Superspeed ports are available to the user, which are downward compatible to USB2 Highspeed.

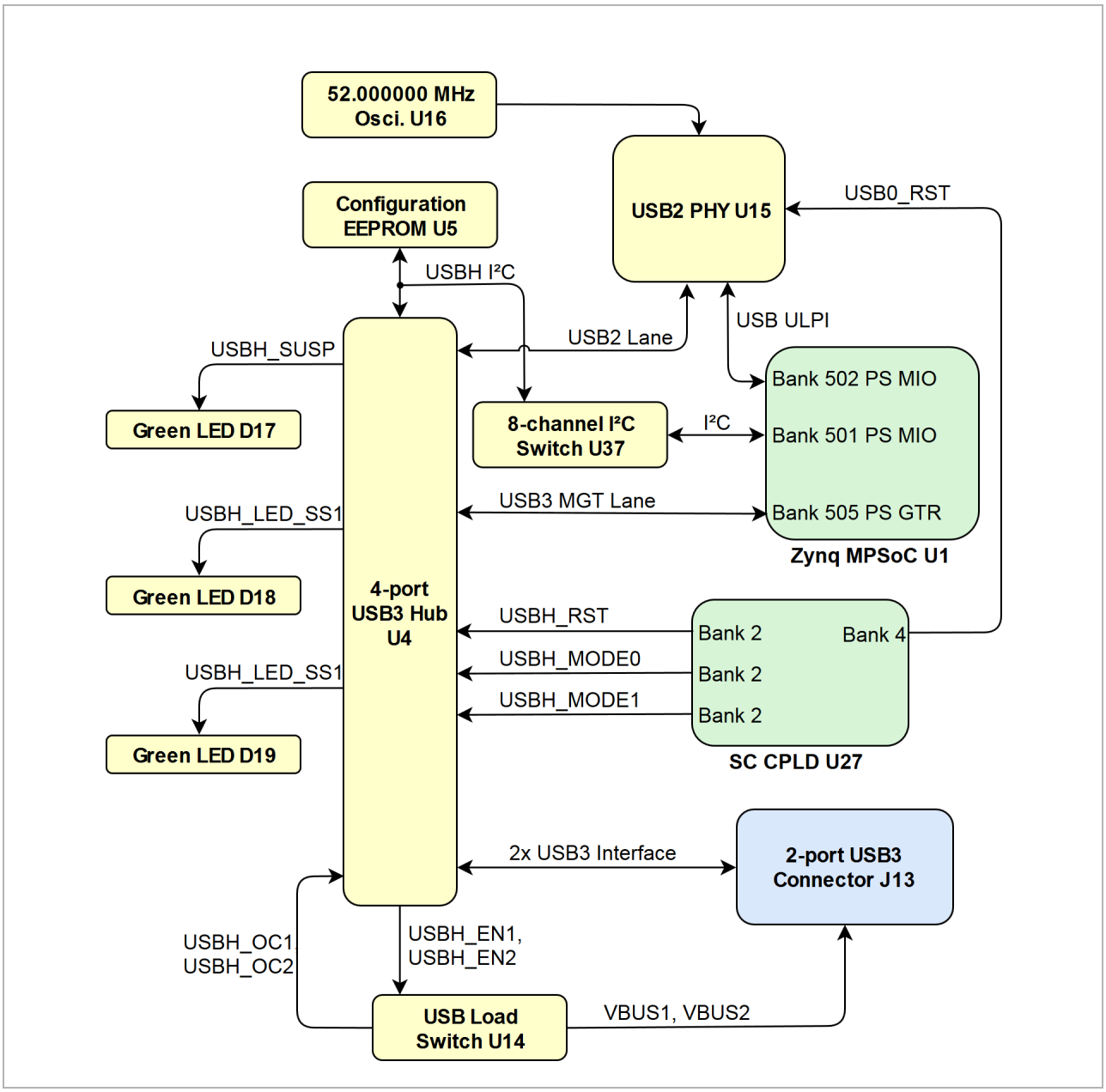


Figure 6: USB3 interface

The 4-port USB3 hub is connected to the Zynq MPSoC's PS GTR bank, the USB2 PHY is connected to the PS MIO bank 502:

IC	Interface	Signal Schematic Names	Connected to	Notes

USB3 Hub U4	USB3 Upstream MGT lane	• B505_TX1_P • B505_TX1_N • B505_RX1_P • B505_RX1_N	PS_MGTRTXP1_505, Y29 PS_MGTRTXN1_505, Y30 PS_MGTRRXP1_505, AA31 PS_MGTRTXN1_505, AA32	-
	USB2 Uptream data LVDS pair	• USB0_D_P • USB0_D_N	USB2 PHY U15 Pins: 18,19	-
	USB3 Downstream lane	• USB3_RXDN1_D_P • USB3_RXDN1_D_N • USB3_TXDN1_D_P • USB3_TXDN1_D_N • USB3_RXDN2_D_P • USB3_RXDN2_D_N • USB3_TXDN2_D_P • USB3_TXDN2_D_N	2-port USB3 A / RJ-45 connector (stacked) J13	-
	USB2 Downstream LVDS pair	• USB2_DN1_D_P • USB2_DN1_D_N • USB2_DN2_D_P • USB2_DN2_D_N	2-port USB3 A / RJ-45 connector (stacked) J13	-
	I²C	• USBH_SDA • USBH_SCL	USB3 hub U4 Configuration EEPROM U5, 8-channel I²C-switch U37	-
	Control Lines	• USBH_MODE0, • USBH_MODE1 • USBH_RST	SC CPLD U27, bank 2 Pins: Y17, Y16, Y15	-
USB2 PHY U15	USB2 ULPI	• USB0_STP • USB0_NXT • USB0_DIR • USB0_CLK • USB0_DATA0 ... USB0_DATA7	PS bank 502 Pins: MIO52 ... MIO63	-
	USB2 data LVDS pair	• USB0_D_P • USB0_D_N	USB3 Hub U4 Pins: 71,72	-
	Control Lines	• USB0_RST	SC CPLD U27, bank 4 Pin: M2	-

Table 36: USB3 signals and interfaces

SFP+ Interface

The TEB0911 board provides the high speed MGT interface connectors "SFP+" (Enhanced small form-factor pluggable) with data transmission rates up to 10 Gbit/s.

Block diagram below shows the dependencies between the implied devices which establish the SFP+ interface:

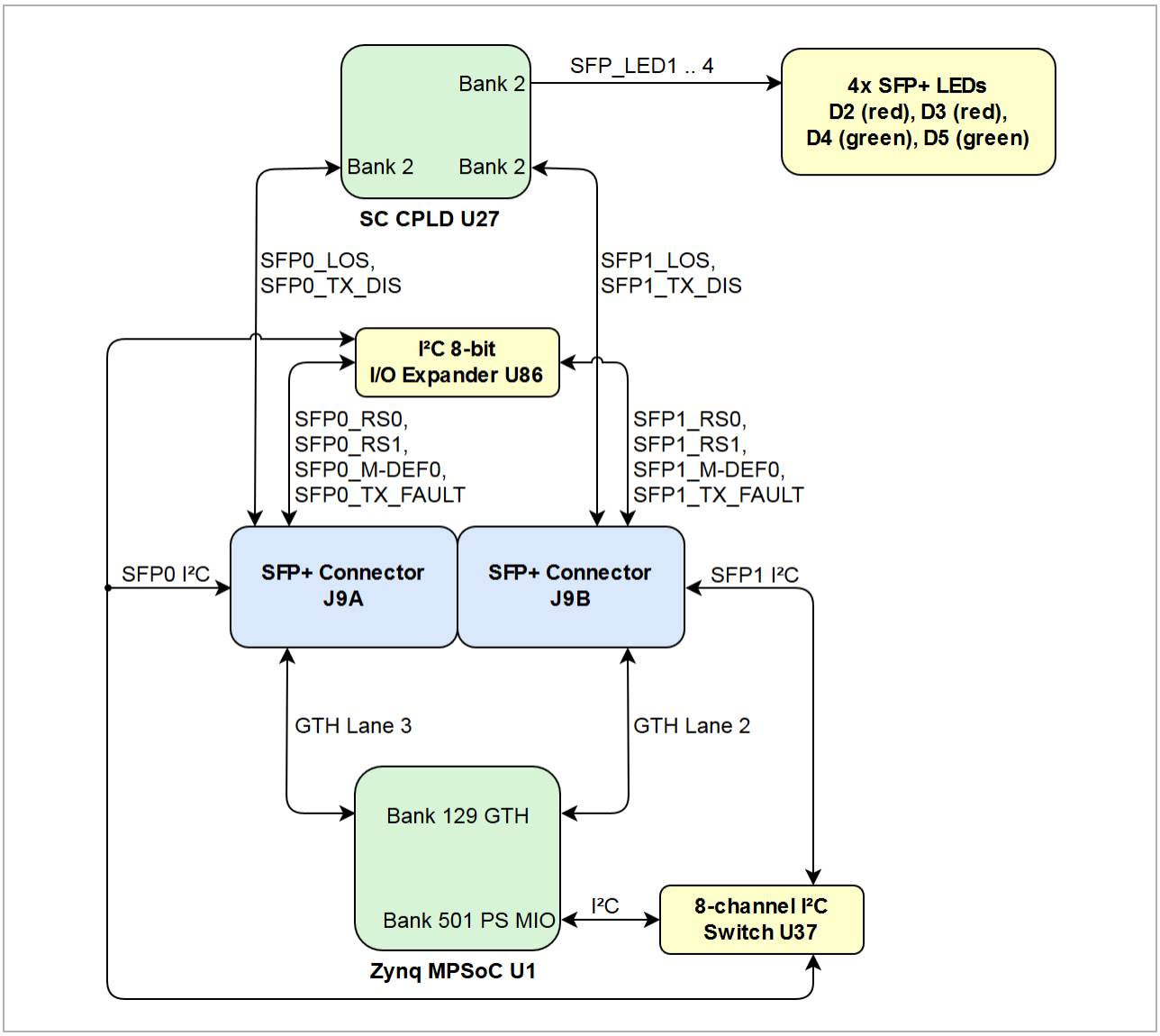


Figure 7: SFP+ interface

Connector	Interface	Signal Schematic Name	Connected to	Logic	Notes
SFP+ J9A	MGT Lane	• B129_TX3_P • B129_TX3_N • B129_RX3_P • B129_RX3_N	MGTHTXP3_129, G31 MGTHTXN3_129, G32 MGTHRXP3_129, F33 MGTHRXN3_129, F34	TX: Output RX: Input	Multi gigabit highspeed data lane
	I²C	• SFP0_SDA • SFP0_SCL	8-channel I²C-switch U37	BiDir	2-wire Serial Interface

	Control Lines	• SFP0_RS0	I²C 8-bit I/O Port-Expander U86	Output, low active	Full RX bandwidth
		• SFP0_RS1		Output, low active	Reduced RX bandwidth
		• SFP0_M-DEF0		Input, low active	Module present / not present
		• SFP0_TX_FAULT		Input, high active	Fault / Normal Operation
		• SFP0_LOS	SC CPLD U27, bank 2, pin V8	Input, high active	Loss of receiver signal
		• SFP0_TX_DIS	SC CPLD U27, bank 2, pin Y7	Output, low active	SFP Enabled / Disabled
SFP+ J9B	MGT Lane	• B129_TX2_P • B129_TX2_N • B129_RX2_P • B129_RX2_N	MGTHTXP2_129, H29 MGTHTXN2_129, H30 MGTHRXP2_129, H33 MGTHRXN2_129, H34	TX: Output RX: Input	Multi gigabit highspeed data lane
	I²C	• SFP1_SDA • SFP1_SCL	8-channel I²C-switch U37	Bidir	2-wire Serial Interface
	Control Lines	• SFP1_RS0	I²C 8-bit I/O Port-Expander U86	Output, low active	Full RX bandwidth
		• SFP1_RS1		Output, low active	Reduced RX bandwidth
		• SFP1_M-DEF0		Input, low active	Module present / not present
		• SFP1_TX_FAULT		Input, high active	Fault / Normal Operation
		• SFP1_LOS	SC CPLD U27, bank 2, pin W7	Input, high active	Loss of receiver signal
		• SFP1_TX_DIS	SC CPLD U27, bank 2, pin V7	Output. low active	SFP Enabled / Disabled

Table 37: SFP+ signals and interfaces

SSD Interface

On the TEB0911 UltraRack board one SSD interface is available provided by a NGFF (Next Generation Form Faktor) M.2 socket (Key M) which supports data transmission rates for PCIe3, SATA3 and USB3 interfaces.

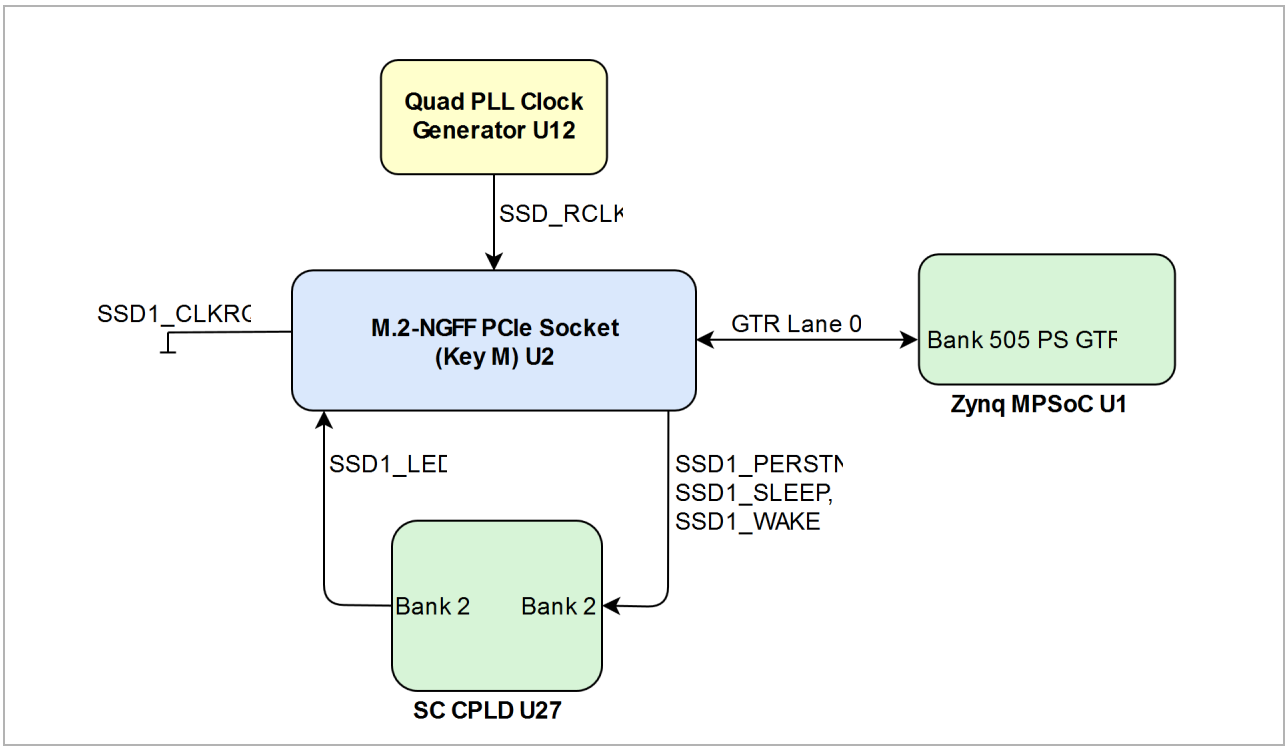


Figure 8: SSD interface

Connector	Interface	Signal Schematic Name	Connected to	Notes
M.2-NGFF PCIe Socket U2	MGT Lane	• B505_TX0_P • B505_TX0_N • B505_RX0_P • B505_RX0_N	PS_MGTRTXP0_505, AB29 PS_MGTRTXN0_505, AB30 PS_MGTRRXP0_505, AB33 PS_MGTRTXN0_505, AB34	Multi gigabit highspeed data lane TX: Output RX: Input
	Clock Input	• SSD_RCLK_P • SSD_RCLK_N	Quad programmable PLL clock generator U12, CLK0	Reference clock signal
	Control Lines	• SSD1_LED	SC CPLD U27, bank 2, pin AA13	LED, Output, High active
		• SSD1_SLEEP	SC CPLD U27, bank 2, pin AA12	PCIe sleep state, Input, Low active
		• SSD1_PERSTN	SC CPLD U27, bank 2, pin AA11	PCIe reset, Input, Low active
		• SSD1_WAKE	SC CPLD U27, bank 2, pin AB11	PCIe Link reactivation, Input, Low active
		• SSD1_CLKRQ	connect to GND	PCIe Clock Request, Low active

Table 38: SSD signals and interfaces

DisplayPort Interface

The TEB0911 board provides the high speed DisplayPort interface for visual output. The DisplayPort is connected with two transmit LVDS-pairs of bank 505 PS GTR lanes. Additionally the auxiliary transmit line is established by the SC CPLD in conjunction with a LVDS Line Driver/Receiver.

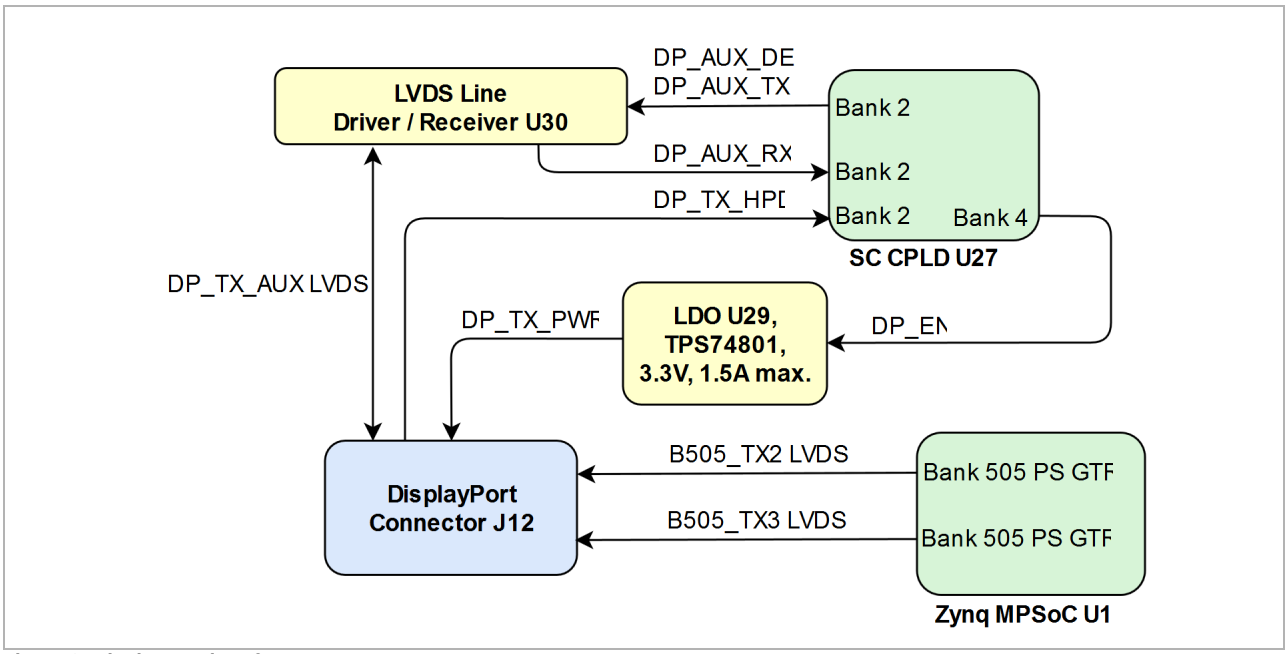


Figure 9: DisplayPort interface

Follwowing table contains a brief description of the MGT lanes and control and status signals of the DisplayPort interface:

Connector	Interface	Signal Schematic Name	Connected to	Notes
DisplayPort Connector J12	MGT Lane	• B505_TX2_P • B505_TX2_N • B505_TX3_P • B505_TX3_N	PS_MGTRTXP2_505, W31 PS_MGTRTXN2_505, W32 PS_MGTRTXP3_505, V29 PS_MGTRTXN3_505, V30	Multi gigabit highspeed data lane (only transmit pairs) TX: Output RX: Input
	Auxiliary Line	• DP_TX_AUX_P • DP_TX_AUX_N	LVDS Line Driver/Receiver, U30	Convert signal from single ended to LVDS Single ended signals: 'DP_AUX_TX', 'DP_AUX_RX', SC CPLD U27, bank 2, pins AA14, AB12
	Control Lines	• DP_TX_HPD	SC CPLD U27, bank 2, pin AA15	DisplayPort Hot Plug Detect
		• DP_EN	LDO U29	3.3V Supply Voltage for DisplayPort

Table 39: DisplayPort signals and interfaces

DDR4 Memory Socket

On the TEB0911 board there is a DDR4 memory interface with a 64-bit databus width available for SO-DIMM modules.

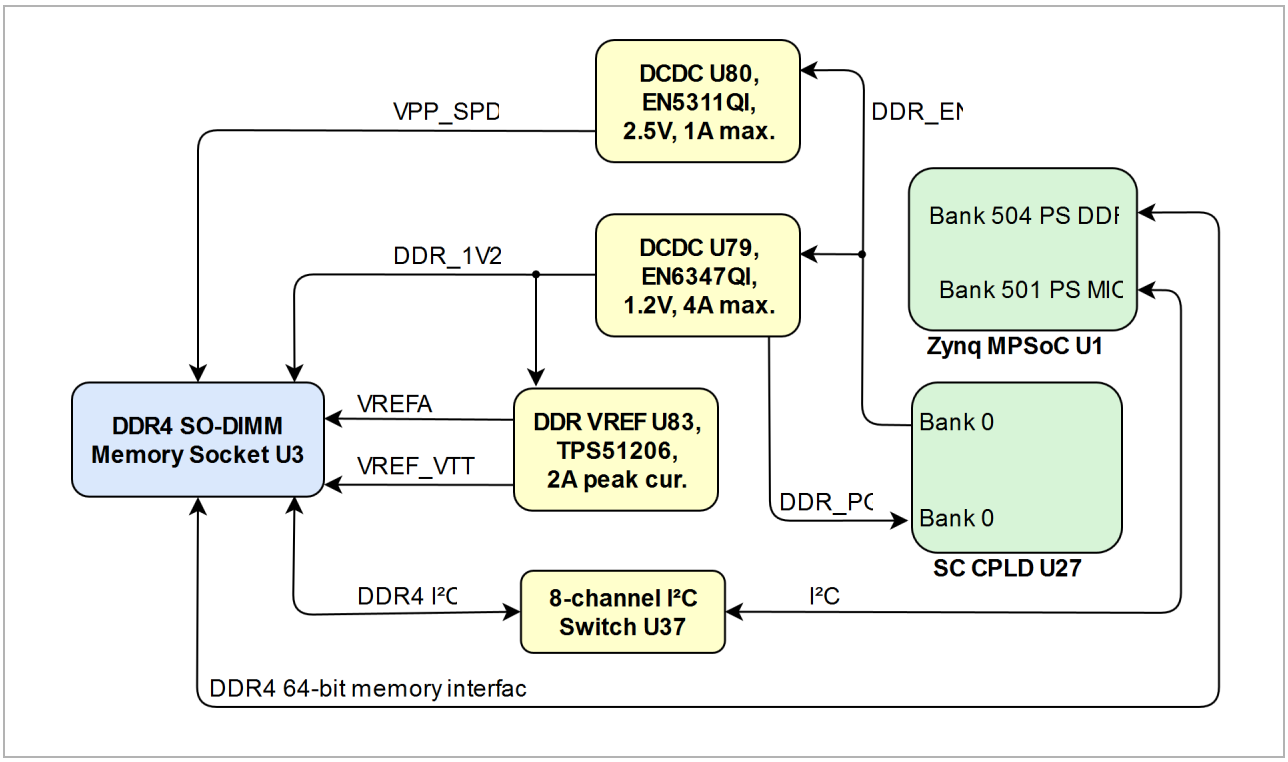


Figure 10: DDR4 memory interface

Following table gives an overview about the I/O signals of the DDR4 SDRAM memory interface:

Connector	DDR4 SDRAM I/O Signal	Signal Schematic Name	Connected to	Notes
DDR4 SO-DIMM Socket U13	Address inputs	• DDR4-A0 ... DDR4-A16	PS DDR Bank 504	-
	Bank address inputs	• DDR4-BA0 / DDR4-BA1		-
	Bank group inputs	• DDR4-BG0 / DDR4-BG1		-
	Differential clocks	• DDR4-CLK0_P • DDR4-CLK0_N • DDR4-CLK1_P • DDR4-CLK1_N		2 x DDR4 clock
	Data input/output	• DQ0 ... DQ63		-
	Check bit input/output	• CB0 ... CB7		-

	Data strobe (differential)	• DDR4-DQS0_P • DDR4-DQS0_N • ... • DDR4-DQS8_P • DDR4-DQS8_N		-
	Data mask and data bus inversion	• DDR4-DM0 ... DDR4-DM8		-
	Serial address inputs	• DDR4-SA0 ... DDR4-SA2		address range configuration on I²C bus
	Control Signals	• DDR4-CS_N0 / DDR4-CS_N1		chip selest signal
		• DDR4-ODT0 / DDR4-ODT1		On-die termination enable
		• DDR4-RESET		nRESET
		• DDR4-PAR		Command and address parity input
		• DDR4-CKE0 / DDR4-CKE1		Clock enable
		• DDR4-ALERT		CRC error flag
		• DDR4-ACT		Activation command input
		• DDR4-EVENT		Temperature event
	I²C	• DDR4-SCL • DDR4-SDA	8-channel I²C switch U37	-

Table 40: DDR4 64-bit memory interface signals and pins

Refer to the Xilinx Zynq UltraScale+ datasheet DS925 for more information on whether the specific package of the Zynq UltraScale+ MPSoC supports the maximum data transmission rate of 2400 MByte/s, which also depends on the used SO-DIMM module.

CAN Interface

The TEB0911 board provides a CAN interface, the CAN transceiver is connected and operated by the SC CPLD:

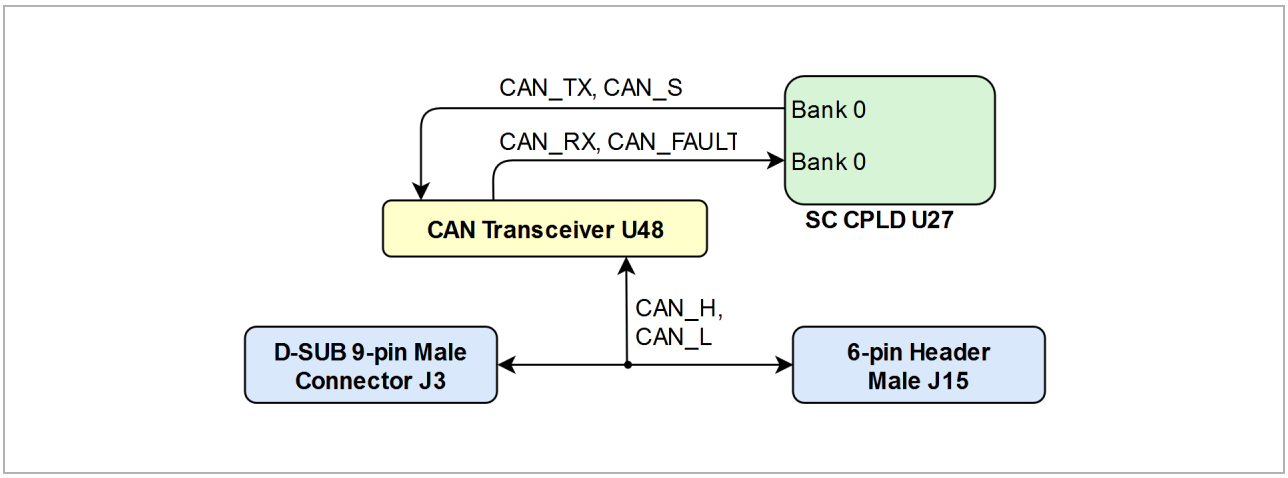


Figure 11: CAN interface

The CAN interface of external devices can be connected via D-SUB 9-pin male connector J3 or to the 6-pin male header J15:

Connector	Signal Schematic Name	Connected to	Notes
D-SUB 9-pin male connector J3	• CAN_H	CAN Transceiver U48, pin 7	-
	• CAN_L	CAN Transceiver U48, pin 6	-
6-pin male header J15	• CAN_H	CAN Transceiver U48, pin 7	-
	• CAN_L	CAN Transceiver U48, pin 6	-
CAN Transceiver	**Signal Schematic Name**	**Connected to**	**Notes**
TCAN337 U48	• CAN_TX	SC CPLD U27, bank 0, pin C16	3.3V VCCIO
	• CAN_RX	SC CPLD U27, bank 0, pin B15	3.3V VCCIO
	• CAN_S	SC CPLD U27, bank 0, pin C15	3.3V VCCIO
	• CAN_FAULT	SC CPLD U27, bank 0, pin D15	3.3V VCCIO

Table 41: CAN interface signals and pins

SD Card Interface

The SD Card interface of the TEB0911 board is routed via SD IO interface to the PS MIO bank 501 of the Zynq Ultrascale+ MPSoC (3.3V VCCO). The SC CPLD U27 controls the load switch Q3 to enable the card sockets J11 with signal 'SD_EN', bank 2, pin U11. The "Card Detect" and "Write Protect" signal are also routed to the SC CPLD:

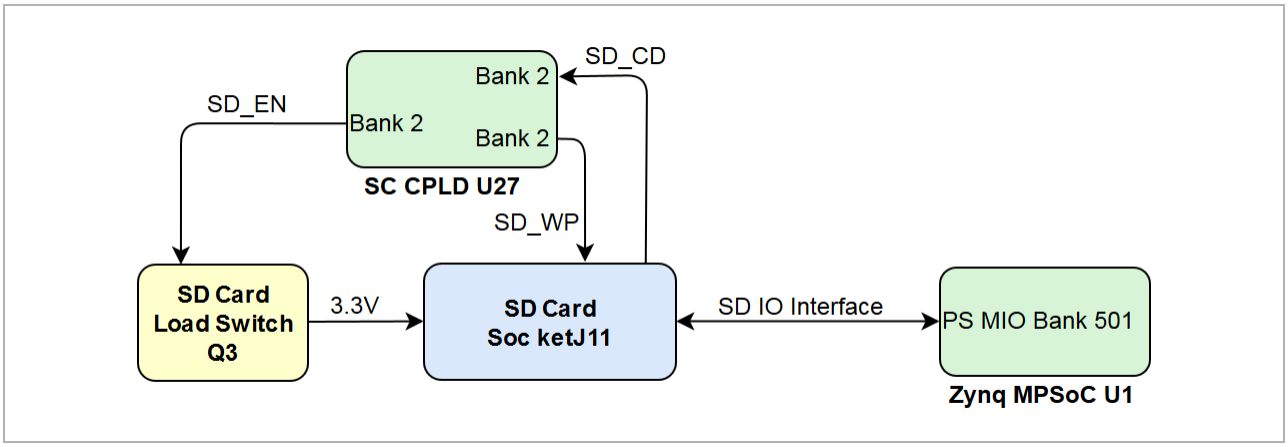


Figure 12: SD Card interface

The SD Card socket have following signal and pin assignment:

Connector	Signal Schematic Name	Connected to	Notes
SD Card Socket J11	• SD_DAT0	PS bank 501 Pins: MIO46 ... MIO51	-
	• SD_DAT1		-
	• SD_DAT2		-
	• SD_DAT3		-
	• SD_CMD		-
	• SD_CK		-
	• SD_CD	SC CPLD U27, bank 2, pin T11	Card Detect
	• SD_WP	SC CPLD U27, bank 2, pin T10	Write Protect

Table 42: SD Card interface signals and connections

4-Wire PWM FAN Connectors

The TEB0911 offers 3x 4-wire PWM FAN connectors for optional cooling fans controlled by SC CPLD U27:

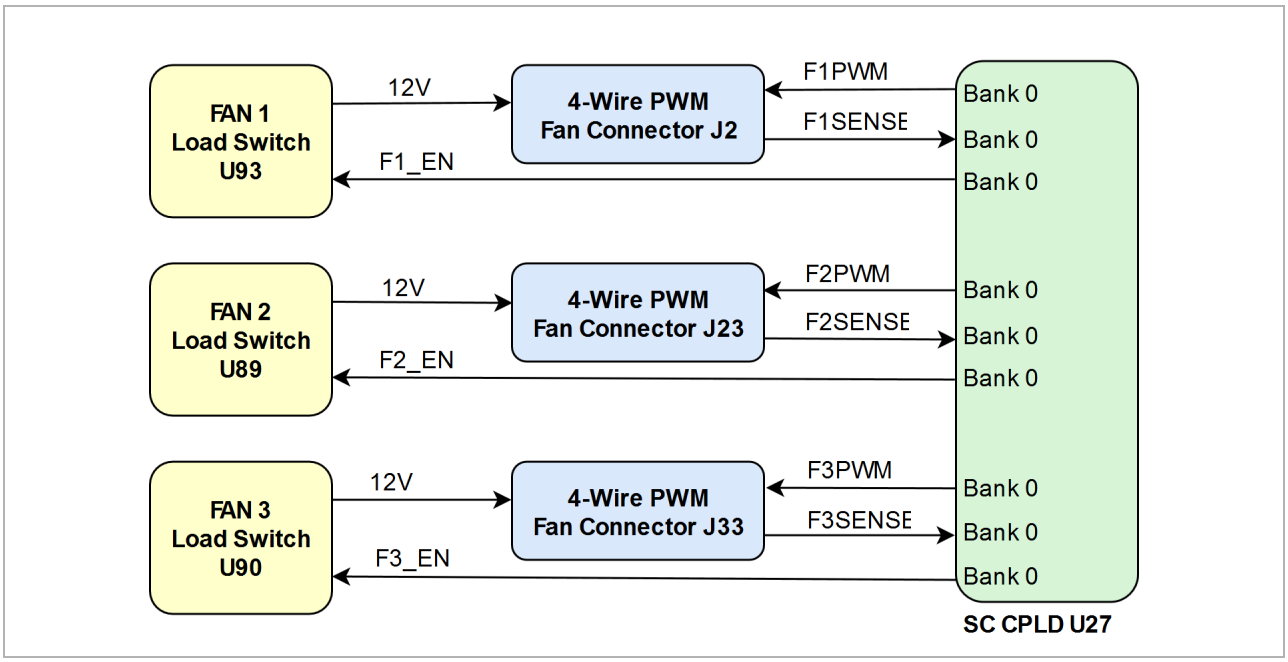


Figure 13: 4-wire PWM FAN connectors

Following table contains a brief description of the control signals of the fan connectors:

Connector	Signal Schematic Name	Connected to	Notes
Fan Connector J2	• F1PWM	SC CPLD U27, bank 0, pin E10	PWM signal to fan
	• F1SENSE	SC CPLD U27, bank 0, pin D11	sense RPM signal of fan
	• F1_EN	SC CPLD U27, bank 0, pin C8	enable 12V fan supply voltage
Fan Connector J23	• F2PWM	SC CPLD U27, bank 0, pin D9	PWM signal to fan
	• F2SENSE	SC CPLD U27, bank 0, pin G12	sense RPM signal of fan
	• F2_EN	SC CPLD U27, bank 0, pin B4	enable 12V fan supply voltage
Fan Connector J33	• F3PWM	SC CPLD U27, bank 0, pin B13	PWM signal to fan
	• F3SENSE	SC CPLD U27, bank 0, pin A13	sense RPM signal of fan
	• F3_EN	SC CPLD U27, bank 0, pin A12	enable 12V fan supply voltage

Table 43: 4-wire PWM fan connectors signals and pins

PLL Clock Interfaces

The programmable 10-output reference clock generator U17 can be accessed through its I²C interface to be programed. The I²C interface is connected to the Zynq MPSoc via I²C switch U13 and to pin header J22.

With the SMA Coaxial connector J25 the clock generator can be supplied with an external clock signal.

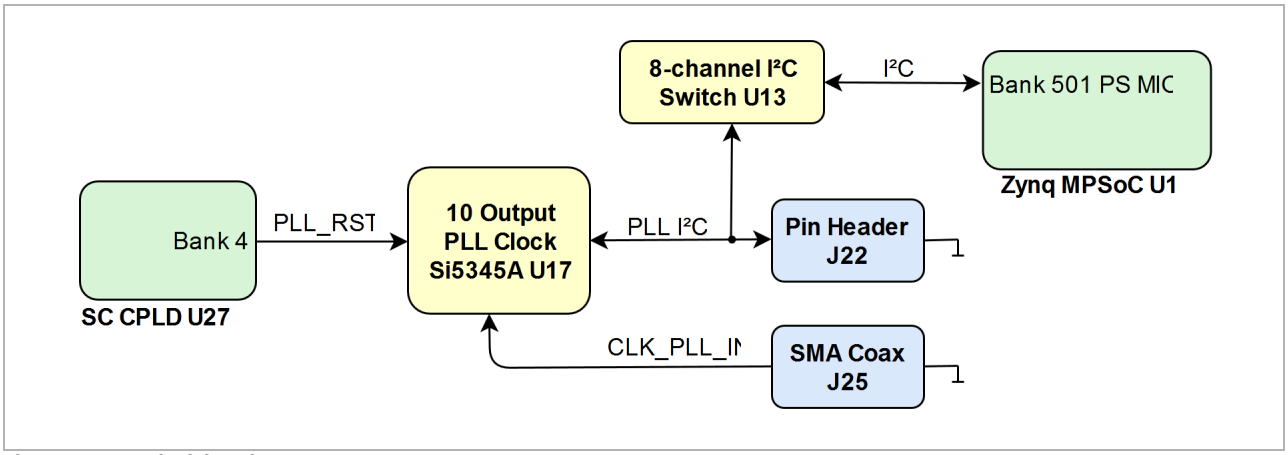


Figure 14: PLL clock interface

Connector	Signal Schematic Name	Connected to	Notes
Pin Header J22	• PLL_SCL	clock generator U17, pin 16	PS_1V8 VCCIO
	• PLL_SDA	clock generator U17, pin 18	
SMA Coax J25	• CLK_PLL_IN	clock generator U17, pin 1	-

Table 44: Clock generator Si5345A external interfaces

On-board Peripherals

System Controller CPLD

The TEB0911 UltraRack is equipped with one System Controller CPLDs - Lattice Semiconductor LCMXO2-7000HC (MachXO2 Product Family) with the schematic designators U27. The SC-CPLD is the central system management unit where essential control signals are logically linked by the implemented logic in CPLD firmware, which generates output signals to control the system, the on-board peripherals and the interfaces. Interfaces like JTAG and I^2C between the on-board peripherals and to the FPGA module are by-passed, forwarded and controlled by the System Controller CPLD.

Other tasks of the System Controller CPLD are the monitoring of the power-on sequence and to display the programming state of the FPGA module. The functionalities and configuration of the pins depend on the CPLDs' firmware. The documentations of the firmware of SC CPLD U27 contains detailed information on this matter.

The Sytem Controller CPLDs are connected to the Zynq Ultrascale+ MPSoC through MIO and PL pins. The signals of these pins are forwarded by the SC CPLD to control some of the on board peripherals.

Following block diagram visualizes the connection of the SC CPLDs with the Zynq Ultrascale+ MPSoC via PS MIO pins and singled ended PL pins:

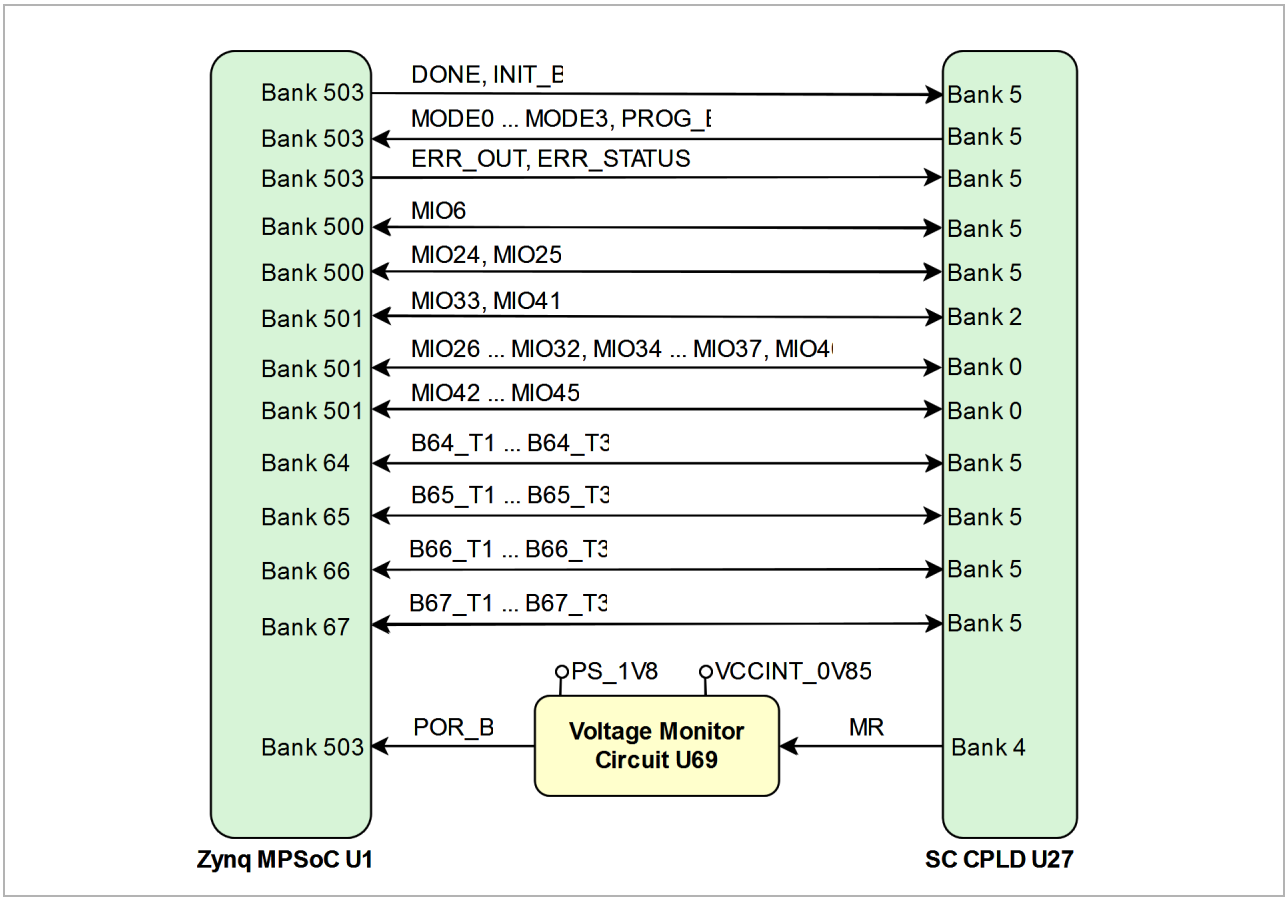


Figure 15: I/O's connecting Zynq MPSoC and SC CPLD

For detailed information about the current function of the MIO-pin in conjunction with the SC CPLD, the internal signal assignment and implemented logic, refer to the Wiki reference page of the SC CPLD firmware of this board or into the bitstream file of the SC CPLD.

The PS_1V8 and VCCINT_0V85 voltage levels are monitored by the voltage monitor circuit U89, which generates the POR_B signal to reset the board if voltage failure occurs. A manual reset is also possible by driving the pin 'MR' on SC CPLD, bank 4, pin L7 to GND. Refer to documentation of the SC CPLD firmware for detailed information to reset the board manually.

High-speed USB2 ULPI PHY

USB2 PHY U15 is provided by USB3320 from Microchip. The ULPI interface is connected to the Zynq Ultrascale+ PS USB0. I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 52.000000 MHz oscillator U16.

PHY Pin	Connected to	Notes
ULPI	PS bank MIO52 ... MIO63	Zynq Ultrascale+ USB0 MIO pins are connected to the PHY
REFCLK	-	52MHz from on board oscillator U16

REFSEL[0..2]	-	All pins set to GND selects the external reference clock frequency (52.000000 MHz)
RESETB	SC CPLD U27, bank 4, Pin: M2	Low active USB2 PHY Reset (pulled-up to PS_1.8V)
DP, DM	4-port USB3 Hub U4	USB2 data lane
CPEN	-	External USB power switch active-high enable signal
VBUS	5V	Connected to USB VBUS via a series of resistors, see schematic
ID	-	For an A-device connect to the ground. For a B-device, leave floating

Table 45: USB PHY interface connections

4-port USB3 Hub

On the TEB0911 board there are to 2 USB3 Super Speed ports available, which are also downward compatible to USB2 High Speed ports. The USB3 ports are provided by Cypress Semiconductor CYUSB3324 4-port USB3 Hub controller U4. The pin-strap configuration option of the USB3 Hub is disabled, so this controller gets the configuration data and parameter from the configuration EEPROM U5. The I²C interface of the EEPROM and the controller are also accessible by the Zynq Ultrascale+ MPSoC through I²C switch U37.

On the Upstream-side, this controller is connected to the MGT1 lane of MPSoC's PS GT bank 505 to establish the USB3 data lane. For the USB2 interface, the controller is connected to the on-board USB2 PHY U15. The USB2 PHY is connected via ULPI interface (MIO pins 52..63) to MPSoC's MIO bank.

The USB3 Hub controller has also an ARM Cortex-M0 controller integrated, refer to the data sheet for further features and programmable options.

Gigabit Ethernet PHY

On-board Gigabit Ethernet PHY U20 is provided with Marvell Alaska 88E1512. The Ethernet PHY RGMII interface is connected to the Zynq Ultrascale+ Ethernet0 PS GEM3. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from the on-board 25.000000 MHz oscillator U21. The 125MHz PHY output clock (PHY_CLK125M) is routed to System Controller CPLD U27, bank 4, pin K2.

8-Channel I²C Switches

All on-board and on-module peripherals with accessible I²C interface are muxed to the I²C interface of the Zynq Ultrascale+ MPSoC as master.

For this purpose, the TEB0911 board is equipped with two 8-channel I²C switches provided by TCA9548A from Texas Instruments, together creating up to 16 switched I²C channels.

Refer to the data sheet of the TCA9548A chip how to address and and transmit data to the I²C slave devices through this switches.

The on-board I^2C bus works with reference voltage 3.3V, it is connected to the MPSoC I^2C interface via PS MIO bank (pins MIO38, MIO39) and configured as master.

MIO	Signal Schematic Name	Notes
38	• I2C_SCL	3.3V reference voltage
39	• I2C_SDA	3.3V reference voltage

Table 46: MIO-pin assignment of the module's I^2C interface

The I²C switches can be reseted simultanously by the pin 'I2C_RST', which is connected to SC CPLD U27, bank 4 pin L2 with low active logic.

I²C addresses (7 bit without read/write-bit) for on-board slave devices are listed in the table below:

I²C Slave Devices connected to MPSoC I²C Interface	**I²C Switch Position**	**I²C Slave Address**	**Schematic Names of I²C Bus Lines**
8-channel I²C switch U13	-	0x76	• I2C_SDA / I2C_SCL
8-channel I²C switch U37	-	0x77	• I2C_SDA / I2C_SCL
I²C Slave Devices connected to 8-channel I²C Switch U13	**I²C Switch Position**	**I²C Slave Address**	**Schematic Names of I²C Bus Lines**
FMC Connector J7 (FMC D)	2	0x50	• FMCD_SDA / FMCD_SCL
FMC Connector J6 (FMC E)	3	0x50	• FMCE_SDA / FMCE_SCL
FMC Connector J4 (FMC B)	4	0x50	• FMCB_SDA / FMCB_SCL
FMC Connector J8 (FMC C)	5	0x50	• FMCC_SDA / FMCC_SCL
PLL clock generator U17 Si5345A	6	0x69	• PLL_SDA / PLL_SCL
I²C Slave Devices connected to 8-channel I²C Switch U37	**I²C Switch Position**	**I²C Slave Address**	**Schematic Names of I²C Bus Lines**
FMC Connector J10 (FMC A)	1	0x50	• FMCA_SDA / FMCA_SCL
FMC Connector J21 (FMC F)	2	0x50	• FMCF_SDA / FMCF_SCL
SFP+ Connector J9A	3	0x50 / 0x51	• SFP0_SDA / SFP0_SCL
8-bit I²C IO Expander U86 (SPF+ connector control signals)	3	0x27	• SFP0_SDA / SFP0_SCL
SFP+ Connector J9B	4	0x50 / 0x51	• SFP1_SDA / SFP1_SCL
PLL clock generator U12 Si5338A	5	0x70	• MEM_SDA / MEM_SCL

Configuration EEPROM U83	5	0x51	• MEM_SDA / MEM_SCL
Configuration EEPROM U45	5	0x52	• MEM_SDA / MEM_SCL
Configuration EEPROM U60	5	0x53	• MEM_SDA / MEM_SCL
Configuration EEPROM U57	5	0x57	• MEM_SDA / MEM_SCL
SC CPLD U27	5	user configurable	• MEM_SDA / MEM_SCL
DDR4 SODIMM I²C interface	6	module dependent	• DDR4-SDA / DDR4-SCL
USB3 Hub U4	7	0x60	• USBH_SDA / USBH_SCL
USB3 Hub configuration EEPROM U5	7	0x51	• USBH_SDA / USBH_SCL

Table 46: On-board peripherals' I^{2}C-interfaces device slave addresses

Configuration EEPROMs

The TEB0911 carrier board contains several EEPROMs for configuration and general user purposes. The EEPROMs are provided by Microchip, the I²C interfaces of the EEPROM's are multiplexed to the I²C switch U37:

EEPROM Modell	Designator	Memory Density	Purpose
24LC128-I/ST	U57	128 Kbit	user
24AA025E48T-I/OT	U60	2 Kbit	user
24AA025E48T-I/OT	U45	2 Kbit	user
24AA025E48T-I/OT	U83	2 Kbit	user
24LC128-I/ST	U5	128 Kbit	USB3 Hub U4 configuration memory

Table 47: On-board configuration EEPROMs overview

CAN FD Transceiver

On-board CAN FD (Flexible Data Rate) transceiver U48 is provided by Texas Instruments TCAN337. This controller is the physical layer of the CAN interface and is specified for data rates up to 1 Mbps. The controller has many protection features included to ensure CAN network robustness and to eliminate the need for additional protection circuits. Refer to the data sheet of this transceiver for more details and specifications.

The transceiver is connected to System Controller CPLD U27, means it works on this interface with 3.3V VCCIO. The logical signal processing of the CAN interface depends on the current firmware ot the SC CPLD.

On-board Flash Memory

On-board QSPI flash memory U24 and U25 on the TEB0911 board is provided by Micron Serial NOR Flash Memory N25Q256A with 256 Mbit (32 MByte) storage capacity each. The QSPI Flash memory ICs are connected to the PS MIO bank (Dual QSPI MIO0 ... MIO12) of the Zynq Ultrascale+ MPSoC. This non volatile memory is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the Zynq MPSoC allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.

The TEB0911 board is also equipped with embedded MMC memory connected to the PS MIO bank (MIO13 ... MIO23) of the Zynq Ultrascale+ MPSoC. The memory is provided by MTFC4GACAJCN-4M IT from Micron Technology. It has a memory density of 32 Gbit (4 GByte) and is sectored into 8 banks a 4 Gbit.

IC	Name	Memory Density	Connected to	Notes
QSPI Flash U24	N25Q256A11E1240E	256 Mbit (32 MByte)	QSPI0: MIO0 ... MIO5	dual parallel booting possible, 64 MByte total QSPI Flash memory
QSPI Flash U25	N25Q256A11E1240E	256 Mbit (32 MByte)	QSPI0: MIO7 ... MIO12	connected via Dual QSPI MIO0 ... MIO12
eMMC Flash U26	MTFC4GACAJCN-4M IT	32 Gbit (4 GByte)	SD0 eMMC: MIO13 ... MIO23	bootable eMMC

Table 48: On-board Flash memory ICs overview

Quad SPI Flash memory ICs U24 and U25 are connected to the Zynq MPSoC PS QSPI0 interface via PS MIO bank 500, pins MIO0 ... MIO5 and MIO7 ... MIO12.
eMMC Flash memory IC U25 is connected to Zynq MPSoC by pins MIO13 ... MIO23.

MIO	Signal Schematic Name	Flash U24 Pin		MIO	Signal Schematic Name	Flash U25 Pin		MIO	Signal Schematic Name	Flash U26 Pin
0	• MIO0	B2		7	• MIO7	C2		13	• MMC-D0	H3
1	• MIO1	D2		8	• MIO8	D3		14	• MMC-D1	H4
2	• MIO2	C4		9	• MIO9	D2		15	• MMC-D2	H5
3	• MIO3	D4		10	• MIO10	C4		16	• MMC-D3	J2
4	• MIO4	D3		11	• MIO11	D4		17	• MMC-D4	J3
5	• MIO5	C2		12	• MIO12	B2		18	• MMC-D5	J4
								19	• MMC-D6	J5
								20	• MMC-D7	J6
								21	• MMC-CMD	W5
								22	• MMC-CLKR	W6
								23	• MM_ RST	U5

Table 49: PS MIO pin assignment of the Flash memory ICs

⚠ SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash during power-on. By default this bit is set to high at the manufacturing plant.

Oscillators

The TEB0911 board is equipped several on-board oscillators to provide the Zynq Ultrascale+ MPSoC's PS and PL banks and the on-board peripherals with reference clock-signals:

Clock Source	Signal Schematic Name	Frequency	Clock Input Destination
SiTime SiT8008BI oscillator, U22	• PS_CLK	33.333333 MHz	Zynq MPSoC PS Config Bank 503, pin U24
SiTime SiT8008AI oscillator, U16	• USB_CLK	52.000000 MHz	USB2 transceiver PHY U15, pin 26
Kyocera CX3225SB26000, Y3	-	26.000 MHz	4-port USB3 Hub U4, pin 68/69
Kyocera CX3225SB26000, Y2	• XAXB_P • XAXB_N	54.000 MHz	PLL clock generator U17, pin 8/9
SiTime SiT8008BI oscillator, U21	• ETH_CLKIN	25.000000 MHz	Gigabit Ethernet PHY U20, pin 34
SiTime SiT8008AI oscillator, U87 **optional, not equipped**	• CLK_SC	25.000000 MHz	System Controller CPLD U27, bank 2, pin AA9
SiTime SiT8008BI oscillator, U18	• IN0_P	25.000000 MHz	PLL clock generator U17, pin 63
SiTime SiT8008AI oscillator, U85	-	25.000000 MHz	PLL clock generator U12, pin 3
DSC1123 oscillator, U92 **optional, not equipped**	• B505_CLK3_P • B505_CLK3_N	100.0000 MHz	PS GTR Bank 505 Lane 3, dedicated for DisplayPort, pin U31, U32

Table 50: Reference clock signal oscillators

Programmable Clock Generator Si5338A

There is a Si5338A U12, Silicon Labs I^2C programmable quad PLL clock generator on-board to generate various reference clocks for the Zynq MPSoC MGT banks and on-board peripherals.

Si5338A Pin	Signal Schematic Name	Connected to	Clock Direction	Note
IN1	• CLK8_N	U17, pin 54	Input	Differential reference clock input from PLL clock generator U17
IN2	• CLK8_P	U17, pin 53	Input	
IN3	-	U85, pin 3	Input	25.000000 MHz oscillator, Si8008AI
IN4	-	GND	Input	LSB (pin 'IN4') of the default I²C-adress 0x70 not set
IN5	-	Not connected	Input	Not used

IN6	-	GND	Input	Not used
CLK0A	• SSD_RCLK_P	U2, pin 55	Output	NGFF M.2 PCIe socket (Key M), dedicated as SSD interface
CLK0B	• SSD_RCLK_N	U2, pin 53	Output	
CLK1A	• B505_CLK2_N	U1, pin U27	Output	PS GTR Bank 505 Lane 2
CLK1B	• B505_CLK2_P	U1, pin U28	Output	
CLK2A	• B505_CLK1_N	U1, pin W27	Output	PS GTR Bank 505 Lane 1
CLK2B	• B505_CLK1_P	U1, pin W28	Output	
CLK3A	• B505_CLK0_P	U1, pin AA27	Output	PS GTR Bank 505 Lane 0
CLK3B	• B505_CLK0_N	U1, pin AA28	Output	

Table 51: Programmable quad PLL clock generator inputs and outputs

Programmable Clock Generator Si5345A

Following table shows on-board Silicon Labs I^2C programmable Si5345A U17 10-output programmable PLL reference clock generator inputs and outputs:

Si5345A Pin	Signal Schematic Name	Connected to	Clock Direction	Note
IN0	• IN0_P	not connected	Input	Not used
	• IN0_N	GND		
IN1	• IN1_P	SMA Coax J25, pin 1	Input	external reference clock input
	• IN1_N	GND		
IN2	-	not connected	Input	not used
	-	not connected		
IN3	-	not connected	Input	not used
	-	not connected		
OUT0	• CLK0_P	not connected	Output	not used
	• CLK0_N	not connected		

OUT1	• CLK1_P	U1, pin E8	Output	GTH bank 229 reference clock input
	• CLK1_N	U1, pin E7		
OUT2	• CLK2_P	U1, pin B10	Output	GTH bank 230 reference clock input
	• CLK2_N	U1, pin B9		
OUT3	• CLK3_P	U1, pin J8	Output	GTH bank 228 reference clock input
	• CLK3_N	U1, pin J7		
OUT4	• CLK4_P	U1, pin N27	Output	GTH bank 128 reference clock input
	• CLK4_N	U1, pin N28		
OUT5	• CLK5_P	U1, pin J27	Output	GTH bank 129 reference clock input
	• CLK5_N	U1, pin J28		
OUT6	• CLK6_P	U1, pin E27	Output	GTH bank 130 reference clock input
	• CLK6_N	U1, pin E28		
OUT7	• CLK7_P	U27, pin E1	Output	Clock signal input to SC CPLD, bank 5
	• CLK7_N	not connected		
OUT8	• CLK8_P	U12, pin 2	Output	Differential reference clock input to PLL clock generator U12
	• CLK8_N	U12, pin 1		
OUT9	-	not connected	Output	not used
	-	not connected		
XA/XB	• XAXB_P	54.000 MHz quartz oscillator Y1	Input	Differential quartz oscillator clock input
	• XAXB_N			

Table 52: Programmable 10-output PLL clock generator inputs and outputs

The PLL clock generator U17 can be resetted by the low active pin 'PLL_RST' connected to SC CPLD U27, bank 4, pin L4.

The on-board header J22 provides the possibility to program the clock generator U17 via I²C bus (1.8V reference voltage).

On-board LEDs

The TEB0911 board is equipped with several LEDs to signal current states and activities.

LED	Color	Connected to	Description and Notes
D6	red	Zynq MPSoC U1, pin W21	Reflects inverted DONE signal. ON when FPGA is not configured, OFF as soon as PL configuration is finished.
D17	green	USB3 Hub U4, pin 25	LED is on if all USB3 and USB2 ports are in the suspend state and is off when one of the ports comes out of the suspend state.
D18	green	USB3 Hub U4, pin 4	LED output for downstream 1 port.
D19	green	USB3 Hub U4, pin 63	LED output for downstream 3 port.
D2	red	SC CPLD U27, bank 2, pin AB17	SFP+ interface status. The LEDs are fitted on-board under the SFP+ connector cage. The light of the LEDs are conducted to the front of the connector through integrated LED light pipes.
D4	green	SC CPLD U27, bank 2, pin AB18	
D3	red	SC CPLD U27, bank 2, pin AA16	
D5	green	SC CPLD U27, bank 2, pin AB15	
D13	green	SC CPLD U27, bank 2, pin U12	functionality depends on the current firmware of the SC CPLD U27 refer to the documentation section: LED
D14	green	SC CPLD U27, bank 2, pin V12	
D15	green	SC CPLD U27, bank 2, pin W12	
D16	red	SC CPLD U27, bank 2, pin V13	

Table 53: On-board LEDs

User Buttons

There are two switch buttons available to the user connected to the SC CPLD U27:

Button	Connected to	Notes
S1	SC CPLD U27, bank 0, pin F13	high active logic, connected to 3V3SB, functionality depends on the current firmware of the SC CPLD U27 refer to the documentation
S2	SC CPLD U27, bank 0, pin G13	

Table 54: On-board switch buttons

Configuration DIP-switches

There are two 4-bit DIP-witches S3 and S4 present on the TEB0911 board to configure options and set parameters. The following section describes the functionalities of the particular switches.

Table below describes the functionalities of the switches of DIP-switches S3 and S4 at their each positions:

DIP-switch S3	Signal Schematic Name	Connected to	Functionality	Notes

S3-1	• PUDC_B	Zynq MPSoC U1, pin AD15	Positions ON: PUDC_B is Low OFF: PUDC_B is HIGH	Internal pull-up resistors during configuration are enabled at ON-position,means I/O's are 3-stated until configuration of the FPGA completes.
S3-2	• JTAGENB	SC CPLD U27, bank 0, pin A16	Positions ON: SC CPLD's JTAG enabled OFF: SC CPLD's JTAG disabled	JTAG interface of the SC CPLD, accessible on XMOD header J35
S3-3	• SC_SW1	SC CPLD U27, bank 0, pin E17	set 2-bit code for boot mode selection	TEB0911 CPLD Firmware Documentation Section: Boot Mode
S3-4	• SC_SW2	SC CPLD U27, bank 0, pin D16		
DIP-switch S4	**Signal Schematic Name**	**Connected to**	**Functionality**	**Notes**
S4-1	• U_SW1	SC CPLD U27, bank 0, pin D18	user defined	For functionalities of these switches in the current CPLD firmware, refer to the TEB0911 CPLD Firmware Documentation.
S4-2	• U_SW2	SC CPLD U27, bank 0, pin D16		
S4-3	• U_SW3	SC CPLD U27, bank 0, pin C19		
S4-4	• U_SW4	SC CPLD U27, bank 0, pin C18		

Table 55: DIP-switch S3 and S4 functionality description

Power and Power-On Sequence

Power Consumption

The maximum power consumption of the board mainly depends on the design running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input	Typical Current
24V VIN	TBD*

Table 56: Typical power consumption, *to Be Determined soon with reference design setup.

Power supply with minimum current capability of 2A for system startup is recommended. If using all FMC connectors with FPGA Mezzanine Cards, a higher current availability of up to 4A is recommended.

The TEB0911 UltraRack board is equipped with the Xilinx Zynq UltraScale+ MPSoC delivers a heterogeneous multi-processing system with integrated programmable logic and independently operable elements and is designed to meet embedded system power management requirement by advanced power management features. This features allow to offset the power and heat constraints against overall performance and operational efficiency.

This features allowing highly flexible power management are achieved by establishing Power Domains for power isolation. The Zynq UltraScale+ MPSoC has multiple power domains, whereby each power domain requires its own particular on-board DC-DC converters.

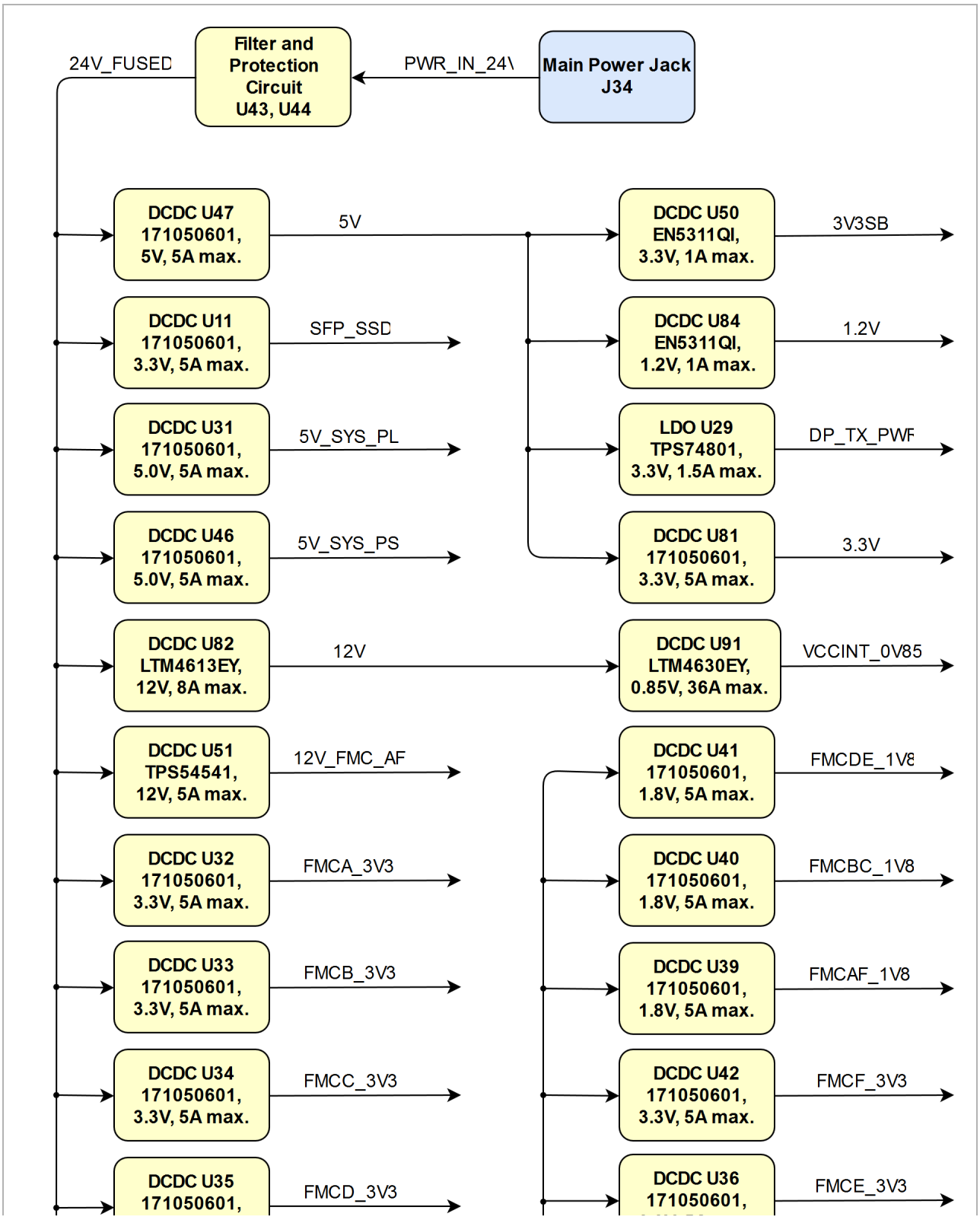
The Processing System contains three Power Domains:

- Battery Power Domain (BBRAM and RTC)

- Full-Power Domain (Application Processing Unit, DDR Controller, Graphics Processing Unit and High-Speed Connectivity)
- Low-Power Domain (Real-Time Processing Unit, Security and Configuration Unit, Platform Management Unit, System Monitor and General Connectivity)
- Programmable Logic (PL)

Power Distribution Dependencies

There are following dependencies how the initial 24V voltage from the main power jack J34 is distributed to the on-board DC-DC converters, which power up further DC-DC converters and the particular on-board voltages:


24V_FUSED
Filter and Protection Circuit U43, U44
PWR_IN_24V
Main Power Jack J34
DCDC U47 171050601, 5V, 5A max.
5V
DCDC U50 EN5311QI, 3.3V, 1A max.
3V3SB
DCDC U11 171050601, 3.3V, 5A max.
SFP_SSD
DCDC U84 EN5311QI, 1.2V, 1A max.
1.2V
DCDC U31 171050601, 5.0V, 5A max.
5V_SYS_PL
LDO U29 TPS74801, 3.3V, 1.5A max.
DP_TX_PWR
DCDC U46 171050601, 5.0V, 5A max.
5V_SYS_PS
DCDC U81 171050601, 3.3V, 5A max.
3.3V
DCDC U82 LTM4613EY, 12V, 8A max.
12V
DCDC U91 LTM4630EY, 0.85V, 36A max.
VCCINT_0V85
DCDC U51 TPS54541, 12V, 5A max.
12V_FMC_AF
DCDC U41 171050601, 1.8V, 5A max.
FMCDE_1V8
DCDC U32 171050601, 3.3V, 5A max.
FMCA_3V3
DCDC U40 171050601, 1.8V, 5A max.
FMCBC_1V8
DCDC U33 171050601, 3.3V, 5A max.
FMCB_3V3
DCDC U39 171050601, 1.8V, 5A max.
FMCAF_1V8
DCDC U34 171050601, 3.3V, 5A max.
FMCC_3V3
DCDC U42 171050601, 3.3V, 5A max.
FMCF_3V3
DCDC U35 171050601,
FMCD_3V3
DCDC U36 171050601,
FMCE_3V3

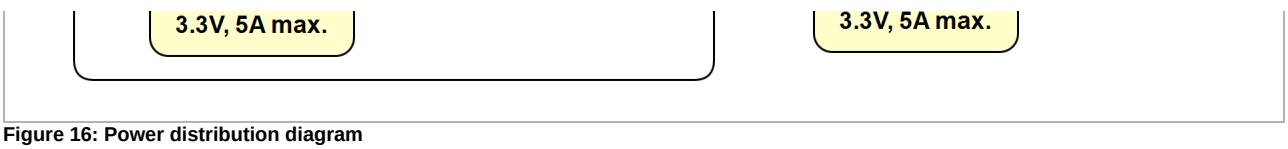
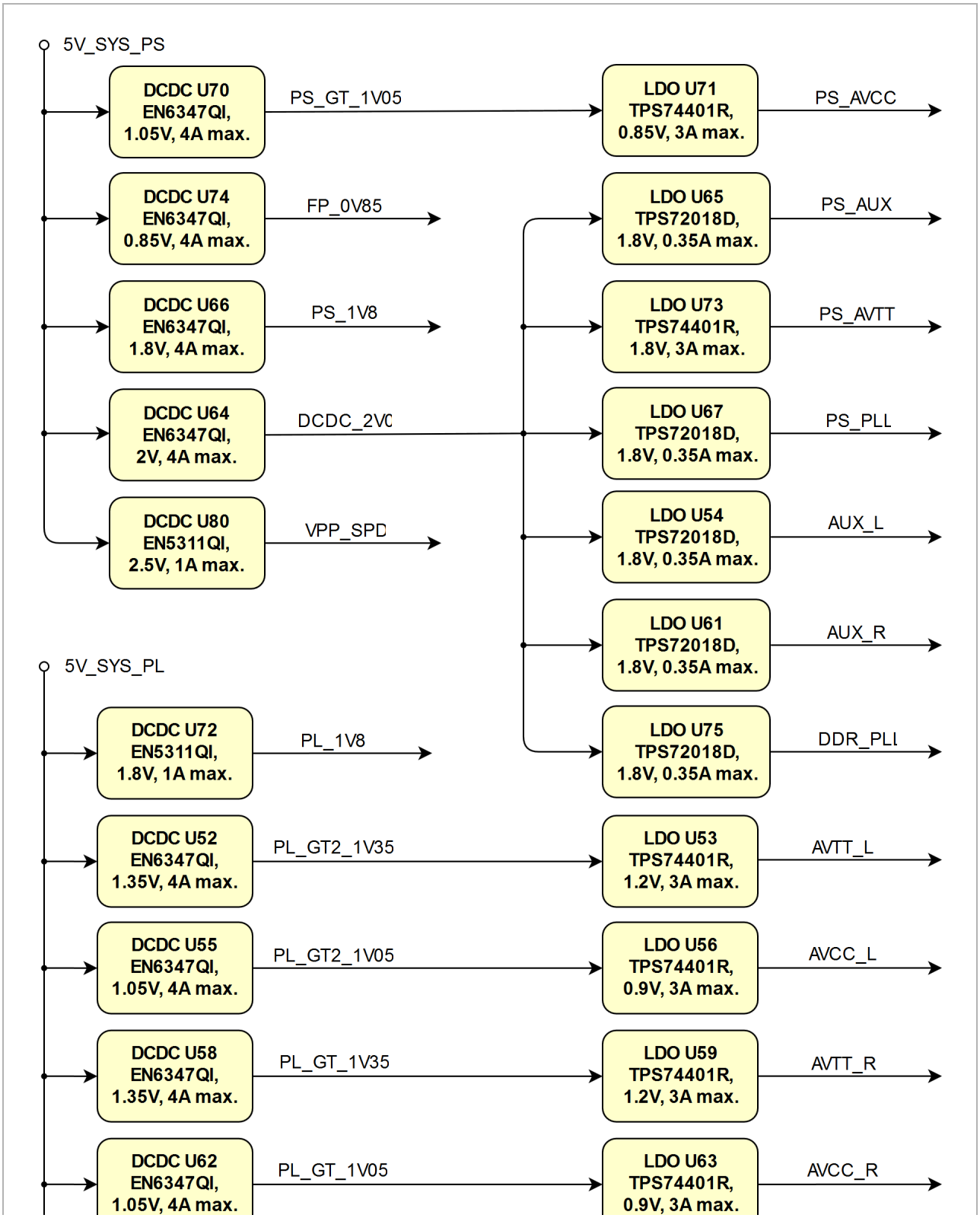


Figure 16: Power distribution diagram

Power distribution to the MPSoC PS and PL units:


5V_SYS_PS
DCDC U70
EN6347QI,
1.05V, 4A max.
PS_GT_1V05
LDO U71
TPS74401R,
0.85V, 3A max.
PS_AVCC
DCDC U74
EN6347QI,
0.85V, 4A max.
FP_0V85
LDO U65
TPS72018D,
1.8V, 0.35A max.
PS_AUX
DCDC U66
EN6347QI,
1.8V, 4A max.
PS_1V8
LDO U73
TPS74401R,
1.8V, 3A max.
PS_AVTT
DCDC U64
EN6347QI,
2V, 4A max.
DCDC_2V0
LDO U67
TPS72018D,
1.8V, 0.35A max.
PS_PLL
DCDC U80
EN5311QI,
2.5V, 1A max.
VPP_SPD
LDO U54
TPS72018D,
1.8V, 0.35A max.
AUX_L
LDO U61
TPS72018D,
1.8V, 0.35A max.
AUX_R
5V_SYS_PL
DCDC U72
EN5311QI,
1.8V, 1A max.
PL_1V8
LDO U75
TPS72018D,
1.8V, 0.35A max.
DDR_PLL
DCDC U52
EN6347QI,
1.35V, 4A max.
PL_GT2_1V35
LDO U53
TPS74401R,
1.2V, 3A max.
AVTT_L
DCDC U55
EN6347QI,
1.05V, 4A max.
PL_GT2_1V05
LDO U56
TPS74401R,
0.9V, 3A max.
AVCC_L
DCDC U58
EN6347QI,
1.35V, 4A max.
PL_GT_1V35
LDO U59
TPS74401R,
1.2V, 3A max.
AVTT_R
DCDC U62
EN6347QI,
1.05V, 4A max.
PL_GT_1V05
LDO U63
TPS74401R,
0.9V, 3A max.
AVCC_R

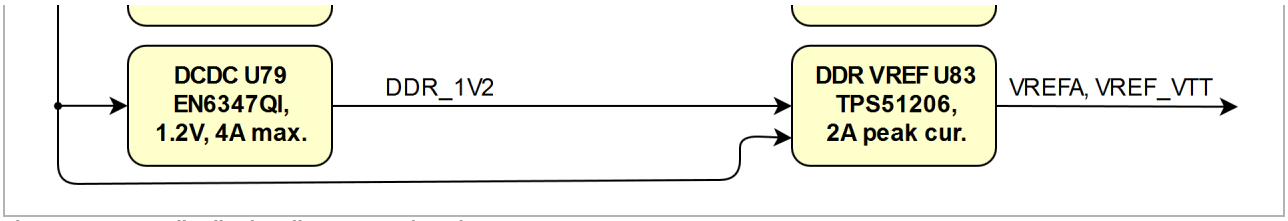


Figure 17: Power distribution diagram continued

Note: The DC-DC converter U91 LTM4630EY has an integrated temperature diode for device temperature monitoring. The analog signal 'TEMP_CORE_DC' on pin J6 of the converter is routed to the dedicated differential analog interface (XADC) of the Zynq MPSoC, pin U18 (V_P), pin V17 (V_N) is connected to analog GND.

To avoid any damage to the module, check for stabilized on-board voltages should be carried out(i.e. power good and enable signals) before powering up any SoC's I/O bank voltages VCCO_x. All I/Os should be tri-stated during power-on sequence.

Power-On Sequence

The TEB0911 UltraRack board meets the recommended criteria to power up the Xilinx Zynq UltraScale+ MPSoC properly by keeping a specific sequence of enabling the on-board DC-DC converters dedicated to the particular Power Domains and powering up the on-board voltages.

On the TEB0911 UltraRack board following Power Domains will be powered up in a certain sequence with by enable and power-good signals of the DC-DC converters, which are controlled by the System Controller CPLD U27:

1. Low-Power Domain (LPD)
2. Programmable Logic (PL) and Full-Power Domain (FPD)
3. GTH, PS GTR transceiver and DDR memory

Hence, those three power instances will be powered up consecutively when the Power-Good signals of the previous instance is asserted.

Following diagram describes the sequence of enabling the three power instances utilizing the DC-DC converter control signals (Enable, Power-Good), which will power-up in descending order as listed in the blocks of the diagram.

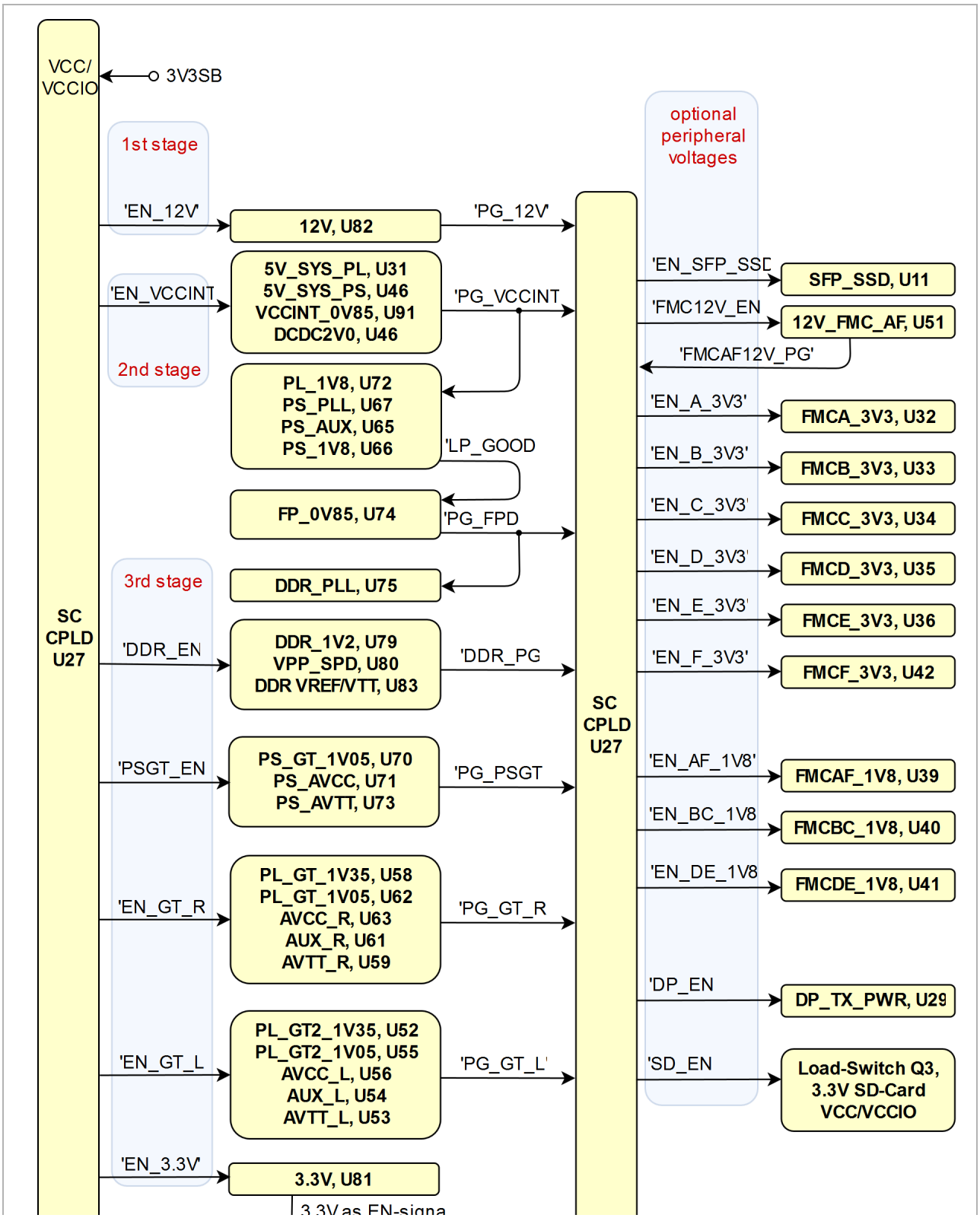

VCC/
VCCIO
3V3SB
SC
CPLD
U27
1st stage
'EN_12V'
12V, U82
'PG_12V'
'EN_VCCINT'
5V_SYS_PL, U31
5V_SYS_PS, U46
VCCINT_0V85, U91
DCDC2V0, U46
'PG_VCCINT'
2nd stage
PL_1V8, U72
PS_PLL, U67
PS_AUX, U65
PS_1V8, U66
'LP_GOOD'
FP_0V85, U74
'PG_FPD'
3rd stage
DDR_PLL, U75
'DDR_EN'
DDR_1V2, U79
VPP_SPD, U80
DDR VREF/VTT, U83
'DDR_PG'
'PSGT_EN'
PS_GT_1V05, U70
PS_AVCC, U71
PS_AVTT, U73
'PG_PSGT'
'EN_GT_R'
PL_GT_1V35, U58
PL_GT_1V05, U62
AVCC_R, U63
AUX_R, U61
AVTT_R, U59
'PG_GT_R'
'EN_GT_L'
PL_GT2_1V35, U52
PL_GT2_1V05, U55
AVCC_L, U56
AUX_L, U54
AVTT_L, U53
'PG_GT_L'
'EN_3.3V'
3.3V, U81
3.3V as EN-signa
SC
CPLD
U27
optional
peripheral
voltages
'EN_SFP_SSD'
SFP_SSD, U11
'FMC12V_EN'
12V_FMC_AF, U51
'FMCAF12V_PG'
'EN_A_3V3'
FMCA_3V3, U32
'EN_B_3V3'
FMCB_3V3, U33
'EN_C_3V3'
FMCC_3V3, U34
'EN_D_3V3'
FMCD_3V3, U35
'EN_E_3V3'
FMCE_3V3, U36
'EN_F_3V3'
FMCF_3V3, U42
'EN_AF_1V8'
FMCAF_1V8, U39
'EN_BC_1V8'
FMCBC_1V8, U40
'EN_DE_1V8'
FMCDE_1V8, U41
'DP_EN'
DP_TX_PWR, U29
'SD_EN'
Load-Switch Q3,
3.3V SD-Card
VCC/VCCIO

Figure 18: Power-On sequence diagram

Power Rails

Peripheral Designator	VCC / VCCIO Schematic Name	Voltage	Direction	Pins	Notes
J12	DP_TX_PWR	3.3V	Out	Pin 20	Display-Port Connector
J9A	SFP_SSD	3.3V	Out	Pin T15, T16	SFP+ 2x1 Connector
J9B	SFP_SSD	3.3V	Out	Pin L15, L16	
J13A	VBUS1	5.0V	Out	Pin U1	USB3 Ports
J13B	VBUS2	5.0V	Out	Pin U10	
J11	-	3.3V	Out	Pin 4	MicroSD Card Socket
B1	PSBATT	3.0V	In	Pin +	Battery Holder CR1220
U2	SSD1_3V3_1	3.3V	Out	Pin 2, 4	SSD PCIe connector
	SSD1_3V3_2	3.3V	Out	Pin 70, 72, 74	
	SSD1_3V3_3	3.3V	Out	Pin 12, 14, 16, 18	
U3	DDR_1V2	1.2V	Out	Pin 111, 112, 117, 118, 123, 124, 129, 130, 135, 136, 141, 142, 147, 148, 153, 154, 159, 160, 163	DDR4 SO-DIMM socket
	VPP_SPD	2.5V	Out	Pin 255, 257, 259	

Table 57: Power pin description of peripherals' connectors

XMOD / JTAG Designator	VCC / VCCIO Schematic Name	Voltage	Direction	Pins	Notes
J24	3V3SB	3.3V	Out	Pin 5	Zynq MPSoC JTAG
	PS_1V8	1.8V	Out	Pin 6	
J35	3V3SB	3.3V	Out	Pin 5, 6	SC CPLD JTAG

Table 58: Power pin description of XMOD/JTAG Connector

Main Power	VCC / VCCIO Schematic Name	Voltage	Direction	Pins	Notes
J1	PWR_IN_24V	24V	In	Pin 2, 4	24V Power Jack

Table 59: Power pin description of main power supply connector

FMC Designator	VCC / VCCIO Schematic Name	Voltage	Direction	Pins	Notes
J10	12V_FMC_AF	12.0V	Out	Pin C35, C37	-

	3V3VSB	3.3V	Out	Pin D32	-
	FMCA_3V3	3.3V	Out	Pin D36, D38, D40, C39	-
	FMCAF_1V8	1.8V	Out	Pin E39, G39, H40, F40	-
J21	12V_FMC_AF	12.0V	Out	Pin C35, C37	-
	3V3VSB	3.3V	Out	Pin D32	-
	FMCF_3V3	3.3V	Out	Pin D36, D38, D40, C39	-
	FMCAF_1V8	1.8V	Out	Pin E39, G39, H40, F40	-
J4	12V	12.0V	Out	Pin C35, C37	-
	3V3VSB	3.3V	Out	Pin D32	-
	FMCB_3V3	3.3V	Out	Pin D36, D38, D40, C39	-
	FMCBC_1V8	1.8V	Out	Pin E39, G39, H40, F40	-
J8	12V	12.0V	Out	Pin C35, C37	-
	3V3VSB	3.3V	Out	Pin D32	-
	FMCC_3V3	3.3V	Out	Pin D36, D38, D40, C39	-
	FMCBC_1V8	1.8V	Out	Pin E39, G39, H40, F40	-
J7	12V	12.0V	Out	Pin C35, C37	-
	3V3VSB	3.3V	Out	Pin D32	-
	FMCD_3V3	3.3V	Out	Pin D36, D38, D40, C39	-
	FMCDE_1V8	1.8V	Out	Pin E39, G39, H40, F40	-
J6	12V	12.0V	Out	Pin C35, C37	-
	3V3VSB	3.3V	Out	Pin D32	-
	FMCE_3V3	3.3V	Out	Pin D36, D38, D40, C39	-
	FMCDE_1V8	1.8V	Out	Pin E39, G39, H40, F40	-

Table 60: Power pin description of FMC connectors

FAN Designator	VCC / VCCIO Schematic Name	Voltage	Direction	Pins	Notes
J2	-	12.0V	Out	Pin 2	headers for optional cooling FANs
J23	-	12.0V	Out	Pin 2	
J33	-	12.0V	Out	Pin 2	

Table 61: Power pin description of FAN connectors

Bank Voltages

Bank	Schematic Name	Voltage	Voltage Range
500 (PS MIO)	PS_1V8	1.8V	all bank voltages fixed
501 (PS MIO)	3.3V	3.3V	
502 (PS MIO)	PS_1V8	1.8V	
503 (PS Config)	PS_1V8	1.8V	
504 (PS DDR)	DDR_1V2	1.2V	

64 HP	FMCDE_1V8	1.8V
65 HP	FMCDE_1V8	1.8V
66 HP	FMCDE_1V8	1.8V
67 HP	FMCBC_1V8	1.8V
44 HD	FMCAF_1V8	1.8V
47 HD	FMCBC_1V8	1.8V
48 HD	FMCBC_1V8	1.8V
49 HD	FMCBC_1V8	1.8V
50 HD	FMCBC_1V8	1.8V

Table 62: Zynq MPSoC PS/PL VCCO bank voltages

Variants Currently In Production

Trenz shop TEB9011 overview page	
English page	German page

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference Document	Notes
VIN supply voltage	-0.3	28	V	TEB0911 Schematic REV03	-
VBATT	-0.3	6	V	TPS780180300 data sheet	1.8V typical output
PS GTR receiver input	-0.5	1.1	V	Xilinx DS925 data sheet	-
MGT reference clock input	-0.5	1.3	V	Xilinx DS925 data sheet	supplied from FMC connectors
GTH transcever input voltage	-0.5	1.2	V	Xilinx DS925 data sheet	-
PL I/O input voltage (HP / HD bank)	-0.55	VCCO + 0.55	V	Xilinx DS925 data sheet	PL bank VCCO voltages are fixed at 1.8V
PS I/O input voltage	-0.5	VCCO + 0.55	V	Xilinx DS925 data sheet	see section 'bank voltages' for PS bank VCCO
SC CPLD U27 I/O input voltage	-0.5	3.75	V	Lattice MachXO2 familiy data sheet	-
PLL clock generator input	-0.85	3.8	V	Si5345/44/42 Rev D Data Sheet	supplied through SMA coax J25
Storage temperature	-20	60	°C	TVS Diode Array 82402374 data sheet	-

Table 63: Module absolute maximum ratings

⚠ Assembly variants for higher storage temperature range are available on request.

Recommended Operating Conditions

Parameter	Min	Max	Units	Reference Document	Notes
VIN supply voltage	22	25	V	Schematic REV03	24V nominal
VBATT	2.2	5.5	V	TPS780180300 data sheet	supplied by 3.0V CR1220 battery
PL I/O input voltage (HP / HD bank)	-0.2	VCCO + 0.2	V	Xilinx DS925 data sheet	PL bank VCCO voltages are fixed at 1.8V
PS I/O input voltage	-0.2	VCCO + 0.2	V	Xilinx DS925 data sheet	see section 'bank voltages' for PS bank VCCO
SC CPLD U27 I/O input voltage	-0.3	3.6	V	Lattice MachXO2 familiy data sheet	-
SC CPLD U27 differential I/O input voltage	0	2.605	V	Lattice MachXO2 familiy data sheet	-
Operating temperature	0	60	°C	F455B / Xilinx DS925 data sheet	-

Table 64: Module recommended operating conditions

Please check Xilinx datasheet ... for complete list of absolute maximum and recommended operating ratings.

Operating Temperature Ranges

The TEB0911 board operational temperature range is 0 °C ... 85 °C without FMC cooling fans M1 ... M6 and NGFF M.2 PCIe socket U2.

Physical Dimensions

- Board size: 406mm × 234.30mm. Please download the assembly diagram for exact numbers.
- PCB thickness: 1.65 mm.
- Please download the step model for exact numbers.

All dimensions are given in millimeters.

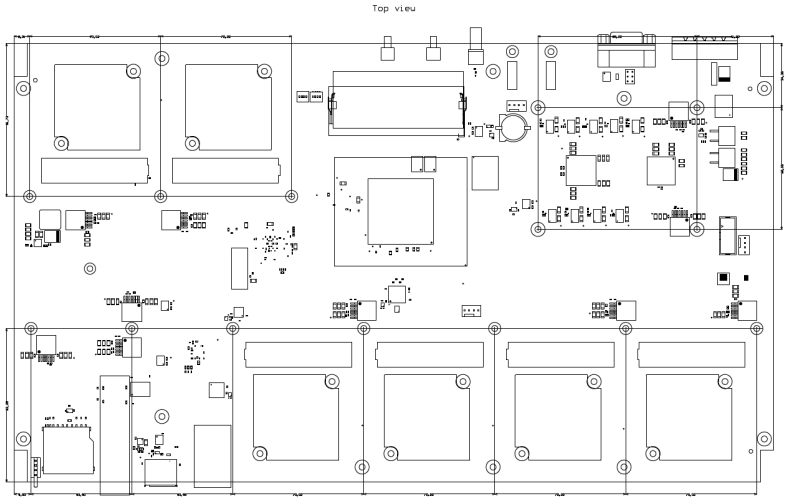


Figure 19: Board physical dimensions drawing

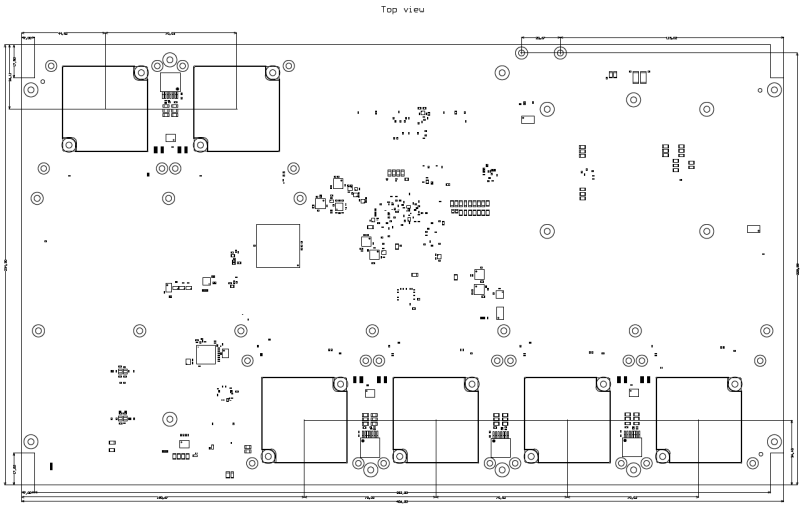


Figure 20: Board physical dimensions drawing

Revision History

Hardware Revision History

Date	Revision	Notes	Link to PCN	Documentation Link
-	03	Current available board revision	-	TEB0911-03
-	02	Second production release	-	TEB0911-02
-	01	First production release	-	TEB0911-01

Table 65: Module hardware revision history

Hardware revision number can be found on the PCB board together with the board model number separated by the dash.

Figure 20: Board hardware revision number

Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• Figure 1: fixed Zynq to FMC IO count to 148
2019-08-27	v.184	John Hartfiel	• typo
2019-05-10	v.183	John Hartfiel	• correction of J8 Pin count description
2018-07-23	v.182	Ali Naseri	• Initial document

--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	

Table 66: Document change history

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Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

02 Sept 2017