

TE0783 CPLD

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Overview

Firmware for PCB CPLD with designator U32. Second CPLD Device in Chain: LCMX02-4000HC

Feature Summary

- Power Management
- Boot Mode
- Reset
- UART
- IO Expender(RGPIO)

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Bank Power	Description
BM2/MIO4 / BM2_MIO4	out	B35	3.3V	Boot Mode Pin to FPGA (SD or QSPI)

BOOTMODE	out	B32	3.3V	B2B UART from MIO15
CONFIGX	in	B33	3.3V	B2B UART to MIO14
CPLD_GPIO0		A3	3.3V	B2B / <i>currently_not_used</i>
CPLD_GPIO1		B1	3.3V	B2B / <i>currently_not_used</i>
CPLD_GPIO2		A1	3.3V	B2B / <i>currently_not_used</i>
CPLD_GPIO3	in	A2	3.3V	B2B, used for Boot Mode
DONE	in	A35	3.3V	FPGA Done signal
EN_1V	out	B3	3.3V	disable/enable module power 1V and all other related voltages
EXT_IO1	inout	A33	EXT_IO_VCC	B2B, RGPIO /
EXT_IO10	inout	B22	EXT_IO_VCC	B2B, RGPIO
EXT_IO11	inout	A24	EXT_IO_VCC	B2B, RGPIO
EXT_IO12	inout	A23	EXT_IO_VCC	B2B, RGPIO
EXT_IO13	inout	B21	EXT_IO_VCC	B2B, RGPIO
EXT_IO14	inout	A28	EXT_IO_VCC	B2B, RGPIO
EXT_IO15	inout	B18	EXT_IO_VCC	B2B, RGPIO
EXT_IO16	inout	A22	EXT_IO_VCC	B2B, RGPIO
EXT_IO17	inout	B8	EXT_IO_VCC	B2B, RGPIO
EXT_IO18	inout	A9	EXT_IO_VCC	B2B, RGPIO
EXT_IO19	inout	A20	EXT_IO_VCC	B2B, RGPIO
EXT_IO2	inout	B24	EXT_IO_VCC	B2B, RGPIO
EXT_IO20	inout	B14	EXT_IO_VCC	B2B, RGPIO
EXT_IO21	inout	A8	EXT_IO_VCC	B2B, RGPIO
EXT_IO22	inout	B7	EXT_IO_VCC	B2B, RGPIO
EXT_IO23	inout	B13	EXT_IO_VCC	B2B, RGPIO
EXT_IO24	inout	A18	EXT_IO_VCC	B2B, RGPIO
EXT_IO25	inout	A5	EXT_IO_VCC	B2B, RGPIO
EXT_IO26	inout	B4	EXT_IO_VCC	B2B, RGPIO
EXT_IO27	inout	A13	EXT_IO_VCC	B2B, RGPIO
EXT_IO28	inout	A17	EXT_IO_VCC	B2B, RGPIO
EXT_IO29	inout	A6	EXT_IO_VCC	B2B, RGPIO
EXT_IO3	inout	A27	EXT_IO_VCC	B2B, RGPIO
EXT_IO30	inout	B5	EXT_IO_VCC	B2B, RGPIO
EXT_IO31	inout	B12	EXT_IO_VCC	B2B, RGPIO
EXT_IO32	inout	A16	EXT_IO_VCC	B2B, RGPIO
EXT_IO33	inout	A7	EXT_IO_VCC	B2B, RGPIO
EXT_IO34	inout	B9	EXT_IO_VCC	B2B, RGPIO
EXT_IO35	inout	A15	EXT_IO_VCC	B2B, RGPIO
EXT_IO36	inout	B15	EXT_IO_VCC	B2B, RGPIO
EXT_IO37	inout	A11	EXT_IO_VCC	B2B, RGPIO
EXT_IO38	inout	A12	EXT_IO_VCC	B2B, RGPIO

EXT_IO39	inout	B16	EXT_IO_VCC	B2B, RGPIO
EXT_IO4	inout	B20	EXT_IO_VCC	B2B, RGPIO
EXT_IO40	inout	A21	EXT_IO_VCC	B2B, RGPIO
EXT_IO5	inout	A31	EXT_IO_VCC	B2B, RGPIO
EXT_IO6	inout	B23	EXT_IO_VCC	B2B, RGPIO
EXT_IO7	inout	A26	EXT_IO_VCC	B2B, RGPIO
EXT_IO8	inout	A25	EXT_IO_VCC	B2B, RGPIO
EXT_IO9	inout	A30	EXT_IO_VCC	B2B, RGPIO
FPGA_CPLD1	in	A40	3.3V	FPGA AB19, RGPIO CLK
FPGA_CPLD2	out	B28	3.3V	FPGA AB20, RGPIO out
FPGA_CPLD3	in	A38	3.3V	FPGA AD20, RGPIO in
FPGA_CPLD4	in	A36	3.3V	FPGA AE20 goes to LED2
JTAGENB	in	B30	3.3V	Enable CPLD JTAG access, otherwise M_... is used as GPIO
LED2	out	B10	EXT_IO_VCC	Status LED D1 red
M_TCK	in	A45	3.3V	JTAG if JTAGENB is high/ currently_not_used
M_TDI	in	A47	3.3V	JTAG if JTAGENB is high/ currently_not_used
M_TDO	out	A48	3.3V	JTAG if JTAGENB is high/ currently_not_used
M_TMS	in	B34	3.3V	JTAG if JTAGENB is high/ currently_not_used
MIO14	out	A44	3.3V	UART out to FPGA
MIO15	in	A42	3.3V	UART in from FPGA
nRST_IN	in	A32	3.3V	Reset from B2B to PS_POR
PG_ALL	in	A46	3.3V	Status power
PROG_B	in	B25	3.3V	Status PROG_B/ currently_not_used
PS_POR	inout	A41	3.3V	open drain as second reset from nRSR_IN/ currently_not_used
NC		B29	3.3V	dummy pin / not connected
NC		B27	3.3V	not connected
NC		A34	3.3V	not connected

Functional Description

JTAG

Set JTAGENB(J3-136) high to get access to CPLD via JTAG, otherwise CPLD JTAG Pins can be used as GPIO.

Power

EN_1V is set to constant high.

Boot Mode

CPLD_GPIO3 (J2-16) is used to set boot Mode Pin BM2_MIO4. Signal is inverted to be compatible with second XMOD on TEBT0782

J2-16	Description
low	SD Boot*
high	QSPI (default)

* not supported with TEBT0782

Reset

nRST_IN drive POR_B as open drain.

U27(TPS3106) or nRST_IN can reset Zynq.

UART

MIO14 is connected to CONFIGX.

BOOTMODE is connected to MIO15.

RGPIO (beta)

RGPIO Master is a 32Bit Remote GPIO Interface to talk with FPGA over 3 lanes. System need RGPIO IP on FPGA side.

- RGPIO CLK is FPGA_CPLD1 (up to 50MHz).
- Output is FPGA_CPLD2
- Input is FPGA_CPLD3

RGPIO from FPGA	Description
0...19	Connected to EXT_IO(even numbers), if RGPIO is activated, otherwise EXTIO is high impedance
20...23	Connected to RGPIO 20...23, if RGPIO is activated.
24...27	Reserved
28...31	Activation code from FPGA. Must match "1010"

RGPIO to FPGA	Description
0...19	Connected to EXT_IO(odd numbers)
20...23	RGPIO 20...23 from FPGA, if RGPIO is activated, otherwise zero
24...27	Reserved
28...31	Activation code to FPGA. Must match "1010"

LED

LED2 D1 Red		
Priority	Blink Sequence	Comment
1	*****	PG_ALL, Power problem
2	*****000	PROG_B, SoC PROGAM_B down


3	***0000	PS_POR, SoC PS_POR_B down
4	***00000	DONE, SoC DONE down
5	user defined	FPGA_CPLD4 connected to LED

Appx. A: Change History and Legal Notices

Revision Changes

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
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