# TE0741 IBERT

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**Error rendering macro 'toc'**

java.lang.RuntimeException: com.ctc.wstx.exc.WstxParsingException: String '--' not allowed in comment (missing '>'?) at [row,col {unknown-source}]: [39,-1115]

## Overview

Xilinx IBERT with previous SI5338 reconfiguration. Lanerate is 6.25GB/s. SI5338 is preconfigured, it's also possible to run default Xilinx IBERT example.

## Key Features

- MGT
- SI5338 initialisation with MCS

## Revision History

| Date | Vivado | Project Built | Authors | Description |
|---|---|---|---|---|
| 2018-04-18 | 2017.4 | TE0741-IBERT_noprebuilt-vivado_2017.4-build_07_20180418084107.zip<br>TE0741-IBERT-vivado_2017.4-build_07_20180418083647.zip | John Hartfiel | • initial release |

## Release Notes and Know Issues

| Issues | Description | Workaround | To be fixed version |
|---|---|---|---|
| --- | --- | --- | --- |

## Requirements

### Software

| Software | Version | Note |
|---|---|---|
| Vivado | 2017.4 | needed |
| SDK | 2017.4 | needed |

### Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

| Module Model | Board Part Short Name | PCB Revision Support | DDR | QSPI Flash | Others | Notes |
|---|---|---|---|---|---|---|
| TE0741-03-070-2IF | 070_2if | REV02, REV03 | --- | 32MB | MGT LR: 6,6 Gb/s | |
| TE0741-03-160-2IF | 160_2if | REV02, REV03 | --- | 32MB | MGT LR: 6,6 Gb/s | |
| TE0741-03-325-2IF | 325_2if | REV02, REV03 | --- | 32MB | MGT LR: 6,6 Gb/s | |
| TE0741-03-410-2IF | 410_2if | REV02, REV03 | --- | 32MB | MGT LR: 6,6 Gb/s | |
| TE0741-03-070-2CF | 070_2cf | REV02, REV03 | --- | 32MB | MGT LR: 6,6 Gb/s | |
| TE0741-03-160-2CF | 160_2cf | REV02, REV03 | --- | 32MB | MGT LR: 6,6 Gb/s | |
| TE0741-03-325-2CF | 325_2cf | REV02, REV03 | --- | 32MB | MGT LR: 6,6 Gb/s | |
| TE0741-03-410-2CF | 410_2cf | REV02, REV03 | --- | 32MB | MGT LR: 6,6 Gb/s | |
| TE0741-03-160-2C1 | 160_2c1 | REV02, REV03 | --- | 32MB | MGT LR: 10,3125 Gb/s | |

Design supports following carriers:

| Carrier Model | Notes |
|---|---|
| TEBA0841 | used as reference carrier |

Additional HW Requirements:

| Additional Hardware | Notes |
|---|---|
| USB Cable for JTAG/UART | Check Carrier Board and Programmer for correct type |
| XMOD Programmer | Carrier Board dependent, only if carrier has no own FTDI |
| Heat sink | It's recommended to use heat sink for this design |

# Content

For general structure and of the reference design, see Project Delivery - AMD devices

## Design Sources

| Type | Location | Notes |
|---|---|---|
| Vivado | <design name>/block_design<br><design name>/constraints<br><design name>/ip_lib<br><design name>/firmware | Vivado Project will be generated by TE Scripts |
| SDK/HSI | <design name>/sw_lib | Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI |
| PetaLinux | <design name>/os/petalinux | PetaLinux template with current configuration |

## Additional Sources

| Type | Location | Notes |
|---|---|---|
| SI5338 Project | \misc\SI5338 | |

## Prebuilt

| File | File-Extension | Description |
|---|---|---|
| BIT-File | *.bit | FPGA (PL Part) Configuration File |
| Diverse Reports | --- | Report files in different formats |
| Hardware-Platform-Specification-Files | *.hdf | Exported Vivado Hardware Specification for SDK/HSI and PetaLinux |
| LabTools Project-File | *.lpr | Vivado Labtools Project File |
| MCS-File | *.mcs | Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only) |
| MMI-File | *.mmi | File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only) |
| Software-Application-File | *.elf | Software Application for Zynq or MicroBlaze Processor Systems |

## Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0741 "IBERT" Reference Design

# Design Flow

⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

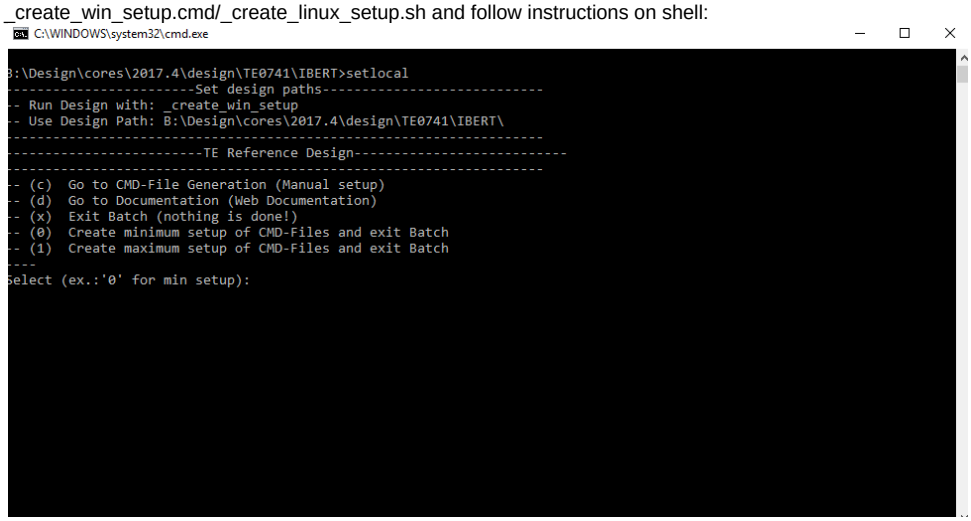
See also:AMD Development Tools#XilinxSoftware-BasicUserGuides

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI.  For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:




2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
    a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
    Note: Select correct one, see TE Board Part Files
5. Create HDF and export to prebuilt folder
    a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
    Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate MCS Firmware (optional):
    a. Create SDK Project with TE Scripts on Vivado TCL: TE::sw_run_sdk
    b. Create "SCU" application
    Note: Select MCS Microblaze and SCU Application
    c. Select Release Built
    d. Regenerate App
7. (optional) Copy "\\workspace\sdk\scu\Release\scu.elf" into "\firmware\microblaze_mcs_0\"
8. Regenerate Vivado Project or Update Bitfile only with "scu.elf"

# Launch

## Programming

> ⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

### QSPI

1. Connect JTAG and power on PCB
2. (if not done) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" or open with "vivado_open_project_guimode.cmd", if generated.
3. Type on Vivado Console: TE::pr_program_flash_mcsfile -swapp
   Note: Alternative use SDK or setup Flash on Vivado manually
4. Reboot (if not done automatically)

### SD

Not used on this Example.

## JTAG

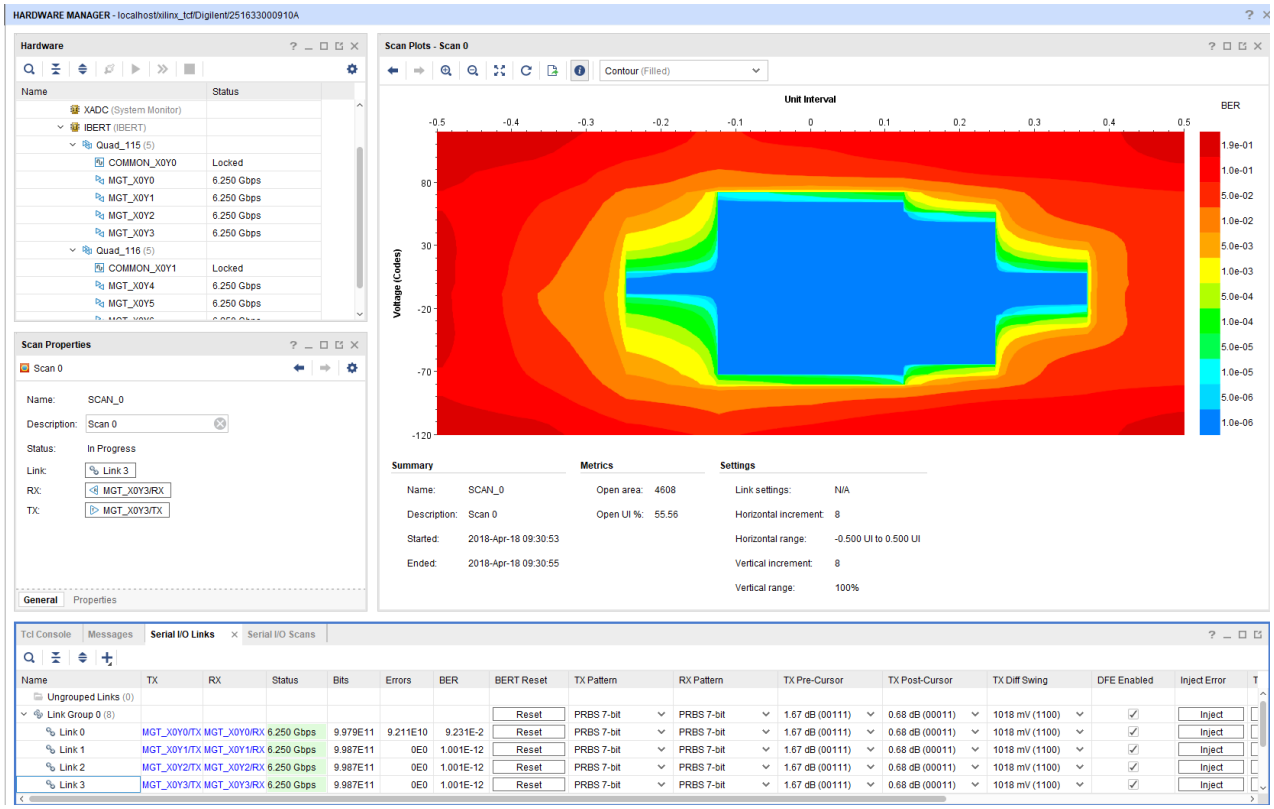
1. Connect JTAG and power on PCB
2. Open Vivado HW Manager
3. Program FPGA with Bitfile from "prebuilt\hardware\<short dir>"

# Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Power on PCB
   Note: FPGA Loads Bitfile from Flash,MCS Firmware configure SI5338 and starts IBERT.
   Do not reboot, if Bitfile programming over JTAG is used as programming method.
4. LEDS:
   a. D1 (red) ON  MGT Power Good
   b. D2 (green) ON MCS SI configuration finished (System Reset is off)

## Vivado HW Manager:

1. Open Vivado HW-Manager
2. "Refresh device" is needed after Bitfile programming, because MCS reconfigure SI5338 and enables IBERT a little bit later.
   a. loopback depends on TEB0841 Revision an connection

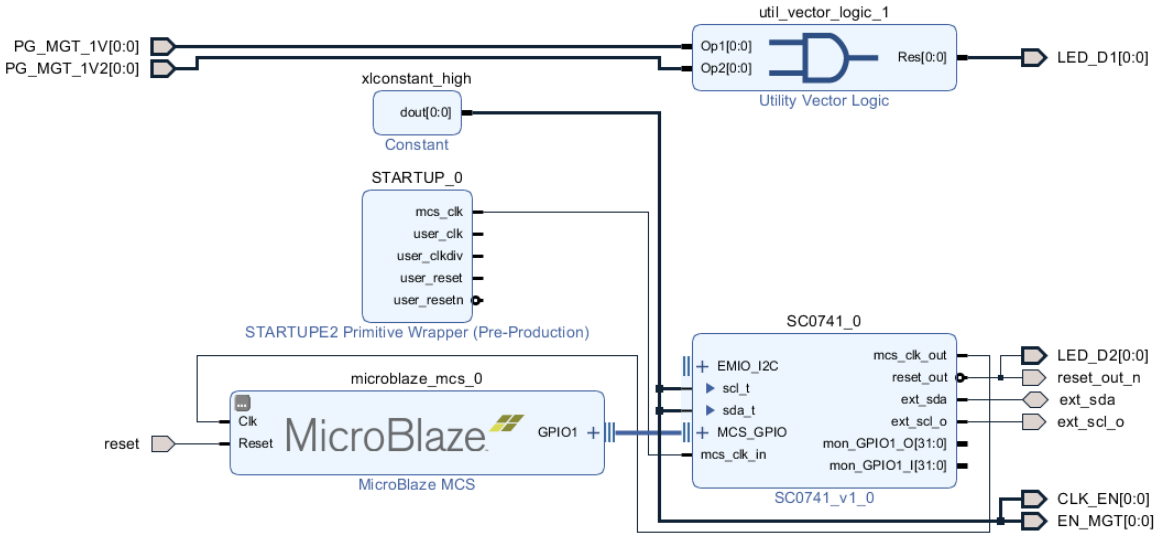



| IBERT | Component Name | Net Name | TEB0841 |
|---|---|---|---|

| | | | |
|---|---|---|---|
| X0Y0 | 115-0 | MGT4 | loop back RX/TX. Note: N.C. on TEB0841-01, use  internal loopback |
| X0Y1 | 115-1 | MGT5 | loopback over SD Pin header possible |
| X0Y2 | 115-2 | MGT6 | loop back RX/TX |
| X0Y3 | 115-3 | MGT7 | loop back RX/TX |
| X0Y4 | 116-0 | MGT0 | loop back RX/TX |
| X0Y5 | 116-1 | MGT1 | loop back RX/TX |
| X0Y6 | 116-2 | MGT2 | loop back RX/TX |
| X0Y7 | 116-3 | MGT3 | loopback over sfp possible |

# System Design - Vivado

## Block Design




## HDL

- IBERT_top.v
- ibert xci IPs

## Constrains

### Basic module constrains

**_i_bitgen_common.xdc**

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

## Design specific constrain

**_i_io.xdc**

```
#LED
set_property PACKAGE_PIN D26 [get_ports {LED_D1[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LED_D1[0]}]
set_property PACKAGE_PIN E26 [get_ports {LED_D2[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LED_D2[0]}]
#MGT Power
set_property PACKAGE_PIN G25 [get_ports {PG_MGT_1V2[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {PG_MGT_1V2[0]}]
set_property PACKAGE_PIN K23 [get_ports {PG_MGT_1V[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {PG_MGT_1V[0]}]
set_property PACKAGE_PIN H22 [get_ports {EN_MGT[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {EN_MGT[0]}]
#SI5338 CLK
set_property PACKAGE_PIN C26 [get_ports {CLK_EN[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {CLK_EN[0]}]
#I2C PLL SI5338
set_property PACKAGE_PIN A20 [get_ports ext_scl_o]
set_property IOSTANDARD LVCMOS33 [get_ports ext_scl_o]
set_property PACKAGE_PIN B21 [get_ports ext_sda]
set_property IOSTANDARD LVCMOS33 [get_ports ext_sda]
```

**_i_ibert_7series_gtx_0.xdc**

```
# file: ibert_7series_gtx_0.xdc
##############################################################################
##   ____  ____
##  /   /\/   /
## /___/  \  /    Vendor: Xilinx
## \   \   \/     Version : 2012.3
##  \   \         Application : IBERT 7Series
##  /   /         Filename : example_ibert_7series_gtx_0.xdc
## /___/   /\
## \   \  /  \
##  \___\/\___\
```

```
##
##
##
## Generated by Xilinx IBERT 7Series
##************************************************************************

##
## System clock Divider paramter values
##
set_property CLKFBOUT_MULT_F 10.000 [get_cells u_ibert_core/inst/SYSCLK_DIVIDER.U_GT_MMCM]
set_property DIVCLK_DIVIDE 1 [get_cells u_ibert_core/inst/SYSCLK_DIVIDER.U_GT_MMCM]
set_property CLKIN1_PERIOD 10.0 [get_cells u_ibert_core/inst/SYSCLK_DIVIDER.U_GT_MMCM]
set_property CLKOUT0_DIVIDE_F 10.000 [get_cells u_ibert_core/inst/SYSCLK_DIVIDER.U_GT_MMCM]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_pins u_ibert_core/inst/SYSCLK_DIVIDER.U_GT_MMCM/CLKIN1]

##
## Icon Constraints
##
create_clock -name J_CLK -period 30 [get_pins -of_objects [get_cells u_ibert_core/inst/bscan_inst/SERIES7_BSCAN.
bscan_inst] -filter {name =~ *DRCK}]
create_clock -name D_CLK -period 10.0 [get_ports SYSCLKP_I]
set_clock_groups -group [get_clocks D_CLK] -asynchronous
set_clock_groups -group [get_clocks J_CLK] -asynchronous

##
## Clock Constraints for MGT refclk
##
create_clock -name REFCLK0_1 -period 8.0 [get_ports GTREFCLK1P_I[0]]
set_clock_groups -group [get_clocks -include_generated_clocks REFCLK0_1] -asynchronous
create_clock -name REFCLK0_0 -period 8.0 [get_ports GTREFCLK0P_I[0]]
set_clock_groups -group [get_clocks -include_generated_clocks REFCLK0_0] -asynchronous

##
## TX/RX out clock constraints
##
# GT X0Y0
create_clock -name Q0_RXCLK0 -period 5.12 [get_pins {u_ibert_core/inst/QUAD[0].u_q/CH[0].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q0_RXCLK0] -asynchronous
create_clock -name  Q0_TX0 -period 5.12 [get_pins {u_ibert_core/inst/QUAD[0].u_q/CH[0].u_ch/u_gtxe2_channel
/TXOUTCLK}]
set_clock_groups -group [get_clocks Q0_TX0] -asynchronous
# GT X0Y1
create_clock -name Q0_RXCLK1 -period 5.12 [get_pins {u_ibert_core/inst/QUAD[0].u_q/CH[1].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q0_RXCLK1] -asynchronous
# GT X0Y2
create_clock -name Q0_RXCLK2 -period 5.12 [get_pins {u_ibert_core/inst/QUAD[0].u_q/CH[2].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q0_RXCLK2] -asynchronous
# GT X0Y3
create_clock -name Q0_RXCLK3 -period 5.12 [get_pins {u_ibert_core/inst/QUAD[0].u_q/CH[3].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q0_RXCLK3] -asynchronous
# GT X0Y4
create_clock -name Q1_RXCLK0 -period 5.12 [get_pins {u_ibert_core/inst/QUAD[1].u_q/CH[0].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q1_RXCLK0] -asynchronous
create_clock -name  Q1_TX0 -period 5.12 [get_pins {u_ibert_core/inst/QUAD[1].u_q/CH[0].u_ch/u_gtxe2_channel
/TXOUTCLK}]
set_clock_groups -group [get_clocks Q1_TX0] -asynchronous
```

```
# GT X0Y5
create_clock -name Q1_RXCLK1 -period 5.12 [get_pins {u_ibert_core/inst/QUAD[1].u_q/CH[1].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q1_RXCLK1] -asynchronous
# GT X0Y6
create_clock -name Q1_RXCLK2 -period 5.12 [get_pins {u_ibert_core/inst/QUAD[1].u_q/CH[2].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q1_RXCLK2] -asynchronous
# GT X0Y7
create_clock -name Q1_RXCLK3 -period 5.12 [get_pins {u_ibert_core/inst/QUAD[1].u_q/CH[3].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q1_RXCLK3] -asynchronous

##
## System clock pin locs and timing constraints
##
set_property PACKAGE_PIN F22 [get_ports SYSCLKP_I]
set_property IOSTANDARD LVDS_25 [get_ports SYSCLKP_I]
set_property PACKAGE_PIN E23 [get_ports SYSCLKN_I]
set_property IOSTANDARD LVDS_25 [get_ports SYSCLKN_I]

##
## GTXE2 Channel and Common Loc constraints
##
set_property LOC GTXE2_CHANNEL_X0Y0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[0].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_CHANNEL_X0Y1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[1].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_CHANNEL_X0Y2 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[2].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_CHANNEL_X0Y3 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[3].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_COMMON_X0Y0 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property LOC GTXE2_CHANNEL_X0Y4 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[0].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_CHANNEL_X0Y5 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[1].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_CHANNEL_X0Y6 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[2].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_CHANNEL_X0Y7 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[3].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_COMMON_X0Y1 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]

##
## BUFH Loc constraints for TX/RX userclks
##
set_property LOC BUFHCE_X1Y36 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_clocking/local_txusr.NON_K7.
u_txusr]
set_property LOC BUFHCE_X1Y37 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr0]
set_property LOC BUFHCE_X1Y38 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr1]
set_property LOC BUFHCE_X1Y39 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr2]
set_property LOC BUFHCE_X1Y40 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr3]
set_property LOC BUFHCE_X1Y48 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_clocking/local_txusr.NON_K7.
u_txusr]
set_property LOC BUFHCE_X1Y49 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr0]
set_property LOC BUFHCE_X1Y50 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr1]
set_property LOC BUFHCE_X1Y51 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr2]
set_property LOC BUFHCE_X1Y52 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr3]


##
```

```
## MGT reference clock BUFFERS location constraints
##
set_property LOC IBUFDS_GTE2_X0Y2 [get_cells u_buf_q1_clk0]
set_property LOC IBUFDS_GTE2_X0Y3 [get_cells u_buf_q1_clk1]

##
## Asynchronous constraints for Userclks and systemclock clock groups
##
#set_clock_groups -group [get_clocks Q*_RXCLK*] -group [get_clocks Q*_TX*] -asynchronous
#set_clock_groups -group [get_clocks D_CLK*] -group [get_clocks Q*_TX*] -asynchronous
#set_clock_groups -group [get_clocks Q*_RXCLK*] -group [get_clocks D_CLK*] -asynchronous
#set_clock_groups -group [get_generated_clocks -of_objects [get_pins u_ibert_core/inst/SYSCLK_DIVIDER.U_GT_MMCM
/CLKOUT0]] -group [get_clocks Q*_TX*] -asynchronous
#set_clock_groups -group [get_clocks Q*_RXCLK*] -group [get_generated_clocks -of_objects [get_pins u_ibert_core
/inst/SYSCLK_DIVIDER.U_GT_MMCM/CLKOUT0]] -asynchronous

##
## Set Case Analysis constraints for fabric clock calculation
##
#MUX select QPLLREFCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/u_common/U_COMPLEX_REGS/reg_202/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[2]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[0].u_q/u_common/U_COMPLEX_REGS/reg_202/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[1]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/u_common/U_COMPLEX_REGS/reg_202/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[0]/Q ]
#MUX select CPLLREFCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[6]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[5]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[4]/Q ]
#MUX select RXRATE:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_216/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[5]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_216/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[4]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_216/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[3]/Q ]
#MUX select TXRATE:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[8]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[7]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[6]/Q ]
#MUX select RXOUTCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[15]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[14]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[13]/Q ]
#MUX select TXOUTCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[2]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[1]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[0]/Q ]
```

```
#MUX select QPLLREFCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/u_common/U_COMPLEX_REGS/reg_202/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[2]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[1].u_q/u_common/U_COMPLEX_REGS/reg_202/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[1]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/u_common/U_COMPLEX_REGS/reg_202/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[0]/Q ]
#MUX select CPLLREFCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[6]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[5]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[4]/Q ]
#MUX select RXRATE:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_216/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[5]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_216/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[4]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_216/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[3]/Q ]
#MUX select TXRATE:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[8]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[7]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[6]/Q ]
#MUX select RXOUTCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[15]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[14]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[13]/Q ]
#MUX select TXOUTCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[2]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[1]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[0]/Q ]

##
## Attribute values for GTXE2 Channel and Common instances
##
##
## Attribute Values for QUAD[0] - Channel
##

 ##------Comma Detection and Alignment---------
set_property ALIGN_COMMA_DOUBLE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_COMMA_ENABLE 10'b0001111111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ALIGN_COMMA_WORD 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_MCOMMA_DET "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_MCOMMA_VALUE 10'b1010000011 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ALIGN_PCOMMA_DET "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_PCOMMA_VALUE 10'b0101111100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
```

```
set_property DEC_MCOMMA_DETECT "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property DEC_PCOMMA_DETECT "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property DEC_VALID_COMMA_ONLY "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property DMONITOR_CFG 24'h000A01 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##--------------Channel Bonding--------------
set_property CBCC_DATA_SOURCE_SEL "DECODED" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_KEEP_ALIGN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_MAX_SKEW 7 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_LEN 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_1 10'b0101111100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_1 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_USE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------Clock Correction------------
set_property CLK_COR_KEEP_IDLE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_MAX_LAT 19.0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_MIN_LAT 15.0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_PRECEDENCE "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_CORRECT_USE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_REPEAT_WAIT 0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_LEN 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_1 10'b0100011100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_1 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_USE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------Channel PLL----------------------
set_property CPLL_CFG 24'hBC07DC [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_FBDIV 5 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_FBDIV_45 5 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_INIT_CFG 24'h00001E [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_LOCK_CFG 16'h01C0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_REFCLK_DIV 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXOUT_DIV 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXOUT_DIV 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------------Eyescan--------------
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set_property ES_CONTROL 6'b000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_ERRDET_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_EYE_SCAN_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_HORZ_OFFSET 12'h000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_PMA_CFG 10'b0000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_PRESCALE 5'b00000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_QUALIFIER 80'h00000000000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ES_QUAL_MASK 80'h00000000000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ES_SDATA_MASK 80'h00000000000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ES_VERT_OFFSET 9'b000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property FTS_DESKEW_SEQ_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property FTS_LANE_DESKEW_CFG 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property FTS_LANE_DESKEW_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property GEARBOX_MODE 3'b000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property OUTREFCLK_SEL_INV 2'b11 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PCS_PCIE_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PCS_RSVD_ATTR 48'h000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PMA_RSV 32'h00018480 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PMA_RSV2 16'h2070 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PMA_RSV3 2'b00 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_BIAS_CFG 12'b000000000100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------Rx Elastic Buffer and Phase alignment-------------
set_property RXBUF_ADDR_MODE "FAST" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_EIDLE_HI_CNT 4'b1000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_EIDLE_LO_CNT 4'b0000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_BUFFER_CFG 6'b000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_RESET_ON_CB_CHANGE "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXBUF_RESET_ON_COMMAALIGN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXBUF_RESET_ON_EIDLE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_RESET_ON_RATE_CHANGE "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXBUFRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_THRESH_OVFLW 61 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_THRESH_OVRD "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_THRESH_UNDFLW 4 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDLY_CFG 16'h001F [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDLY_LCFG 9'h030 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDLY_TAP_CFG 16'h0000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------RX driver, OOB signalling, Coupling and Eq., CDR------------
set_property RXCDR_CFG 72'h03800023FF10200020 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXCDRFREQRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_FR_RESET_ON_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_HOLD_DURING_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_LOCK_CFG 6'b010101 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_PH_RESET_ON_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDRPHRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDFELPMRESET_TIME 7'b0001111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXOOB_CFG 7'b0000110 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------------------RX Interface-------------------------
set_property RX_INT_DATAWIDTH 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DATA_WIDTH 32 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
```

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set_property RX_CLKMUX_PD 1'b1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CLK25_DIV 5 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CM_SEL 2'b11 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CM_TRIM 3'b100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DDI_SEL 6'b000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DEBUG_CFG 12'b000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------RX Decision Feedback Equalizer(DFE)-------------
set_property RX_DEFER_RESET_BUF_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_GAIN_CFG 23'h020FEA [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H2_CFG 12'b000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H3_CFG 12'b000001000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H4_CFG 11'b00011110000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H5_CFG 11'b00011100000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_LPM_HOLD_DURING_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_KL_CFG 13'b0000011111110 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_KL_CFG2 32'h3010D90C [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_LPM_CFG 16'h0954 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_OS_CFG 13'b0000010000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_UT_CFG 17'b10001111000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_VP_CFG 17'b00011111100000011 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_XYD_CFG 13'b0000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DISPERR_SEQ_MATCH "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##----------------------RX Gearbox---------------------------
set_property RXGEARBOX_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXISCANRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXLPM_HF_CFG 14'b00000011110000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXLPM_LF_CFG 14'b00000011110000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXPCSRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPH_CFG 24'h000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPHDLY_CFG 24'h084020 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPH_MONITOR_SEL 5'b00000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPMARESET_TIME 5'b00011 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##----------------------PRBS Detection-----------------------
set_property RXPRBS_ERR_LOOPBACK 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_SIG_VALID_DLY 10 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXSLIDE_AUTO_WAIT 7 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXSLIDE_MODE "off" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_XCLK_SEL "RXREC" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------RX Attributes for PCI Express/SATA/SAS----------
set_property PD_TRANS_TIME_FROM_P2 12'h03c [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PD_TRANS_TIME_NONE_P2 8'h3c [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PD_TRANS_TIME_TO_P2 8'h64 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SAS_MAX_COM 64 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SAS_MIN_COM 36 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_BURST_SEQ_LEN 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_BURST_VAL 3'b100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_CPLL_CFG "VCO_3000MHZ" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_EIDLE_VAL 3'b100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MAX_BURST 8 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MAX_INIT 21 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
```

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set_property SATA_MAX_WAKE 7 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MIN_BURST 4 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MIN_INIT 12 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MIN_WAKE 4 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SHOW_REALIGN_COMMA "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TERM_RCAL_CFG 5'b10000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TERM_RCAL_OVRD 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TRANS_TIME_RATE 8'h0E [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TST_RSV 32'h00000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------TX Buffering and Phase Alignment----------------
set_property TXBUF_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXBUF_RESET_ON_RATE_CHANGE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]

 ##-----------------------TX Interface------------------------
set_property TX_DATA_WIDTH 32 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_DEEMPH0 5'b00000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_DEEMPH1 5'b00000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXDLY_CFG 16'h001F [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXDLY_LCFG 9'h030 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXDLY_TAP_CFG 16'h0000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_INT_DATAWIDTH 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_CLKMUX_PD 1'b1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_CLK25_DIV 5 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##--------------TX Driver and OOB Signalling------------------
set_property TX_EIDLE_ASSERT_DELAY 3'b110 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_EIDLE_DEASSERT_DELAY 3'b100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_LOOPBACK_DRIVE_HIZ "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MAINCURSOR_SEL 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_DRIVE_MODE "DIRECT" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------------------TX Gearbox---------------------------
set_property TXGEARBOX_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##----------------TX Attributes for PCI Express---------------
set_property TX_MARGIN_FULL_0 7'b1001110 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_1 7'b1001001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_2 7'b1000101 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_3 7'b1000010 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_4 7'b1000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_0 7'b1000110 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_1 7'b1000100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_2 7'b1000010 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_3 7'b1000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_4 7'b1000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPCSRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPH_CFG 16'h0780 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPHDLY_CFG 24'h084020 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPH_MONITOR_SEL 5'b00000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPMARESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_PREDRIVER_MODE 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_QPI_STATUS_EN 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_RXDETECT_CFG 14'h1832 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_RXDETECT_REF 3'b100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_XCLK_SEL "TXOUT" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property UCODEER_CLR 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
##
## Attribute Values for QUAD[0] - Common
##
```

```
set_property BIAS_CFG 64'h0000040000001000 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property COMMON_CFG 32'h00000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_CFG 27'h06801C1 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_CLKOUT_CFG 4'b0000 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_COARSE_FREQ_OVRD 6'b010000 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_COARSE_FREQ_OVRD_EN 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_CP 10'b0000011111 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_CP_MONITOR_EN 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_DMONITOR_SEL 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_FBDIV_MONITOR_EN 1'b1 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_INIT_CFG 24'h000028 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_LOCK_CFG 16'h21E8 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_LPF 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_REFCLK_DIV 2 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
##
## Attribute Values for QUAD[1] - Channel
##

 ##------Comma Detection and Alignment---------
set_property ALIGN_COMMA_DOUBLE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_COMMA_ENABLE 10'b0001111111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ALIGN_COMMA_WORD 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_MCOMMA_DET "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_MCOMMA_VALUE 10'b1010000011 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ALIGN_PCOMMA_DET "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_PCOMMA_VALUE 10'b0101111100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property DEC_MCOMMA_DETECT "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property DEC_PCOMMA_DETECT "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property DEC_VALID_COMMA_ONLY "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property DMONITOR_CFG 24'h000A01 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##--------------Channel Bonding--------------
set_property CBCC_DATA_SOURCE_SEL "DECODED" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_KEEP_ALIGN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_MAX_SKEW 7 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_LEN 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_1 10'b0101111100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_1 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_USE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------Clock Correction------------
set_property CLK_COR_KEEP_IDLE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
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set_property CLK_COR_MAX_LAT 19.0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_MIN_LAT 15.0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_PRECEDENCE "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_CORRECT_USE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_REPEAT_WAIT 0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_LEN 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_1 10'b0100011100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_1 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_USE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------Channel PLL----------------------
set_property CPLL_CFG 24'hBC07DC [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_FBDIV 5 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_FBDIV_45 5 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_INIT_CFG 24'h00001E [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_LOCK_CFG 16'h01C0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_REFCLK_DIV 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXOUT_DIV 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXOUT_DIV 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------------Eyescan--------------
set_property ES_CONTROL 6'b000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_ERRDET_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_EYE_SCAN_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_HORZ_OFFSET 12'h000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_PMA_CFG 10'b0000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_PRESCALE 5'b00000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_QUALIFIER 80'h00000000000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ES_QUAL_MASK 80'h00000000000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ES_SDATA_MASK 80'h00000000000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ES_VERT_OFFSET 9'b000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property FTS_DESKEW_SEQ_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property FTS_LANE_DESKEW_CFG 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property FTS_LANE_DESKEW_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property GEARBOX_MODE 3'b000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property OUTREFCLK_SEL_INV 2'b11 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PCS_PCIE_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PCS_RSVD_ATTR 48'h000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PMA_RSV 32'h00018480 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PMA_RSV2 16'h2070 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PMA_RSV3 2'b00 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_BIAS_CFG 12'b000000000100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------Rx Elastic Buffer and Phase alignment-------------
set_property RXBUF_ADDR_MODE "FAST" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_EIDLE_HI_CNT 4'b1000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_EIDLE_LO_CNT 4'b0000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_BUFFER_CFG 6'b000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_RESET_ON_CB_CHANGE "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
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/u_gtxe2_channel]
set_property RXBUF_RESET_ON_COMMAALIGN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXBUF_RESET_ON_EIDLE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_RESET_ON_RATE_CHANGE "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXBUFRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_THRESH_OVFLW 61 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_THRESH_OVRD "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_THRESH_UNDFLW 4 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDLY_CFG 16'h001F [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDLY_LCFG 9'h030 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDLY_TAP_CFG 16'h0000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------RX driver, OOB signalling, Coupling and Eq., CDR------------
set_property RXCDR_CFG 72'h03800023FF10200020 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXCDRFREQRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_FR_RESET_ON_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_HOLD_DURING_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_LOCK_CFG 6'b010101 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_PH_RESET_ON_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDRPHRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDFELPMRESET_TIME 7'b0001111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXOOB_CFG 7'b0000110 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##----------------------RX Interface-------------------------
set_property RX_INT_DATAWIDTH 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DATA_WIDTH 32 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CLKMUX_PD 1'b1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CLK25_DIV 5 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CM_SEL 2'b11 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CM_TRIM 3'b100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DDI_SEL 6'b000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DEBUG_CFG 12'b000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------RX Decision Feedback Equalizer(DFE)-------------
set_property RX_DEFER_RESET_BUF_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_GAIN_CFG 23'h020FEA [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H2_CFG 12'b000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H3_CFG 12'b000001000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H4_CFG 11'b00011110000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H5_CFG 11'b00011100000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_LPM_HOLD_DURING_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_KL_CFG 13'b0000011111110 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_KL_CFG2 32'h3010D90C [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_LPM_CFG 16'h0954 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_OS_CFG 13'b0000010000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_UT_CFG 17'b10001111000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_VP_CFG 17'b00011111100000011 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_XYD_CFG 13'b0000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DISPERR_SEQ_MATCH "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##----------------------RX Gearbox---------------------------
set_property RXGEARBOX_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXISCANRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
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set_property RXLPM_HF_CFG 14'b00000011110000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXLPM_LF_CFG 14'b00000011110000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXPCSRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPH_CFG 24'h000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPHDLY_CFG 24'h084020 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPH_MONITOR_SEL 5'b00000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPMARESET_TIME 5'b00011 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------------------PRBS Detection-----------------------
set_property RXPRBS_ERR_LOOPBACK 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_SIG_VALID_DLY 10 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXSLIDE_AUTO_WAIT 7 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXSLIDE_MODE "off" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_XCLK_SEL "RXREC" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------RX Attributes for PCI Express/SATA/SAS----------
set_property PD_TRANS_TIME_FROM_P2 12'h03c [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PD_TRANS_TIME_NONE_P2 8'h3c [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PD_TRANS_TIME_TO_P2 8'h64 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SAS_MAX_COM 64 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SAS_MIN_COM 36 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_BURST_SEQ_LEN 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_BURST_VAL 3'b100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_CPLL_CFG "VCO_3000MHZ" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_EIDLE_VAL 3'b100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MAX_BURST 8 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MAX_INIT 21 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MAX_WAKE 7 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MIN_BURST 4 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MIN_INIT 12 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MIN_WAKE 4 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SHOW_REALIGN_COMMA "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TERM_RCAL_CFG 5'b10000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TERM_RCAL_OVRD 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TRANS_TIME_RATE 8'h0E [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TST_RSV 32'h00000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------TX Buffering and Phase Alignment----------------
set_property TXBUF_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXBUF_RESET_ON_RATE_CHANGE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]

 ##-----------------------TX Interface-------------------------
set_property TX_DATA_WIDTH 32 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_DEEMPH0 5'b00000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_DEEMPH1 5'b00000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXDLY_CFG 16'h001F [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXDLY_LCFG 9'h030 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXDLY_TAP_CFG 16'h0000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_INT_DATAWIDTH 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_CLKMUX_PD 1'b1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_CLK25_DIV 5 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##--------------TX Driver and OOB Signalling------------------
set_property TX_EIDLE_ASSERT_DELAY 3'b110 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_EIDLE_DEASSERT_DELAY 3'b100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_LOOPBACK_DRIVE_HIZ "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MAINCURSOR_SEL 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_DRIVE_MODE "DIRECT" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
```

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 ##-----------------------TX Gearbox--------------------------
set_property TXGEARBOX_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##----------------TX Attributes for PCI Express---------------
set_property TX_MARGIN_FULL_0 7'b1001110 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_1 7'b1001001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_2 7'b1000101 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_3 7'b1000010 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_4 7'b1000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_0 7'b1000110 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_1 7'b1000100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_2 7'b1000010 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_3 7'b1000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_4 7'b1000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPCSRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPH_CFG 16'h0780 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPHDLY_CFG 24'h084020 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPH_MONITOR_SEL 5'b00000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPMARESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_PREDRIVER_MODE 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_QPI_STATUS_EN 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_RXDETECT_CFG 14'h1832 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_RXDETECT_REF 3'b100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_XCLK_SEL "TXOUT" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property UCODEER_CLR 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
##
## Attribute Values for QUAD[1] - Common
##
set_property BIAS_CFG 64'h0000040000001000 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property COMMON_CFG 32'h00000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_CFG 27'h06801C1 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_CLKOUT_CFG 4'b0000 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_COARSE_FREQ_OVRD 6'b010000 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_COARSE_FREQ_OVRD_EN 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_CP 10'b0000011111 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_CP_MONITOR_EN 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_DMONITOR_SEL 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_FBDIV_MONITOR_EN 1'b1 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_INIT_CFG 24'h000028 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_LOCK_CFG 16'h21E8 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_LPF 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_REFCLK_DIV 2 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
```

# Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

## Application

### SCU

MCS Firmware to configure SI5338 and Reset System.

Template location: \sw_lib\sw_apps\scu

# Additional Software

## SI5338

Download ClockBuilder Desktop for SI5338

1. Install and start ClockBuilder
2. Select SI5338
3. Options  Open register map file
   Note: File location <design name>/misc/Si5338/RegisterMap.txt
4. Modify settings
5. Options  save C code header files
6. Replace Header files from SCU template with generated file

# Appx. A: Change History and Legal Notices

## Document Change History

To get content of older revision  got to "Change History"  of this page and select older document revision number.

| Date | Document Revision | Authors | Description |
|---|---|---|---|
| **Error rendering macro 'page-info'**<br>Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core. | **Error rendering macro 'page-info'**<br>Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang. | **Error rendering macro 'page-info'**<br>Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com. | • description update |

| | | | |
|---|---|---|---|
| ContentEntityObject] [interface com.atlassian. user.User, class java.lang. String, class com.atlassian. confluence.core. ContentEntityObject] | String, class com.atlassian. confluence.core. ContentEntityObject]<br><br>Unknown macro: 'metadata' | atlassian.confluence.core. ContentEntityObject] [interface com.atlassian. user.User, class java.lang. String, class com.atlassian. confluence.core. ContentEntityObject] | |
| 18 Apr 2018 | v.2 | John Hartfiel | • Release 2017.4 |
| 2018-04-18 | v.1 | **Error rendering macro 'page-info'**<br><br>Ambiguous method overloading for method jdk. proxy279.$Proxy4022#has ContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian. confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian. confluence.user. ConfluenceUser, class java. lang.String, class com. atlassian.confluence.core. ContentEntityObject] [interface com.atlassian. user.User, class java.lang. String, class com.atlassian. confluence.core. ContentEntityObject] | • Initial release |

| | | | |
|---|---|---|---|
| | All | **Error rendering macro 'page-info'**<br><br>Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] | |

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

**Error rendering macro 'page-info'**

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]