

# TEF0008 TRM

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## Overview

The Trenc Electronic TEF0008 is a FPGA to Mezzanine Card (FMC) based on VITA 57.1 FMC HPC Standard, with four SFP+ 10Gb ports for fiber optical SFP modules. It is intended for use on a FMC HPC carrier and can not be used stand-alone.

## Key Features

- Four SFP+ 10Gb ports
- HPC FMC connector

- Low jitter programmable clock generator
- Intel(Altera) Max10 FPGA 10M08SAU169C8G
- Status LED (green)

Block Diagram

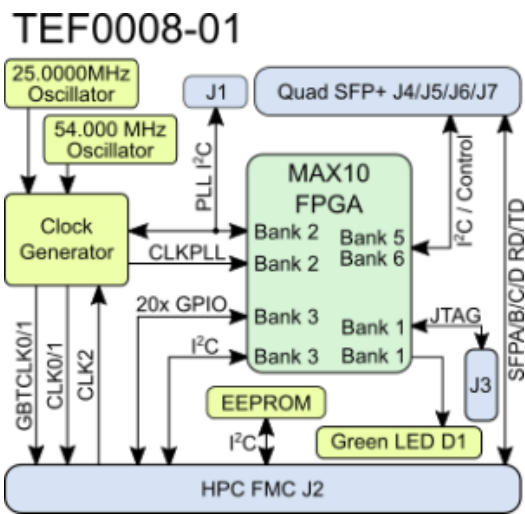


Figure 1: TEF0008 block diagram.

Main Components

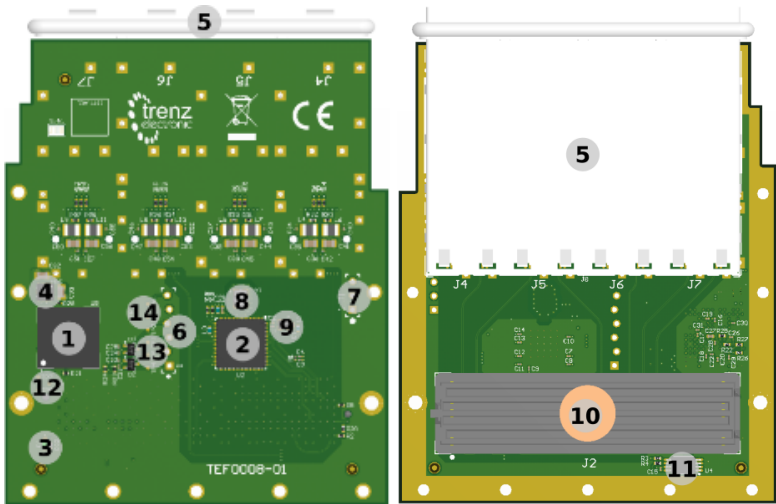


Figure 2: TEF0008 FMC overview.

Table 1: TEF0008 main components.

1. MAX10 FPGA, U5
2. Programmable low jitter clock generator Si5354A, U2
3. Status LED (green), D1
4. 3.3V to 1.8V DCDC converter, U6
5. Quad SFP+ cage and connectors, J4-J7
6. 1x6 pin header for JTAG programming of FPGA (3.3V), J3
7. 1x3 pin header for I<sup>2</sup>C (1.8V), J1
8. XTAL 54.0000 MHz (CX3225SB), Y1
9. Oszillator 25.000000 MHz (SiT8008B), U1
10. HPC FMC connector, J2
11. 128KBit EEPROM, U4
12. Testpoints Max10, TP7-TP9
13. Testpoints JTAG, TP1-TP4
14. Testpoints Power, TP5, TP6, TP10

## Initial Delivery State

| Storage device name             | Content    | Notes                                                                      |
|---------------------------------|------------|----------------------------------------------------------------------------|
| Max10 FPGA 10M08SAU169C8G       | Programmed | U5. Level shifter and controller functions.                                |
| Clock generator<br>Si5345A-B-GM | Programmed | U2. OUT0 25MHz, OUT2 125MHz, OUT7 156.25 MHz, OUT8 156.25MHz, OUT9 125MHz. |
| EEPROM<br>24LC128-I/ST          | empty      | U4, IPMI and VITA57.1 compatible.                                          |

**Table 1:** Initial delivery state of programmable devices on the module.

## Boot Process

The MAX10 FPGA boots from its internal configuration flash memory, which is programmable via JTAG (J3).

## Signals, Interfaces and Pins

### Board to Board (B2B) I/Os

I/O signals connected to the FPGA I/O bank and B2B connector:

| Bank | Type   | B2B Connector | I/O Signal Count | Bank Voltage | Notes                          |
|------|--------|---------------|------------------|--------------|--------------------------------|
| 3    | GPI/Os | J2            | 20 I/Os          | VADJ         | Supplied by the carrier board. |

**Table 2:** General overview of I/O signals connected to the B2B connectors.

## MGT Lanes

MGT (Multi Gigabit Transceiver) lane consists of one transmit and one receive (TD/RD) differential pairs, two signals each or four signals total per one MGT lane. Following table lists lane number, MGT bank number, transceiver type, signal schematic name, and HPC FMC Pin:

| Lane | SFP+ | Signal Name | HPC FMC Pin |
|------|------|-------------|-------------|
|------|------|-------------|-------------|

|   |    |                                                                                                                              |                                                                                                                  |
|---|----|------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| 0 | J4 | <ul style="list-style-type: none"> <li>• SFPA_RD_P</li> <li>• SFPA_RD_N</li> <li>• SFPA_TD_P</li> <li>• SFPA_TD_N</li> </ul> | <ul style="list-style-type: none"> <li>• J2-C6</li> <li>• J2-C7</li> <li>• J2-C2</li> <li>• J2-C3</li> </ul>     |
| 1 | J5 | <ul style="list-style-type: none"> <li>• SFPB_RD_P</li> <li>• SFPB_RD_N</li> <li>• SFPB_TD_P</li> <li>• SFPB_TD_N</li> </ul> | <ul style="list-style-type: none"> <li>• J2-A2</li> <li>• J2-A3</li> <li>• J2-A22</li> <li>• J2-A23</li> </ul>   |
| 2 | J6 | <ul style="list-style-type: none"> <li>• SFPC_RD_P</li> <li>• SFPC_RD_N</li> <li>• SFPC_TD_P</li> <li>• SFPC_TD_N</li> </ul> | <ul style="list-style-type: none"> <li>• J2-A6</li> <li>• J2-A7</li> <li>• J2-A26</li> <li>• J2-A27</li> </ul>   |
| 3 | J7 | <ul style="list-style-type: none"> <li>• SFPD_RD_P</li> <li>• SFPD_RD_N</li> <li>• SFPD_TD_P</li> <li>• SFPD_TD_N</li> </ul> | <ul style="list-style-type: none"> <li>• J2-A10</li> <li>• J2-A11</li> <li>• J2-A30</li> <li>• J2-A31</li> </ul> |

**Table 3:** MGT lanes.

Below are listed MGT banks reference clock sources.

| Clock signal | Source | HPC FMC Pin           | Notes             |
|--------------|--------|-----------------------|-------------------|
| GBTCLK0_P    | U2-51  | J2-D4, GBTCLK0_M2C_P  | On-board Si5345A. |
| GBTCLK0_N    | U2-50  | J2-D5, GBTCLK0_M2C_N  | On-board Si5345A. |
| GBTCLK1_P    | U2-31  | J2-B20, GBTCLK1_M2C_P | On-board Si5345A. |
| GBTCLK1_N    | U2-30  | J2-B21, GBTCLK1_M2C_N | On-board Si5345A. |

**Table 4:** MGT reference clock sources.

## SFP+ Control Interface

Following table contains a brief description of the control and status signals of the SFP+ connectors:

| Signal Schematic Name | FPGA Direction | Description                   | Logic       |
|-----------------------|----------------|-------------------------------|-------------|
| SFPx_TX_DISABLE       | Output         | SFP Enabled / Disabled        | Low active  |
| SFPx_LOS              | Input          | Loss of receiver signal       | High active |
| SFPx_RS0              | Output         | Full RX bandwidth             | Low active  |
| SFPx_RS1              | Output         | Reduced RX bandwidth          | Low active  |
| SFPx_M-DEF0           | Input          | Module present / not present  | Low active  |
| SFPx_TX_FAULT         | Input          | Fault / Normal Operation      | High active |
| SFPx_SDA              | BiDir          | 2-wire Serial Interface Data  | -           |
| SFPx_SCL              | Output (BiDir) | 2-wire Serial Interface Clock | -           |

**Table 5:** Overview of SFP control Signals.





Up to 100kHz the modules operate without clock stretching. Therefore SCL can be implemented as driven by Master only.

## JTAG Interface

JTAG access to the MAX10 FPGA is provided through HPC FMC Connector and an additional pin header connector as well as testpoints.

| JTAG Signal | HPC FMC Pin | Pin Header | Testpoints |
|-------------|-------------|------------|------------|
| TCK         | J2-D29      | J3-4       | TP2        |
| TDI         | J2-D33      | J3-2       | TP1        |
| TDO         | J2-D30      | J3-3       | TP3        |
| TMS         | J2-D31      | J3-1       | TP4        |

**Table 6:** JTAG interface signals.

## I<sup>2</sup>C Interface

Despite the EEPROM U4 all other on-board I<sup>2</sup>C devices are connected to the MAX10 FPGA for level shift and I<sup>2</sup>C MUX. Addresses for devices are listed in the table below. The EEPROM is accessed via the FMC connector.

| I <sup>2</sup> C Device | I2C Address       | Notes                                                                                               |
|-------------------------|-------------------|-----------------------------------------------------------------------------------------------------|
| J4, SFP+                | 1100001 / 1100000 | Conventional SFP Memory / Enhanced Feature Set Memory, Device select via MAX10 FPGA implementation. |
| J5, SFP+                | 1100001 / 1100000 | Conventional SFP Memory / Enhanced Feature Set Memory, Device select via MAX10 FPGA implementation. |
| J6, SFP+                | 1100001 / 1100000 | Conventional SFP Memory / Enhanced Feature Set Memory, Device select via MAX10 FPGA implementation. |
| J7, SFP+                | 1100001 / 1100000 | Conventional SFP Memory / Enhanced Feature Set Memory, Device select via MAX10 FPGA implementation. |
| U2, Si5345A             | 1101001           | Level shifted via MAX10 FPGA, Device select via MAX10 FPGA implementation.                          |
| U4, EEPROM              | 10100xx           | Last digits determined by carrier board via HPC FMC (C34 GA0, C35 GA1).                             |

**Table 7:** I<sup>2</sup>C slave device addresses.

## HPC FMC Connector

The following table lists all on the FMC connector assigned net names.

|   | A         | B        | C         | D         | E   | F      | G      | H      | J   | K      |
|---|-----------|----------|-----------|-----------|-----|--------|--------|--------|-----|--------|
| 1 | GND       | NetJ2_B1 | GND       | PG_C2M    | GND | PG_M2C | GND    |        | GND |        |
| 2 | SFPB_RD_P | GND      | SFPA_TD_P | GND       |     | GND    | CLK1_P | GND    |     | GND    |
| 3 | SFPB_RD_N | GND      | SFPA_TD_N | GND       |     | GND    | CLK1_N | GND    |     | GND    |
| 4 | GND       |          | GND       | GBTCLK0_P | GND |        | GND    | CLK0_P | GND | CLK2_P |
| 5 | GND       |          | GND       | GBTCLK0_N | GND |        | GND    | CLK0_N | GND | CLK2_N |
| 6 | SFPC_RD_P | GND      | SFPA_RD_P | GND       |     | GND    | LA00_P | GND    |     | GND    |

|    |           |           |           |         |      |      |        |        |     |     |
|----|-----------|-----------|-----------|---------|------|------|--------|--------|-----|-----|
| 7  | SFPC_RD_N | GND       | SFPA_RD_N | GND     |      |      | LA00_N | LA02_P |     |     |
| 8  | GND       |           | GND       | LA01_P  | GND  |      | GND    | LA02_N | GND |     |
| 9  | GND       |           | GND       | LA01_N  |      | GND  | LA03_P | GND    |     | GND |
| 10 | SFPD_RD_P | GND       | LA06_P    | GND     |      |      | LA03_N | LA04_P |     |     |
| 11 | SFPD_RD_N | GND       | LA06_N    | LA05_P  | GND  |      | GND    | LA04_N | GND |     |
| 12 | GND       |           | GND       | LA05_N  |      | GND  | LA08_P | GND    |     | GND |
| 13 | GND       |           | GND       | GND     |      |      | LA08_N | LA07_P |     |     |
| 14 |           | GND       |           | LA09_P  | GND  |      | GND    | LA07_N | GND |     |
| 15 |           | GND       |           | LA09_N  |      | GND  |        | GND    |     | GND |
| 16 | GND       |           | GND       | GND     |      |      |        |        |     |     |
| 17 | GND       |           | GND       |         | GND  |      | GND    |        | GND |     |
| 18 |           | GND       |           |         |      | GND  |        | GND    |     | GND |
| 19 |           | GND       |           | GND     |      |      |        |        |     |     |
| 20 | GND       | GBTCLK1_P | GND       |         | GND  |      | GND    |        | GND |     |
| 21 | GND       | GBTCLK1_N | GND       |         |      | GND  |        | GND    |     | GND |
| 22 | SFPB_TD_P | GND       |           | GND     |      |      |        |        |     |     |
| 23 | SFPB_TD_N | GND       |           |         | GND  |      | GND    |        | GND |     |
| 24 | GND       |           | GND       |         |      | GND  |        | GND    |     | GND |
| 25 | GND       |           | GND       | GND     |      |      |        |        |     |     |
| 26 | SFPC_TD_P | GND       |           |         | GND  |      | GND    |        | GND |     |
| 27 | SFPC_TD_N | GND       |           |         |      | GND  |        | GND    |     | GND |
| 28 | GND       |           | GND       | GND     |      |      |        |        |     |     |
| 29 | GND       |           | GND       | TCK     | GND  |      | GND    |        | GND |     |
| 30 | SFPD_TD_P | GND       | FMC_SCL   | TDI     |      | GND  |        | GND    |     | GND |
| 31 | SFPD_TD_N | GND       | FMC_SDA   | TDO     |      |      |        |        |     |     |
| 32 | GND       |           | GND       | 3P3VAUX | GND  |      | GND    |        | GND |     |
| 33 | GND       |           | GND       | TMS     |      | GND  |        | GND    |     | GND |
| 34 |           | GND       | GA0       |         |      |      |        |        |     |     |
| 35 |           | GND       | 12V       | GA1     | GND  |      | GND    |        | GND |     |
| 36 | GND       |           | GND       | 3P3V    |      | GND  |        | GND    |     | GND |
| 37 | GND       |           | 12V       | GND     |      |      |        |        |     |     |
| 38 |           | GND       | GND       | 3P3V    | GND  |      | GND    |        | GND |     |
| 39 |           | GND       | 3P3V      | GND     | VADJ | GND  | VADJ   | GND    |     | GND |
| 40 | GND       |           | GND       | 3P3V    | GND  | VADJ | GND    | VADJ   | GND |     |

**Table 8:** HPC FMC Connector pin assignment.

## On-board Peripherals

### MAX10 FPGA

The MAX10 FPGA (10M08SAU169C8G) is used as SFP control, level shifter and I<sup>2</sup>C MUX. For a detailed description see [TEF0008 MAX10](#).

## Programmable Clock Generator

There is a Silicon Labs I<sup>2</sup>C programmable clock generator on-board (Si5345A, U2) to generate reference clocks for the module. Programming can be done using I<sup>2</sup>C via PIN header J1. The I<sup>2</sup>C bus is also routed to the MAX10 FPGA.

| Si5345A Pin | Signal Name / Description | Connected To   | Direction | Note                                       | Default   |
|-------------|---------------------------|----------------|-----------|--------------------------------------------|-----------|
| IN0         | Reference input clock.    | U1             | Input     | 25.000000 MHz oscillator, Si8208AI         |           |
| IN1         | -                         | Not connected. | Input     | Not used.                                  |           |
| IN2         | -                         | Not connected. | Input     | Not used.                                  |           |
| IN3         | CLK2                      | J2-K4/K5       | Input     | HPC FMC configured as C2M clock.           |           |
| A1          | -                         | GND            | Input     | I <sup>2</sup> C slave device address LSB. |           |
| XAXB        | -                         | Y1             | Input     | 54.0000 MHz XTAL CX3225SB                  |           |
| OUT0        | CLKPLL2F                  | U5-H6/G5       | Output    | FPGA bank 2.                               | 25MHz     |
| OUT1        | -                         | Not connected. | Output    | Not used.                                  | ---       |
| OUT2        | GBTCLK1                   | J2-B20/B21     | Output    | M2C via HPC FMC.                           | 125MHz    |
| OUT3        | -                         | Not connected. | Output    | Not used.                                  | ---       |
| OUT4        | -                         | Not connected. | Output    | Not used.                                  | ---       |
| OUT5        | -                         | Not connected. | Output    | Not used.                                  | ---       |
| OUT6        | -                         | Not connected. | Output    | Not used.                                  | ---       |
| OUT7        | GBTCLK0                   | J2-D4/D5       | Output    | M2C via HPC FMC.                           | 156.25MHz |
| OUT8        | CLK0                      | J2-H4/H5       | Output    | M2C via HPC FMC.                           | 156.25MHz |
| OUT9        | CLK1                      | J2-G2/G3       | Output    | M2C via HPC FMC.                           | 125MHz    |

Table 9: Programmable clock generator inputs and outputs.

## Oscillators

The module has following reference clock signals provided by on-board oscillators and external source from carrier board:

| Clock Source                       | Schematic Name | Frequency           | Clock Destination |
|------------------------------------|----------------|---------------------|-------------------|
| SiTime SiT8008AI oscillator, U1    | -              | 25.000000 MHz       | U2-63/64          |
| Carrier board via HPC FMC J2-K4/K5 | CLK2           | Defined by carrier. | U2-61/62          |

Table 10: Reference clock signals.

## EEPROM

A Microchip 24LC128-I/LC serial EEPROM (U4) is provided for IPMI data. It is accessible via the LPC FMC connector (SCL C30, SDA C31).

## On-board LED

| LED | Color | Connected to    | Description and Notes                                                                              |
|-----|-------|-----------------|----------------------------------------------------------------------------------------------------|
| D1  | Green | U5-C2 (bank 1A) | Depending on FPGA design. With the shipped FPGA design it is on, if at least one SFP is connected. |

Table 11: On-board LED.

# Power and Power-On Sequence

## Power Consumption

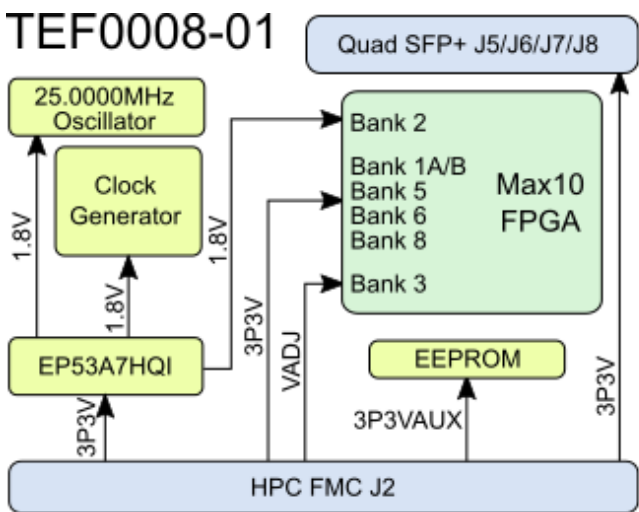
The maximum power consumption of a module depends on the design running on the FPGA.

|                |      |
|----------------|------|
|                |      |
| 3P3V           | TBD* |
| VADJ (at 1.8V) | TBD* |
| 3P3VAUX        | TBD* |

**Table 12:** Typical power consumption.

\* TBD - To Be Determined with reference design setup.

## Power Distribution Dependencies



**Figure 3:** Module power distribution diagram.

## Power Rails

| Power Rail Name | HPC FMC Connector (J2) | Direction | Notes                                         |
|-----------------|------------------------|-----------|-----------------------------------------------|
| 3P3V            | D36, D38, D40, C39     | Input     | Supply voltage from carrier board.            |
| 1.8V            | -                      | Output    | Module on-board 1.8V voltage supply (Max 1A). |
| 3P3VAUX         | D32                    | Input     | Supply voltage from carrier board.            |
| VADJ            | H40, G39, F40, E39     | Input     | Supply voltage from carrier board.            |
| 12V             | C35, C37               | Input     | Not used supply voltage from carrier board.   |



**Table 13:** Module power rails.

## Bank Voltages

| Bank | Schematic Name | Voltage          | Voltage Range |
|------|----------------|------------------|---------------|
| 1A   | 3P3V           | 3.3V             | -             |
| 1B   | 3P3V           | 3.3V             | -             |
| 2    | 1.8V           | 1.8V             | -             |
| 3    | VADJ           | Carrier supplied | 1.2V - 3.3V   |
| 5    | 3P3V           | 3.3V             | -             |
| 6    | 3P3V           | 3.3V             | -             |
| 8    | 3P3V           | 3.3V             | -             |

**Table 14:** Module PL I/O bank voltages.

## Variants Currently In Production

| Module Variant | FPGA           | Operating Temperature | Temperature Range |
|----------------|----------------|-----------------------|-------------------|
| TE0008-02      | 10M08SAU169C8G | 0°C to +85°C          | Extended          |

**Table 15:** Module variants.

## Technical Specifications

### Absolute Maximum Ratings

| Parameter           | Min | Max | Units | Reference Document |
|---------------------|-----|-----|-------|--------------------|
| Storage temperature | -40 | 85  | °C    | -                  |

**Table 16:** Module absolute maximum ratings.

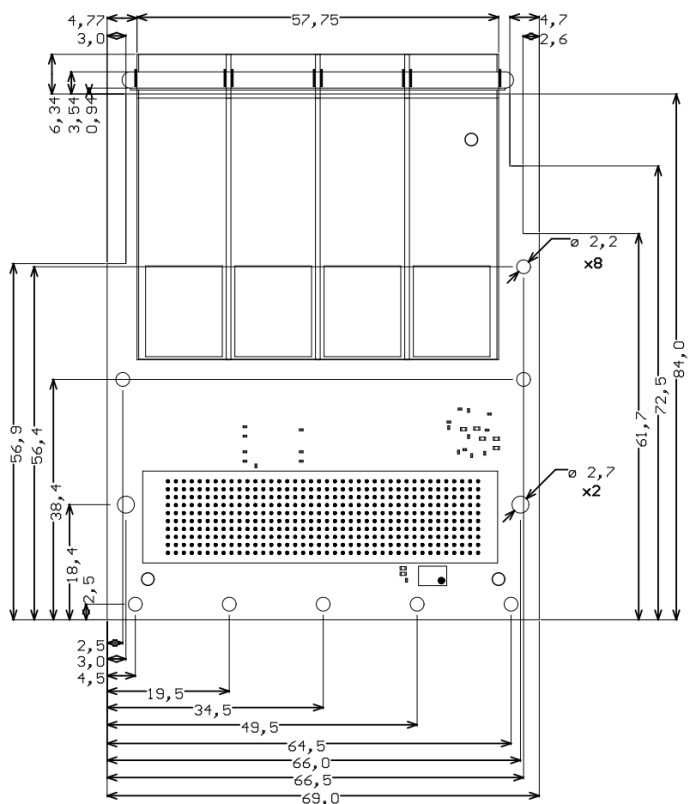
### Operating Temperature Ranges

Extended grade: 0°C to +85°C.

### Physical Dimensions

- Module size: 69 mm × 84 mm, SFP+ conector excluded (+ 5.5 mm). See Vita 57.1 standard.
- PCB thickness: 1.6 mm.
- Highest part on PCB top is 9.5 mm (SFP+ cage, excluded front plate), bottom 1.4 mm (MAX10 FPGA). Please download the step model for exact numbers.

All dimensions are given in millimeters.



**Figure 4:** Module physical dimensions drawing



Mounting holes near the front pannel are not implemented due to physical restrictions caused by the SFP cage. The dimensions exceed in some area the by Vita 57.1 standard defined dimensions. In the middle region of the card the cage is higher than the specified max high for this area. Check carefully if the carrier card uses this space for other components conflicting mechanical. The bottom side is at the high limit.

## Revision History

### Hardware Revision History

| Date       | Revision | Notes                    | PCN | Documentation Link |
|------------|----------|--------------------------|-----|--------------------|
| 2018-06-06 | 02       | First production release |     |                    |
| -          | 01       | Prototypes               |     |                    |

**Table 17:** Module hardware revision history.

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

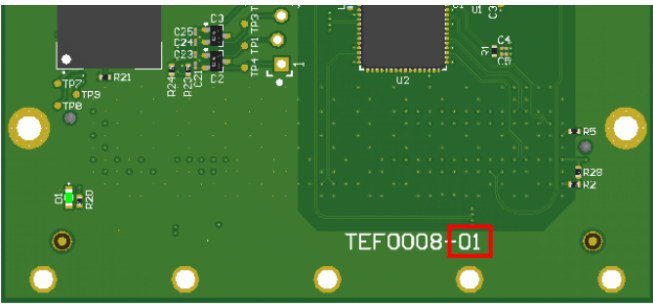


Figure 5: Module hardware revision number.

Document Change History

| Date | Revision | Contributors | Description |
|------|----------|--------------|-------------|
|------|----------|--------------|-------------|

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                   |
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| <p><b>Error rendering macro 'page-info'</b></p> <p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> | <p><b>Error rendering macro 'page-info'</b></p> <p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> | <p><b>Error rendering macro 'page-info'</b></p> <p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> |                                                                                                                                                   |
| 2018-08-24                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | v.38                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Martin Rohrmüller                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | <ul style="list-style-type: none"> <li>• Updated Table 15 and 17 to Rev02.</li> <li>• Added FMC connector pin assignment (Table 8).</li> </ul>    |
| 2018-06-15                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | v.32                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Martin Rohrmüller                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | <ul style="list-style-type: none"> <li>• Initial document.</li> </ul>                                                                             |

|     |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |       |
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| --- | all | <div><p><b>Error rendering macro 'page-info'</b></p><p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p></div> | • --- |
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**Table 18:** Document change history.

Disclaimer

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Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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### RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

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Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Ambiguous method overloading for method `jdk.proxy241.$Proxy3496#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`

02 Sept 2017