TE0841 IBERT

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Error rendering macro 'toc'

java.lang.RuntimeException: com.ctc.wstx.exc.WstxParsingException: String '--' not allowed in comment (missing '>'?) at [row,col {unknown-source}]: [39,-1115]

Overview

Example show, how to reconfigure SI5338 with MCS and monitor CLK. Additional MicroBlaze is add for Hello TE0741 example.

Key Features

- MGT
- SI5338 initialisation with MCS

Revision History

Date	Vivado	Project Built	Authors	Description
2018-06-22	2017.4	TE0841-IBERT_noprebuilt-vivado_2017.4-build_11_20180622140813.zip TE0841-IBERT-vivado_2017.4-build_11_20180622140615.zip	John Hartfiel	• REV02 Board parts • new SI5338 configuration (default REV02) • change xilisf_v5_9 for N25Q512A11G1240E support • Some changes on block design
2018-06-05	2017.4	TE0841-IBERT_noprebuilt-vivado_2017.4-build_10_20180605143852.zip TE0841-IBERT-vivado_2017.4-build_10_20180605143837.zip	John Hartfiel	• initial release

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
PCB REV01 only: IBERT no CLK	PCB REV01 SI5338 is not preprogrammed and SI programming over MCS is disabled by default design and I2C is not connected	Load test_board bitfile for REV01 and load IBERT design again without power off HW	---

Requirements

Software

Software	Version	Note
Vivado	2017.4	needed
SDK	2017.4	needed

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0841-01-035-1C	01_35_1c	REV01	2x 512MB DDR4	32MB	---	
TE0841-01-035-1I	01_35_1i	REV01	2x 512MB DDR4	32MB	---	
TE0841-01-035-2I	01_35_2i	REV01	2x 512MB DDR4	32MB	---	
TE0841-01-040-1C	01_40_1c	REV01	2x 512MB DDR4	32MB	---	Serial number 512479 up tp 512474 has same 64MB Flash like REV02
TE0841-01-040-1I	01_40_1i	REV01	2x 512MB DDR4	32MB	---	
TE0841-01-040-2I	01_40_2i	REV01	2x 512MB DDR4	32MB	---	
TE0841-02-035-1C	02_35_1c	REV02	2x 1GB DDR4	64MB	---	
TE0841-02-035-1I	02_35_1i	REV02	2x 1GB DDR4	64MB	---	
TE0841-02-035-2I	02_35_2i	REV02	2x 1GB DDR4	64MB	---	
TE0841-02-040-1C	02_40_1c	REV02	2x 1GB DDR4	64MB	---	
TE0841-02-040-1I	02_40_1i	REV02	2x 1GB DDR4	64MB	---	
TE0841-02-040-1IL	02_40_1i	REV02	2x 1GB DDR4	64MB	low profile B2B connector	

Design supports following carriers:

Carrier Model	Notes
TEBA0841	used as reference carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI
Heat sink	It's recommended to use heat sink for this design

Content

For general structure and of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib <design name>/firmware	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI

Additional Sources

Type	Location	Notes
SI5338 Project	\misc\SI5338	

Prebuilt

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0841 "IBERT" Reference Design

Design Flow

⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

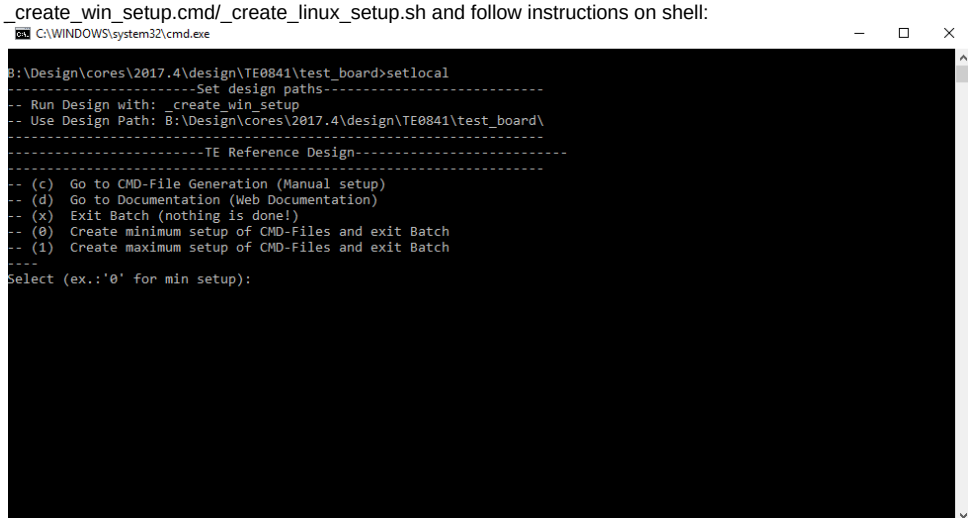
See also:AMD Development Tools#XilinxSoftware-BasicUserGuides

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
    a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
    Note: Select correct one, see TE Board Part Files
5. Create HDF and export to prebuilt folder
    a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
    Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate MCS Firmware (optional):
    a. Create SDK Project with TE Scripts on Vivado TCL: TE::sw_run_sdk
    b. Create "SCU" application
    Note: Select MCS Microblaze and SCU Application
    c. Select Release Built
    d. Regenerate App
7. (optional) Copy "\\workspace\sdk\scu\Release\scu.elf" into "\firmware\microblaze_mcs_0\"
8. Regenerate Vivado Project or Update Bitfile only and "scu.elf"
9. Copy MCS file with Bitfile into prebuilt folder
    a. Create SDK Project with TE Scripts on Vivado TCL: TE::sw_run_hsi

Launch

Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

QSPI

1. Connect JTAG and power on PCB
2. (if not done) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" or open with "vivado_open_project_guimode.cmd", if generated.
3. Type on Vivado Console: TE::pr_program_flash_mcsfile -swapp
   Note: Alternative use SDK or setup Flash on Vivado manually
4. Reboot (if not done automatically)

SD

Not used on this Example.

JTAG

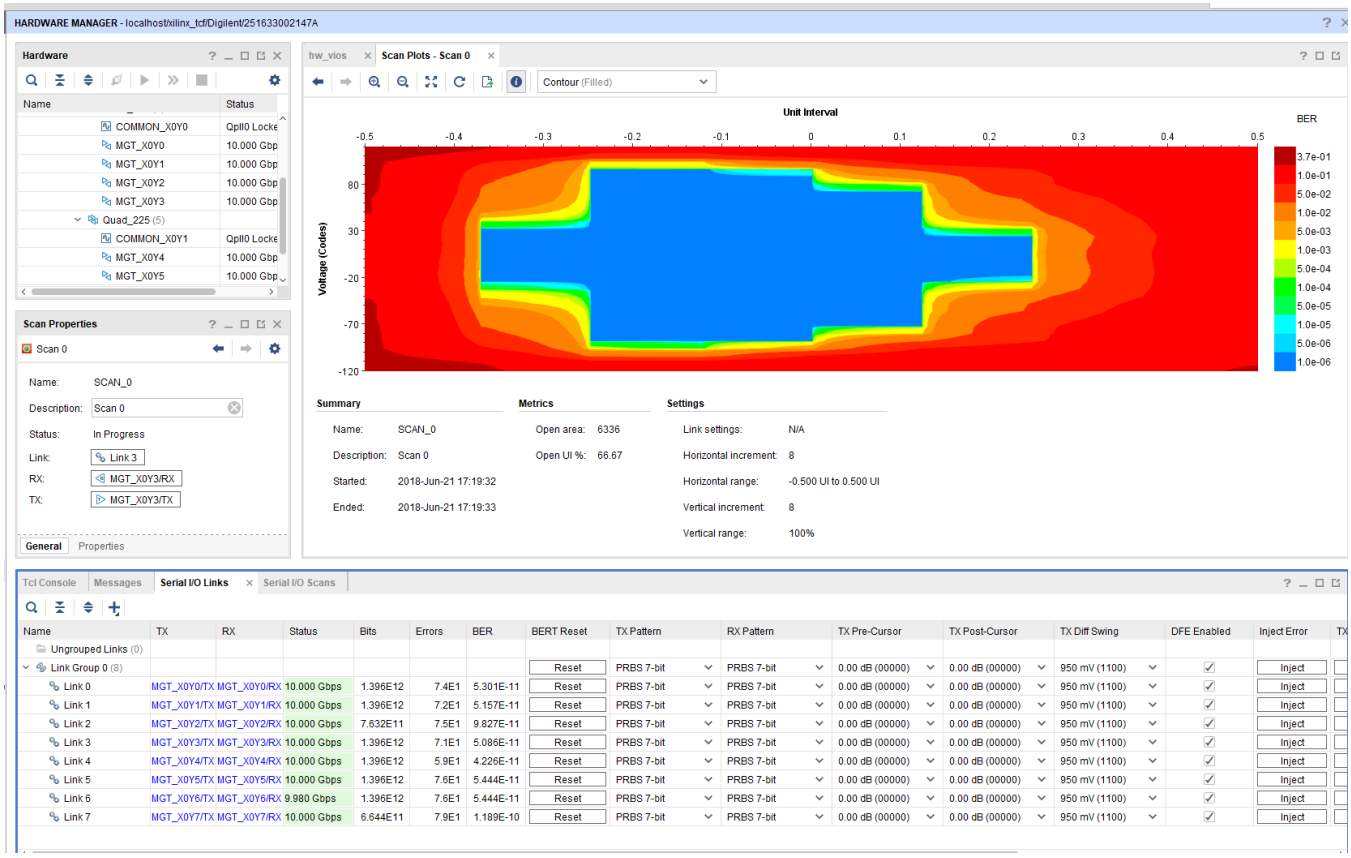
1. Connect JTAG and power on PCB
2. Open Vivado HW Manager
3. Program FPGA with Bitfile from "prebuilt\hardware\<short dir>"

Usage

1. Prepare HW like described on section TE0841 IBERT#Programming
2. Connect UART USB (most cases same as JTAG)
3. Power on PCB
   Note: FPGA Loads Bitfile from Flash,MCS Firmware configure SI5338 and starts IBERT.
   Do not reboot, if Bitfile programming over JTAG is used as programming method.
   a. On TE0841 SI5338 has default configuration and reprogramming of SI5338 is optional
4. LED:
   a. D1 (green) OFF MCS SI configuration finished (System Reset is off)

Vivado HW Manager:

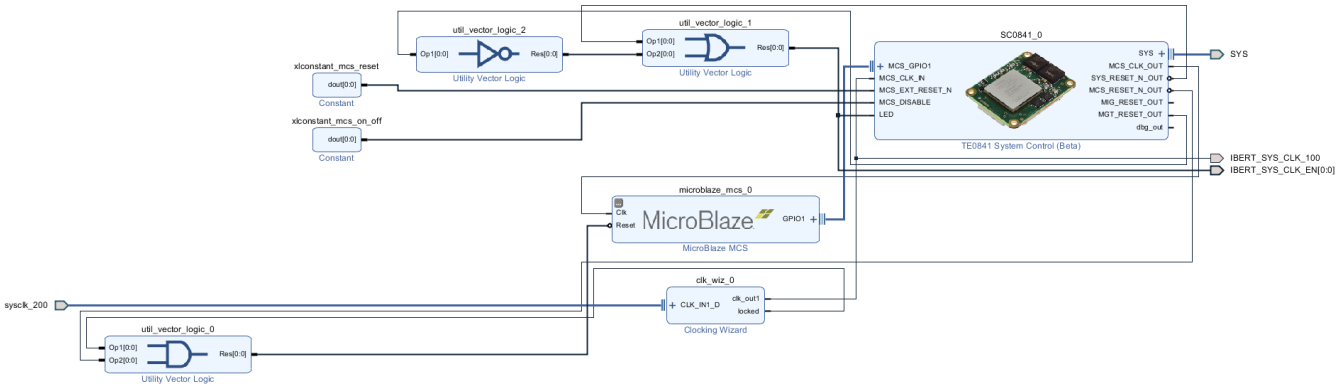
1. Open Vivado HW-Manager
2. "Refresh device" is needed after Bitfile programming, because MCS reconfigure SI5338 and enables IBERT a little bit later.
   a. loopback depends on TEB0841 Revision an connection



IBERT	Component Name	Net Name	TEB0841
X0Y0	224-0	MGT4	loop back RX/TX
X0Y1	224-1	MGT5	loop back RX/TX
X0Y2	224-2	MGT6	loopback over SD Pin header possible with lower Linerate otherwise use internal loopback
X0Y3	224-3	MGT7	loop back RX/TX. Note: N.C. on TEB0841-01, use internal loopback
X0Y4	225-0	MGT0	loop back RX/TX
X0Y5	225-1	MGT1	loop back RX/TX
X0Y6	225-2	MGT2	loop back RX/TX
X0Y7	225-3	MGT3	loopback over sfp possible

System Design - Vivado

Block Design



HDL

- IBERT_top.v
- ibert xci IPs

Constrains

Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 69 [current_design]
set_property CFGBVS GND [current_design]
set_property CONFIG_VOLTAGE 1.8 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

Design specific constrain

ibert_ultrascale_gth_0.xdc

```
# file: ibert_ultrascale_gth_0.xdc
##############################################################################################
##   ____  ____
##  /   /\/   /
## /___/  \  /    Vendor: Xilinx
## \   \   \/     Version : 2012.3
##  \   \         Application : IBERT Ultrascale
##  /   /         Filename : example_ibert_ultrascale_gth_0.xdc
## /___/   /\
## \   \  /  \
##  \___\/\___\
##
##
##
## Generated by Xilinx IBERT 7Series
##************************************************************************
##
## Icon Constraints
##
create_clock -name D_CLK -period 10.0 [get_ports gth_sysclkp_i]
set_clock_groups -group [get_clocks D_CLK -include_generated_clocks] -asynchronous
set_property C_CLK_INPUT_FREQ_HZ 100000000 [get_debug_cores dbg_hub]
set_property C_ENABLE_CLK_DIVIDER true [get_debug_cores dbg_hub]

##gth_refclk lock constraints
##
set_property PACKAGE_PIN AD6 [get_ports gth_refclk0p_i[0]]
set_property PACKAGE_PIN AD5 [get_ports gth_refclk0n_i[0]]
set_property PACKAGE_PIN AB6 [get_ports gth_refclk1p_i[0]]
set_property PACKAGE_PIN AB5 [get_ports gth_refclk1n_i[0]]
##
## Refclk constraints
##
create_clock -name gth_refclk0_0 -period 8.0 [get_ports gth_refclk0p_i[0]]
create_clock -name gth_refclk1_0 -period 8.0 [get_ports gth_refclk1p_i[0]]
set_clock_groups -group [get_clocks gth_refclk0_0 -include_generated_clocks] -asynchronous
set_clock_groups -group [get_clocks gth_refclk1_0 -include_generated_clocks] -asynchronous
##
## System clock pin locs and timing constraints
##
#set_property PACKAGE_PIN R25 [get_ports gth_sysclkp_i]
#set_property IOSTANDARD LVDS [get_ports gth_sysclkp_i]
```

Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

Application

SCU

MCS Firmware to configure SI5338 and Reset System.

Template location: \sw_lib\sw_apps\scu

Additional Software

SI5338

Download ClockBuilder Desktop for SI5338

1. Install and start ClockBuilder
2. Select SI5338
3. Options Open register map file
   Note: File location <design name>/misc/Si5338/RegisterMap.txt
4. Modify settings
5. Options save C code header files
6. Replace Header files from SCU template with generated file

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] Unknown macro: 'metadata'	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• some notes • Issue for PCB REV01 only: MCS is disabled on the prebuilt design files
22 Jun 2018	v.5	John Hartfiel	• Design update • new assembly variants (PCB REV02)
05 Jun 2018	v.4	John Hartfiel	• Release 2017.4

2018-04-16	v.1	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• Initial release

	All	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	

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