TEC0850 TRM

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Overview

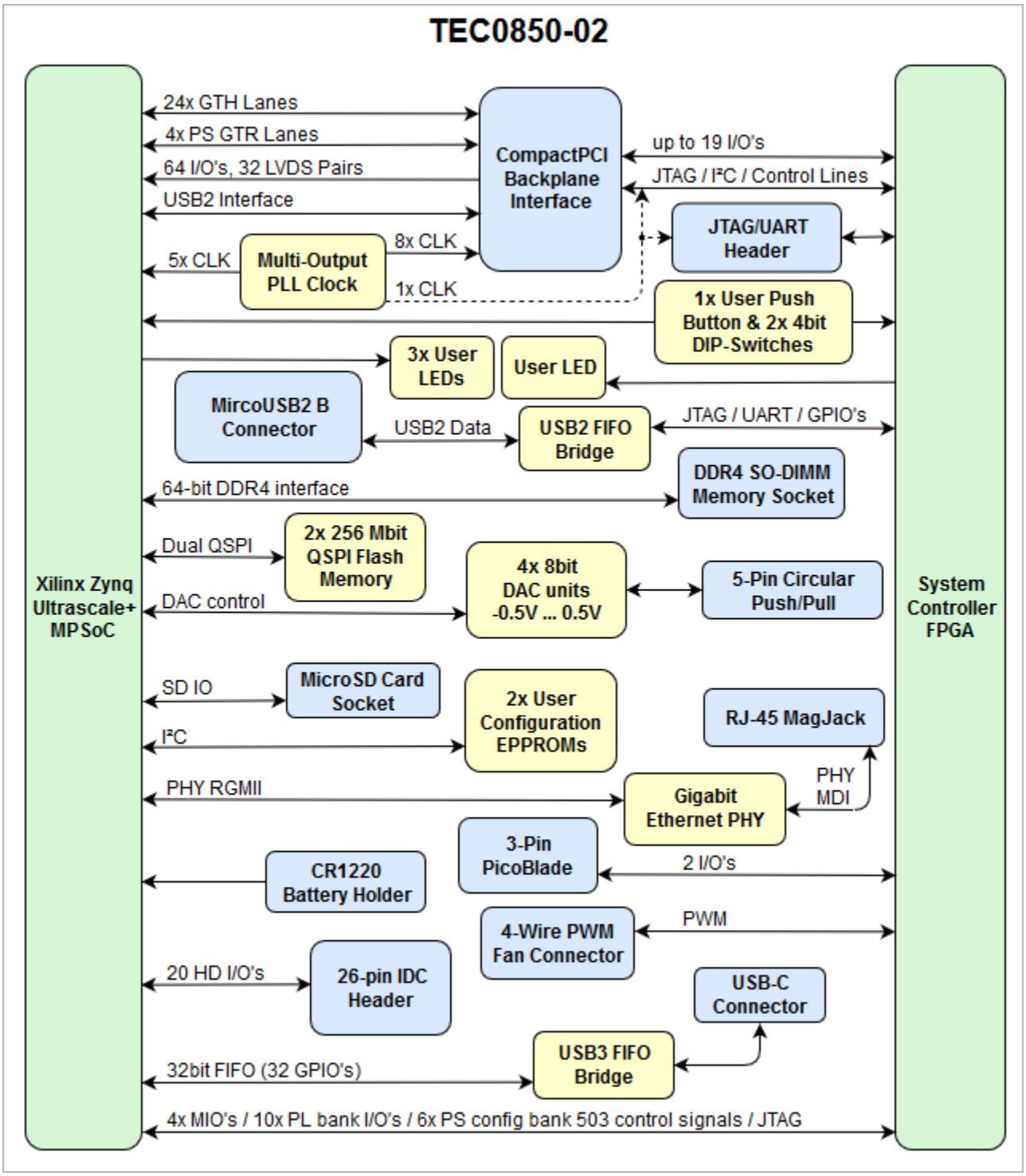
The Trenz Electronic TEC0850 board is a CompactPCI Serial card (3U form factor) integrating a Xilinx Zynq UltraScale+ MPSoC, one DDR4 SDRAM SODIMM socket with 64bit wide data bus, max. dual 512 MByte Flash memory for configuration and operation, 24 Gigabit transceivers on PL side and 4 on PS side, powerful switch-mode power supplies for all onboard voltages, USB2 and USB3 FIFO bridges and a large number of configurable I/Os available on the CompactPCI Serial backplane connectors.

Refer to http://trenz.org/tec0850-info for the current online version of this manual and other available documentation.

Key Features

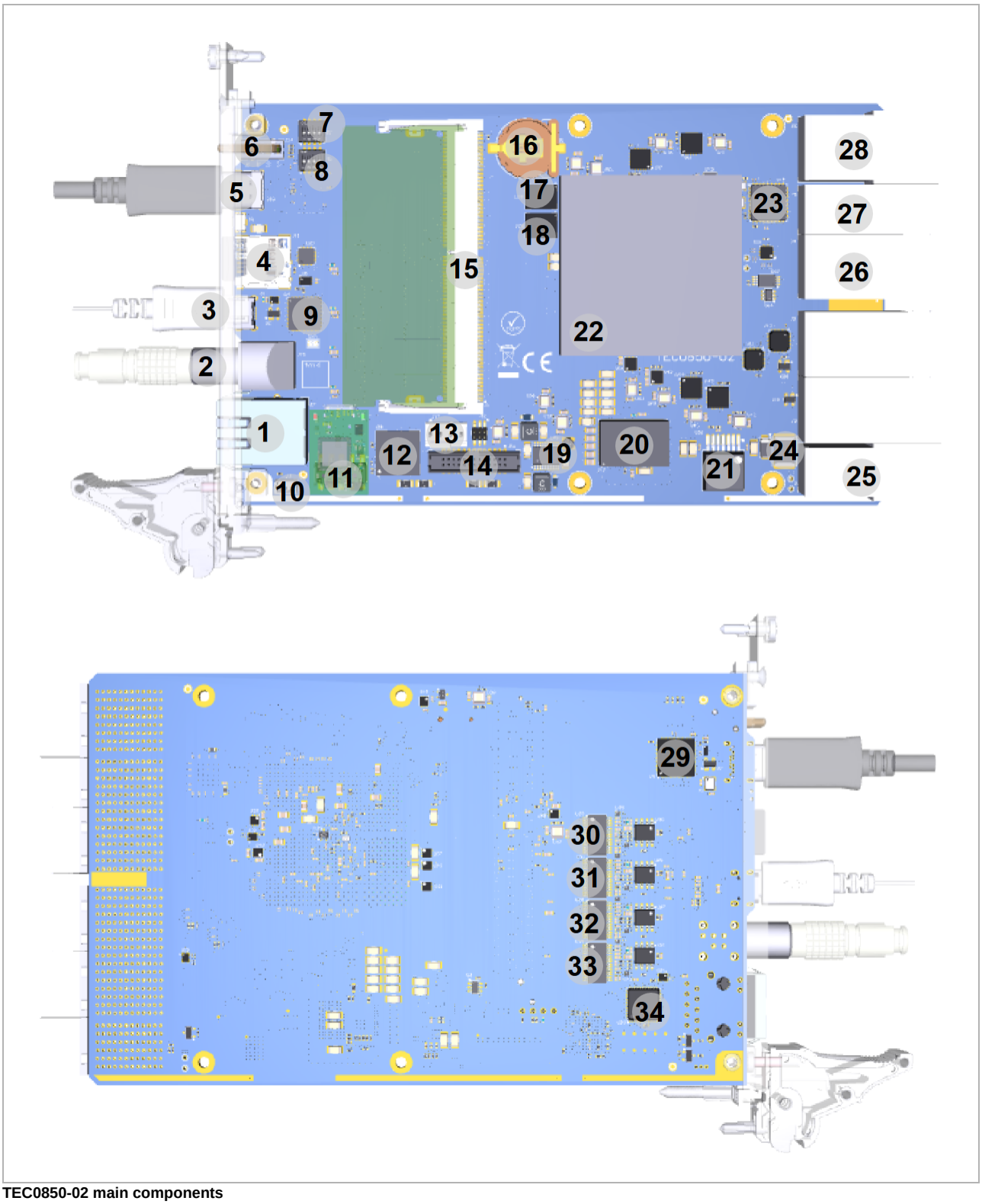
- Zynq UltraScale+ MPSoC ZU15
- Front side interface connectors
  - RJ-45 GbE Ethernet interface
  - Circular push/pull connector with 4x on-board 8bit DAC output
  - MicroSD Card connector
  - USB 2.0 and USB 3.0 to FIFO bridge connector
  - 4x status LEDs
- 4 CompactPCI Serial connectors for backplane connection (3U form factor)
  - 24 GTH lanes
  - 4 PS GTR lanes
  - USB 2.0 interface
  - 64 Zynq PL HP I/O's
  - 8x PLL clock input
  - JTAG, I²C and 7 user I/O's to MAX10 FPGA
- 64bit DDR4 SODIMM (PS connected), 8 GByte maximum
- Dual parallel QSPI Flash (bootable), 512 MByte maximum
- 26-pin header with 20 Zynq PL HD I/O's
- 3-pin header with 2 MAX10 FPGA I/O's
- System Controller (Altera MAX10 FPGA SoC)
  - Power Sequencing
  - System management and control for MPSoC and onboard peripherals
- Si5345 programmable 10 output PLL clock generator
- Si53340 Quad clock buffer
- 2x 4bit DIP switches
- 1x user push button
- Zynq MPSoC cooling FAN connector
- On-board high-efficiency DC-DC converters

Block Diagram



TEC0850-02 block diagram

Main Components



TEC0850-02 main components

1. GbE RJ-45 MagJack, J7
2. 5-pin circular push/pull receptacle connector for DAC output, J15
3. Micro USB 2.0 B receptacle connector, J9
4. MicroSD Card socket, J11
5. USB 3.0 Type C connector, J10
6. LED light pipes J14 integrating LEDs D1 ... D4
7. 4bit DIP-switch, S2
8. 4bit DIP-switch, S1
9. FTDI FT2232 USB 2.0 to UART/JTAG bridge, U4
10. 3-pin PicoBlade header, J8
11. MAX10 FPGA JTAG/UART 10-pin header, J13
12. Altera MAX10 System Controller FPGA, U18
13. 4-Wire PWM fan connector, J17
14. 26-pin IDC header for FPGA PL I/O's, J16
15. DDR4 SO-DIMM 260-pin socket, U3
16. Battery Holder CR1220, B1
17. 256 Mbit (32 MByte) Micron Serial NOR Flash Memory N25Q256A, U24
18. 256 Mbit (32 MByte) Micron Serial NOR Flash Memory N25Q256A, U25
19. DC-DC Converter LT8471IFE @+5VA/-5VA, U74
20. DC-DC Converter EM2130L02QI @VCCINT_0V85, U17
21. DC-DC Converter 171050601 @5V, U50
22. Xilinx Zynq Ultrascale+ MPSoC, U1
23. Si5345A 10-output I²C programmable PLL clock, U14
24. Main power fuse @2.5A/16V, F1
25. cPCI connector, J1
26. cPCI connector, J4
27. cPCI connector, J5
28. cPCI connector, J6
29. FTDI FT601Q USB 3.0 to FIFO bridge, U9
30. TI THS5641 8bit DAC ,U28
31. TI THS5641 8bit DAC ,U31
32. TI THS5641 8bit DAC ,U29
33. TI THS5641 8bit DAC ,U33
34. Marvell Alaska 88E1512 GbE PHY ,U20

Initial Delivery State

Storage device name	Content	Notes
User configuration EEPROMs (1x Microchip 24AA128T-I/ST, 1x Microchip 24AA025E48T-I/OT)	Empty	Not programmed
USB 2.0 to UART/JTAG bridge configuration EEPROM (ST M93C66)	Empty	Not programmed
Si5345A programmable PLL NVM OTP	Empty	Not programmed
2x QSPI Flash memory	Empty	Not programmed

Initial delivery state of programmable devices on the module

Control Signals

To get started with TEC0850 board, some initial signals should be set described in the following table:

Control signal	Switch / Button	Signal Schematic Names	Connected to	Functionality	Notes
SC JTAGEN	S1-1	JTAGEN	SC FPGA U18, bank 1B, pin E5	OFF: MAX 10 JTAG enabled, ON: Zynq MPSoC JTAG enabled	-

EEPROM WP	S1-2	WP	EEPROM U63, pin 7	Write protect, active on OFF position	-
FPGA PUDC	S1-3	PUDC_B	Zynq MPSOC PS Config Bank 503, pin AD15	ON: internal pull-up resistors enabled, OFF: floating	-
SC Switch	S1-4	SW4	SC FPGA U18, bank 8, pin A5	low active logic	Reserved for future use
4bit boot mode setting code	S2-1	MODE3	Zynq MPSOC PS Config Bank 503, pin R23	Set 4-bit code for boot mode selection, most common modes are as follows: Set DIP-switches as bit pattern "S1-4 | S1-3 | S1-2 | S1-1 : Mode": ON | ON | ON | ON : JTAG Boot ON | ON | ON | OFF : Quad-SPI ON | ON | OFF | OFF : SD Card	See Zynq UltraScale+ Device Technical Reference Manual page 236 for full boot modes description
	S2-2	MODE2	Zynq MPSOC PS Config Bank 503, pin T23		
	S2-3	MODE1	Zynq MPSOC PS Config Bank 503, pin R22		
	S2-4	MODE0	Zynq MPSOC PS Config Bank 503, pin T22		
Push button	S3	USR_BTN	SC FPGA U18, bank 5, pin J10	low active logic	See the documentation of the firmware of SC FPGA U18 for current functionality of the onboard Push Button S3
SC FPGA U18 Reset	header J13, pin 6	M10_RST	SC FPGA U18, bank 8, pin A7	low active reset line	-

TEC0850 Control Signals

Signals, Interfaces, and Pins

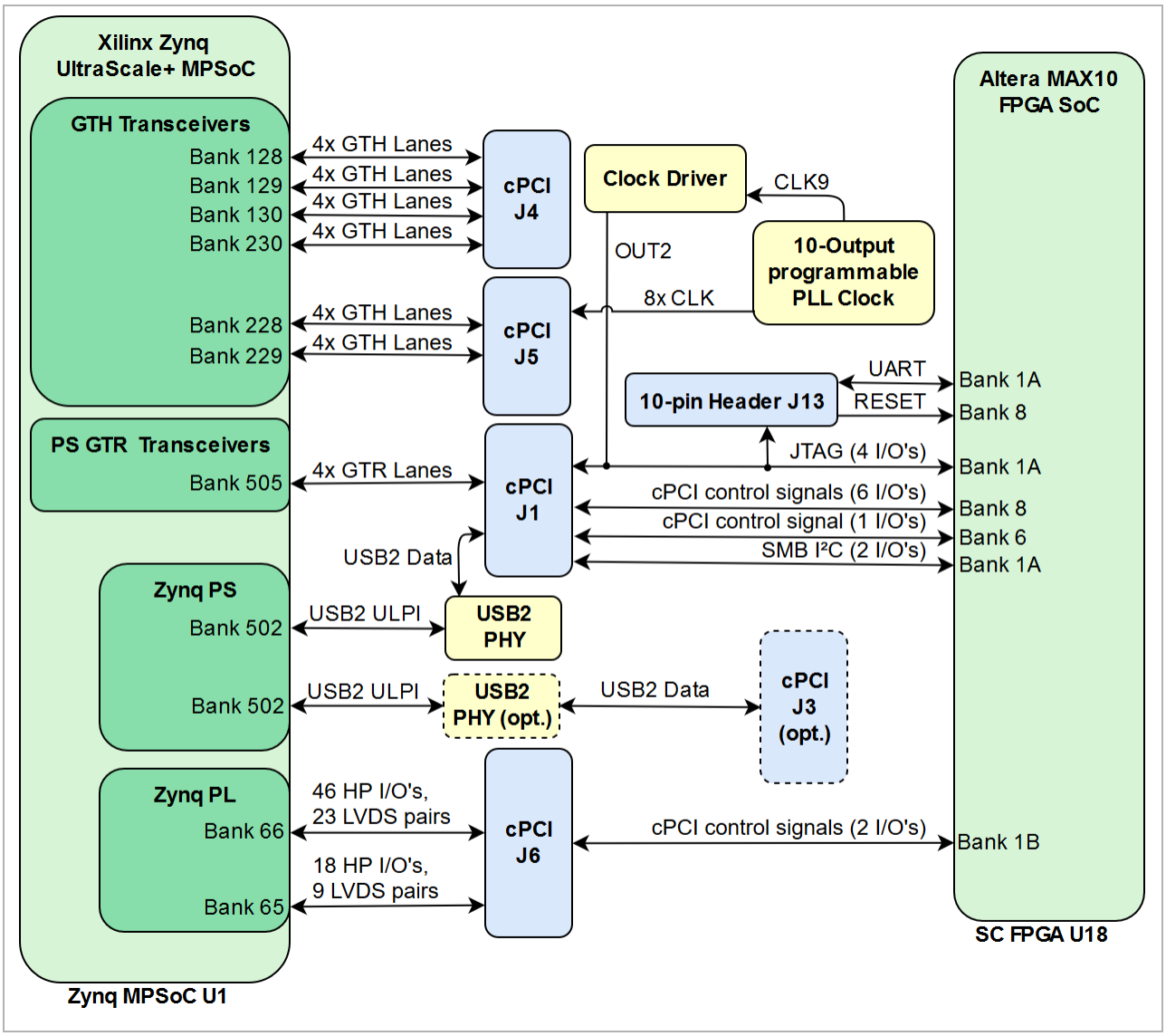
CompactPCI Serial Backplane Connectors

The TEC0850 board is equipped with 3 CompactPCI Serial high-speed backplane connectors which provide serial high-speed interconnects with transmission rates up to 12 Gb/s to the Zynq MPSoCs MGT lanes. On the cPCI connectors are also available single-ended Zynq MPSoC PL HP I/O's, high-speed USB 2.0 interface and single-ended I/O's of the System Controller FPGA.

The connectors support single-ended and differential signaling to the Zynq MPSoC PL HP banks 65 and 66 as those FPGA I/O's are routed as LVDS-pairs to the backplane connector.

The TEC0850 board is designed to be connected to the System Slot of the backplane, whereby 4 of the 6 connectors of the System Slot configuration are fitted to the TEC0850 board.

Following diagram gives an overview of the CompactPCI Serial backplane connectors and their connections to the Zynq Ultrascale+ MPSoC and the System Controller FPGA U18:



TEC0850-02 CompactPCI I/O and high-speed interfaces

Following tables contains information about the interfaces, I/O's, clock and VCCIO sources available on the cPCI connectors:

1. CompactPCI Serial Connector J1
2. CompactPCI Serial Connector J3
3. CompactPCI Serial Connector J4
4. CompactPCI Serial Connector J5
5. CompactPCI Serial Connector J6

CompactPCI Serial Connector J1

Interfaces	I/O Signal Count	LVDS-pairs count	Connected to	VCCO bank Voltage	Notes
I/O	1	-	SC FPGA U18 Bank 6	+3V_D	control signals in cPCI pin assignment
	6	-	SC FPGA U18 Bank 8	+3V_D	control signals in cPCI pin assignment
I²C	2	-	SC FPGA U18 Bank 1A	+3V_D	SC FPGA U18 I²C interface
JTAG	4	-	SC FPGA U18 Bank 1A	+3V_D	SC FPGA U18 JTAG interface
MGT	-	8 (4 x RX/TX)	Bank 502 PS GTR	-	4x PS GTR lanes
USB2	-	1 (RX/TX)	USB2 PHY U11	-	USB2 OTG A-Device (host)
Clock Input	-	1	Clock Driver U73	-	1x Reference clock input from PLL clock U14

cPCI J1 interfaces

MGT Lane	Bank	Type	Signal Schematic Name	cPCI Connector Pin	FPGA Pin
0	505	GTR	• PE1_RX0_P • PE1_RX0_N • PE1_TX0_P • PE1_TX0_N	J1-D5 J1-E5 J1-A5 J1-B5	PS_MGTRRXP0_505, AB29 PS_MGTRRXN0_505, AB30 PS_MGTRTXP0_505, AB33 PS_MGTRTXN0_505, AB34
1	505	GTR	• PE1_RX1_P • PE1_RX1_N • PE1_TX1_P • PE1_TX1_N	J1-J5 J1-K5 J1-G5 J1-H5	PS_MGTRRXP1_505, Y29 PS_MGTRRXN1_505, Y30 PS_MGTRTXP1_505, AA31 PS_MGTRTXN1_505, AA32
2	505	GTR	• PE1_RX2_P • PE1_RX2_N • PE1_TX2_P • PE1_TX2_N	J1-E6 J1-F6 J1-B6 J1-C6	PS_MGTRRXP2_505, W31 PS_MGTRRXN2_505, W32 PS_MGTRTXP2_505, Y33 PS_MGTRTXN2_505, Y34
3	505	GTR	• PE1_RX3_P • PE1_RX3_N • PE1_TX3_P • PE1_TX3_N	J1-K6 J1-L6 J1-H6 J1-I6	PS_MGTRRXP3_505, V29 PS_MGTRRXN3_505, V30 PS_MGTRTXP3_505, V33 PS_MGTRTXN3_505, V34

cPCI J1 MGT lanes

Clock Signal Schematic Name	cPCI Connector Pin	Header J13 Pin	SC FPGA U18 Pin	Notes
• SATA_SL • SATA_SCL	J1-K3 J1-J3	J13-5 J13-1	Bank 1B, Pin G1 Bank 1B, Pin G2	Supplied by 10-output PLL clock U14, optional if decoupling capacitors and resistors are fitted (see schematic), also shared with SC FPGA and header J13.

cPCI J1 clock signals

CompactPCI Serial Connector J3

CompactPCI Serial connector J3 is **not fitted** on the TEC0850 board by default, but is necessary if the second optional USB2 PHY U13 if fitted and its USB2 differential serial data interface is connected to the cPCI connector J2.

Interfaces	I/O Signal Count	LVDS-pairs count	Connected to	VCCO bank Voltage	Notes
USB2	-	1 (RX/TX)	USB2 PHY U13	-	USB2 OTG A-Device (host)

cPCI J3 interfaces

CompactPCI Serial Connector J4

MGT Lane	Bank	Type	Signal Schematic Name	cPCI Connector Pin	FPGA Pin
0	128	GTH	• PE3_RX0_P • PE3_RX0_N • PE3_TX0_P • PE3_TX0_N	J4-D1 J4-E1 J4-A1 J4-B1	MGTHRXP0_128, T33 MGTHRXN0_128, T34 MGTHTXP0_128, T29 MGTHTXN0_128, T30
1	128	GTH	• PE3_RX1_P • PE3_RX1_N • PE3_TX1_P • PE3_TX1_N	J4-J1 J4-K1 J4-G1 J4-H1	MGTHRXP1_128, P33 MGTHRXN1_128, P34 MGTHTXP1_128, R31 MGTHTXN1_128, R32
2	128	GTH	• PE3_RX2_P • PE3_RX2_N • PE3_TX2_P • PE3_TX2_N	J4-E2 J4-F2 J4-B2 J4-C2	MGTHRXP2_128, N31 MGTHRXN2_128, N32 MGTHTXP2_128, P29 MGTHTXN2_128, P30
3	128	GTH	• PE3_RX3_P • PE3_RX3_N • PE3_TX3_P • PE3_TX3_N	J4-K2 J4-L2 J4-H2 J4-I2	MGTHRXP3_128, M33 MGTHRXN3_128, M34 MGTHTXP3_128, M29 MGTHTXN3_128, M30
0	129	GTH	• PE4_RX0_P • PE4_RX0_N • PE4_TX0_P • PE4_TX0_N	J4-D3 J4-E3 J4-A3 J4-B3	MGTHRXP0_129, L31 MGTHRXN0_129, L32 MGTHTXP0_129, K29 MGTHTXN0_129, K30
1	129	GTH	• PE4_RX1_P • PE4_RX1_N • PE4_TX1_P • PE4_TX1_N	J4-J3 J4-K3 J4-G3 J4-H3	MGTHRXP1_129, K33 MGTHRXN1_129, K34 MGTHTXP1_129, J31 MGTHTXN1_129, J32

2	129	GTH	• PE4_RX2_P • PE4_RX2_N • PE4_TX2_P • PE4_TX2_N	J4-E4 J4-F4 J4-B4 J4-C4	MGTHRXP2_129, H33 MGTHRXN2_129, H34 MGTHTXP2_129, H29 MGTHTXN2_129, H30
3	129	GTH	• PE4_RX3_P • PE4_RX3_N • PE4_TX3_P • PE4_TX3_N	J4-K4 J4-L4 J4-H4 J4-I4	MGTHRXP3_129, F33 MGTHRXN3_129, F34 MGTHTXP3_129, G31 MGTHTXN3_129, G32
0	130	GTH	• PE5_RX0_P • PE5_RX0_N • PE5_TX0_P • PE5_TX0_N	J4-D5 J4-E5 J4-A5 J4-B5	MGTHRXP3_130, B33 MGTHRXN3_130, B34 MGTHTXP3_130, A31 MGTHTXN3_130, A32
1	130	GTH	• PE5_RX1_P • PE5_RX1_N • PE5_TX1_P • PE5_TX1_N	J4-J5 J4-K5 J4-G5 J4-H5	MGTHRXP2_130, C31 MGTHRXN2_130, C32 MGTHTXP2_130, B29 MGTHTXN2_130, B30
2	130	GTH	• PE5_RX2_P • PE5_RX2_N • PE5_TX2_P • PE5_TX2_N	J4-E6 J4-F6 J4-B6 J4-C6	MGTHRXP1_130, D33 MGTHRXN1_130, D34 MGTHTXP1_130, D29 MGTHTXN1_130, D30
3	130	GTH	• PE5_RX3_P • PE5_RX3_N • PE5_TX3_P • PE5_TX3_N	J4-K6 J4-L6 J4-H6 J4-I6	MGTHRXP0_130, E31 MGTHRXN0_130, E32 MGTHTXP0_130, F29 MGTHTXN0_130, F30
0	230	GTH	• PE6_RX0_P • PE6_RX0_N • PE6_TX0_P • PE6_TX0_N	J4-D7 J4-E7 J4-A7 J4-B7	MGTHRXP3_230, A4 MGTHRXN3_230, A3 MGTHTXP3_230, A8 MGTHTXN3_230, A7
1	230	GTH	• PE6_RX1_P • PE6_RX1_N • PE6_TX1_P • PE6_TX1_N	J4-J7 J4-K7 J4-G7 J4-H7	MGTHRXP2_230, B2 MGTHRXN2_230, B1 MGTHTXP2_230, B6 MGTHTXN2_230, B5
2	230	GTH	• PE6_RX2_P • PE6_RX2_N • PE6_TX2_P • PE6_TX2_N	J4-E8 J4-F8 J4-B8 J4-C8	MGTHRXP1_230, C4 MGTHRXN1_230, C3 MGTHTXP1_230, D6 MGTHTXN1_230, D5
3	230	GTH	• PE6_RX3_P • PE6_RX3_N • PE6_TX3_P • PE6_TX3_N	J4-K8 J4-L8 J4-H8 J4-I8	MGTHRXP0_230, D2 MGTHRXN0_230, D1 MGTHTXP0_230, E4 MGTHTXN0_230, E3

cPCI J4 MGT lanes

CompactPCI Serial Connector J5

MGT Lane	Bank	Type	Signal Schematic Name	cPCI Connector Pin	FPGA Pin
0	228	GTH	• PE8_RX0_P • PE8_RX0_N • PE8_TX0_P • PE8_TX0_N	J5-D3 J5-E3 J5-A3 J5-B3	MGTHRXP0_228, T2 MGTHRXN0_228, T1 MGTHTXP0_228, R4 MGTHTXN0_228, R3
1	228	GTH	• PE8_RX1_P • PE8_RX1_N • PE8_TX1_P • PE8_TX1_N	J5-J3 J5-K3 J5-G3 J5-H3	MGTHRXP1_228, P2 MGTHRXN1_228, P1 MGTHTXP1_228, P6 MGTHTXN1_228, P5
2	228	GTH	• PE8_RX2_P • PE8_RX2_N • PE8_TX2_P • PE8_TX2_N	J5-E4 J5-F4 J5-B4 J5-C4	MGTHRXP2_228, M2 MGTHRXN2_228, M1 MGTHTXP2_228, N4 MGTHTXN2_228, N3
3	228	GTH	• PE8_RX3_P • PE8_RX3_N • PE8_TX3_P • PE8_TX3_N	J5-K4 J5-L4 J5-H4 J5-I4	MGTHRXP3_228, L4 MGTHRXN3_228, L3 MGTHTXP3_228, M6 MGTHTXN3_228, M5
0	229	GTH	• PE7_RX0_P • PE7_RX0_N • PE7_TX0_P • PE7_TX0_N	J5-D1 J5-E1 J5-A1 J5-B1	MGTHRXP0_229, K2 MGTHRXN0_229, K1 MGTHTXP0_229, K6 MGTHTXN0_229, K5
1	229	GTH	• PE7_RX1_P • PE7_RX1_N • PE7_TX1_P • PE7_TX1_N	J5-J1 J5-K1 J5-G1 J5-H1	MGTHRXP1_229, J4 MGTHRXN1_229, J3 MGTHTXP1_229, H6 MGTHTXN1_229, H5
2	229	GTH	• PE7_RX2_P • PE7_RX2_N • PE7_TX2_P • PE7_TX2_N	J5-E2 J5-F2 J5-B2 J5-C2	MGTHRXP2_229, H2 MGTHRXN2_229, H1 MGTHTXP2_229, G4 MGTHTXN2_229, G3
3	229	GTH	• PE7_RX3_P • PE7_RX3_N • PE7_TX3_P • PE7_TX3_N	J5-K2 J5-L2 J5-H2 J5-I2	MGTHRXP3_229, F2 MGTHRXN3_229, F1 MGTHTXP3_229, F6 MGTHTXN3_229, F5

cPCI J5 MGT lanes

PLL Clock U14 Output	Signal Schematic Name	cPCI Connector J5 Pin	Notes

OUT1	• PE1_CLK_P • PE1_CLK_N	J5-A5 J5-B5	reference clock signals supplied by on-board 10-output PLL clock generator U14
OUT2	• PE2_CLK_P • PE2_CLK_N	J5-D5 J5-E5	
OUT3	• PE3_CLK_P • PE3_CLK_N	J5-G5 J5-H5	
OUT4	• PE4_CLK_P • PE4_CLK_N	J5-J5 J5-K5	
OUT5	• PE5_CLK_P • PE5_CLK_N	J5-B6 J5-C6	
OUT6	• PE6_CLK_P • PE6_CLK_N	J5-E6 J5-F6	
OUT7	• PE7_CLK_P • PE7_CLK_N	J5-H6 J5-I6	
OUT8	• PE8_CLK_P • PE8_CLK_N	J5-K6 J5-L6	

cPCI J5 clock signals

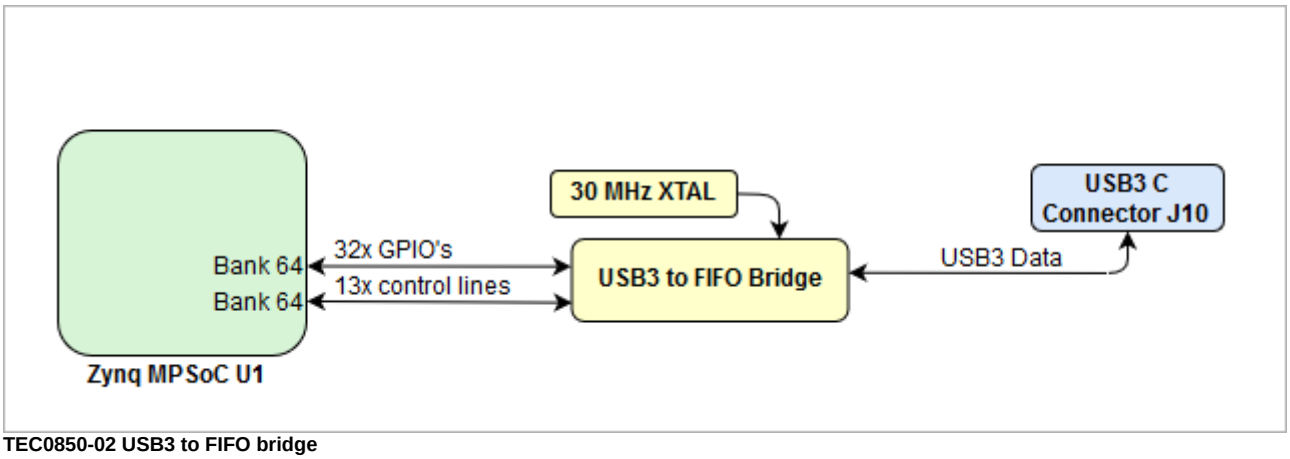
CompactPCI Serial Connector J6

Interfaces	I/O Signal Count	LVDS-pairs count	Connected to	VCCO bank Voltage	Notes
I/O	46	23	PL bank 66	PL_1.8V	-
	18	9	PL bank 65	PL_1.8V	-
	2	-	SC FPGA U18 Bank 1B	+3V_D	Signalname: 'DET_RIO', 'DET_BPR'

cPCI J6 Interfaces

USB-C Connector

Front panel USB-C Interface is connected to USB FIFO bridge chip FT601Q. 32-bit FIFO bridge provides a simple high-speed interface to Zynq UltraScale+ PL.



TEC0850-02 USB3 to FIFO bridge

The USB 3.0 to FIFO bridge FTDI FT601Q U9 is connected to the Zynq MPSoC's PL bank 64 and is accessible through USB-C connector J10:

Interface	Signal Schematic Names	Connected to	Notes
USB3 data lane	• SSRX_P • SSRX_N • SSTXX_P • SSTXX_N	USB C Connector J10	-
USB2 data lane	• SS_D_P • SS_D_N	USB C Connector J10	-
Control Lines	• FTDI_RESET_N • WAKEUP_N • SIWU_N • TXE_N • RXF_N • WR_N • RD_N • OE_N • BE_0 • BE_1 • BE_2 • BE_3 • FIFO_CLK	PL bank 64	-
Parallel GPIO's	• DATA0 • . • . • DATA31	PL bank 64	32bit FIFO register

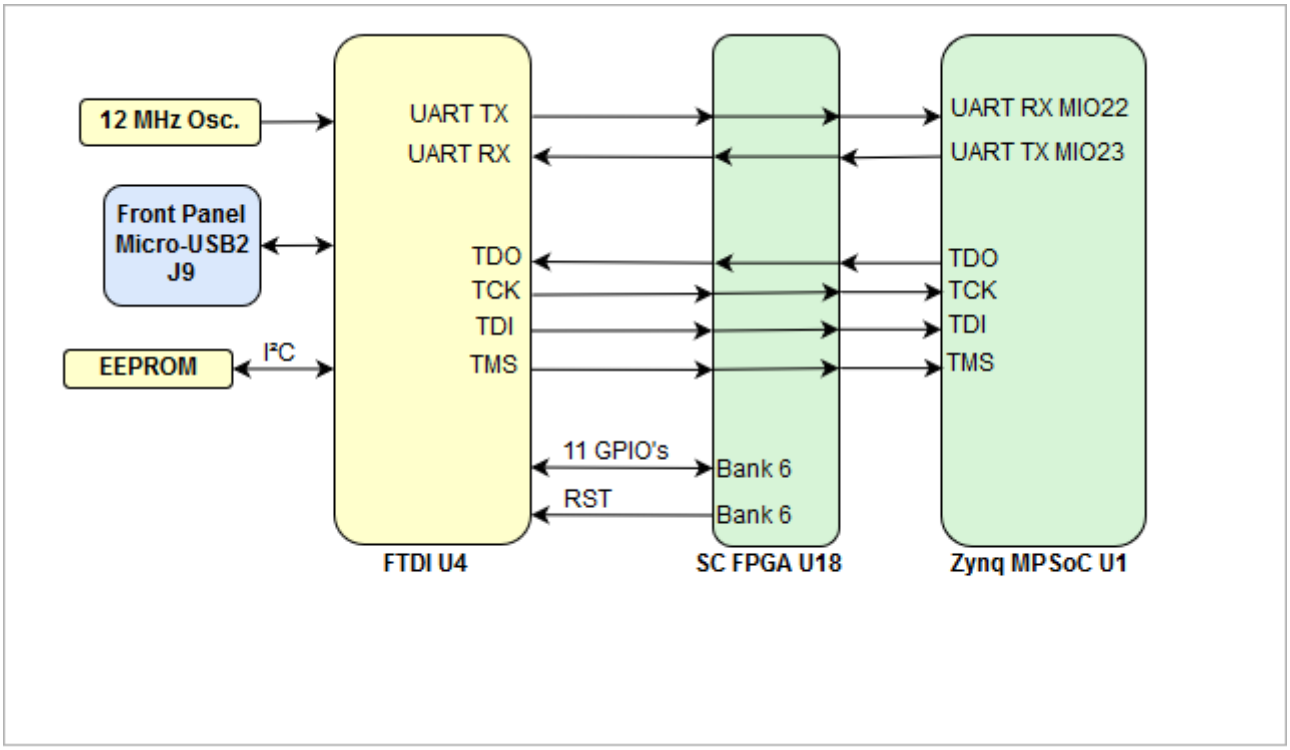
USB-C connector J10

See FT600Q-FT601Q IC Datasheet for interface details.

Micro-USB2 Connector

Front panel Micro-USB2 Interface provides access to UART and JTAG functions via FTDI FT2232 chip. Use of this feature requires that USB driver is installed on your host PC. UART0 with MIO 22 .. 23 should be selected in "Zynq UltraScale+ MPSoC" configuration.

The Digilent plug-in software and cable drivers must be installed on your machine for you to be able to use JTAG interface.



JTAG/UART Interface

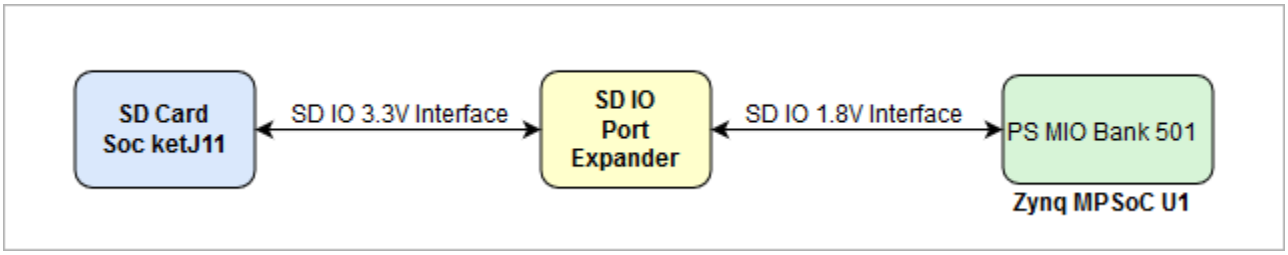
The USB2 to FIFO bridge FTDI FT2232H U4 is connected to the SC FPGA U18 and is accessible through Micro-USB2 connector J9:

Interface	Signal Schematic Names	Connected to	Notes
USB2 data lane	• USB_P • USB_N	Micro-USB2 connector J9	-
Control Lines	• FTDI_RST	SC FPGA U18, bank 6	-
Parallel GPIO's	• ADBUS0 • ADBUS1 • ADBUS2 • ADBUS3 • BDBUS0 • BDBUS1 • BDBUS2 • BDBUS3 • BDBUS4 • BDBUS5 • BDBUS6 • BDBUS7 • BCBUS0 • BCBUS1 • BCBUS2 • BCBUS3 • BCBUS4	SC FPGA U18, bank 6	-

Micro-USB2 connector J9

SD

The SD Card interface of the TEC0850 board is not directly wired to the connector J11 pins but through a Texas Instruments TXS02612 SD IO Port Expander, which is needed for voltage translation due to different voltage levels of the Micro SD Card and MIO-bank of the Xilinx Zynq MPSoC. The Micro SD Card has 3.3V signal voltage level, but the PS MIO-bank on the Xilinx Zynq MPSoC has VCCIO of 1.8V.



MicroSD Card interface

There are some limitations to use SD card Interface in Linux.

- Zynq UltraScale+ SD controller is working only in the 3.3V mode as it connected to SD card socket using SD IO port expander U10 as 1.8V to 3.3 V level shifter.
- Micro SD card socket has no "Write Protect" switch.

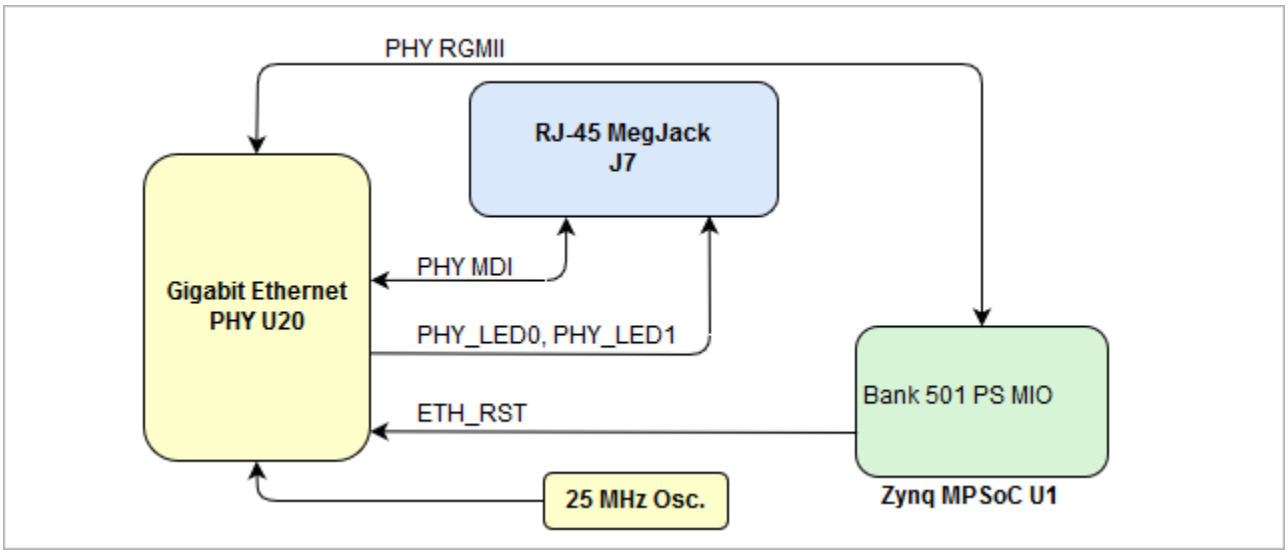
To force Linux driver not to use these features to add following instructions to device tree file.

```
&sdhci1 {

no-1-8-v;
disable-wp;
};
```

RJ45 - Ethernet

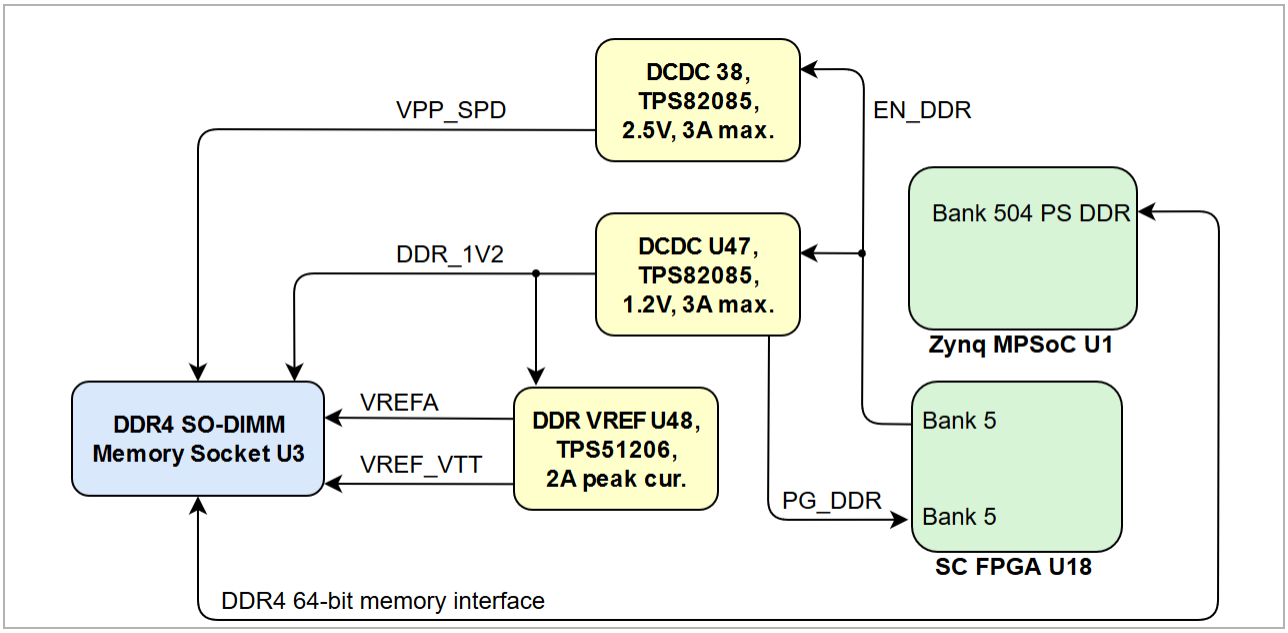
Onboard Gigabit Ethernet PHY is provided with Marvell Alaska 88E1512 IC U20. The Ethernet PHY RGMII interface is connected to the Zynq MPSoC Ethernet interface of the PS MIO bank 501. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from the on-board 25.000000 MHz oscillator U21. The LEDs of the RJ-45 MegJack J13 are connected to the GbE PHY U20 status LED output.



Gigabit Ethernet Interface

DDR4 SODIMM Socket

On the TEC0850 board, there is a DDR4 memory interface U3 with a 64-bit data bus width available for SO-DIMM modules connected to the Zynq UltraScale+ DDRC hard memory controller.



DDR4 SDRAM SODIMM socket

Following table gives an overview of the memory interface I/O signals of the DDR4 SDRAM SO-DIMM Socket U3:

DDR4 SDRAM I/O Signal	Signal Schematic Name	Connected to	Notes

Address inputs	• DDR4-A0 ... DDR4-A16	PS DDR Bank 504	-
Bank address inputs	• DDR4-BA0 / DDR4-BA1		-
Bank group inputs	• DDR4-BG0 / DDR4-BG1		-
Differential clocks	• DDR4-CLK0_P • DDR4-CLK0_N • DDR4-CLK1_P • DDR4-CLK1_N		2 x DDR4 clock
Data input/output	• DQ0 ... DQ63		-
Check bit input/output	• CB0 ... CB7		-
Data strobe (differential)	• DDR4-DQS0_P • DDR4-DQS0_N • ... • DDR4-DQS8_P • DDR4-DQS8_N		-
Data mask and data bus inversion	• DDR4-DM0 ... DDR4-DM8		-
Serial address inputs	• DDR4-SA0 ... DDR4-SA2		address range configuration on I²C bus
Control Signals	• DDR4-CS_N0 / DDR4-CS_N1		chip select signal
	• DDR4-ODT0 / DDR4-ODT1		On-die termination enable
	• DDR4-RESET		nRESET
	• DDR4-PAR		Command and address parity input
	• DDR4-CKE0 / DDR4-CKE1		Clock Enable
	• DDR4-ALERT		CRC error flag
	• DDR4-ACT		Activation command input
	• DDR4-EVENT		Temperature event

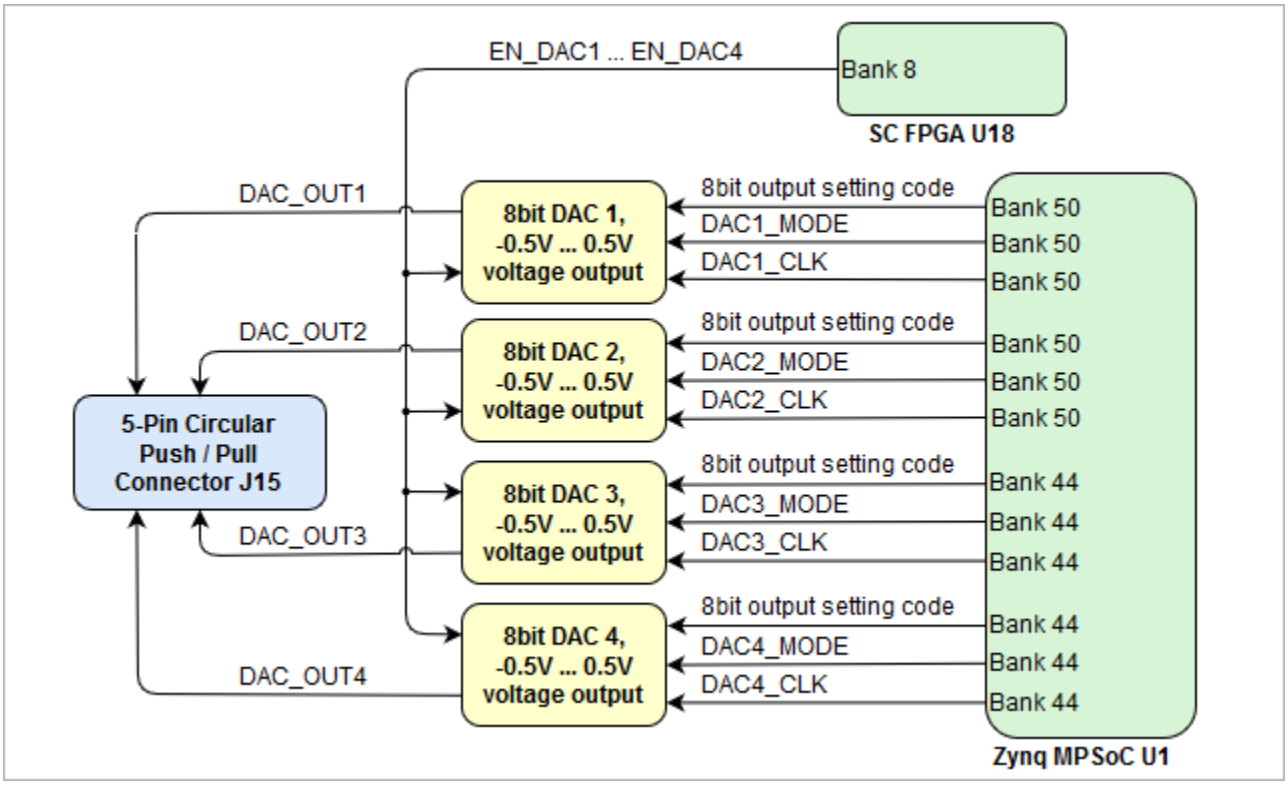
I²C	• DDR4-SCL • DDR4-SDA	not connected	-

DDR4 SDRAM SO-DIMM socket U3

Circular Push Pull Connector

The TEC0850 board provides 4x DAC analog voltage output on the 5-pin circular push/pull connector J15. Each of the DAC units consists of one Texas Instruments THS5641AIPW digital to analog converter, TI THS4631D operational amplifier and two LDOs, by which the DAC unit can be switched on and off.

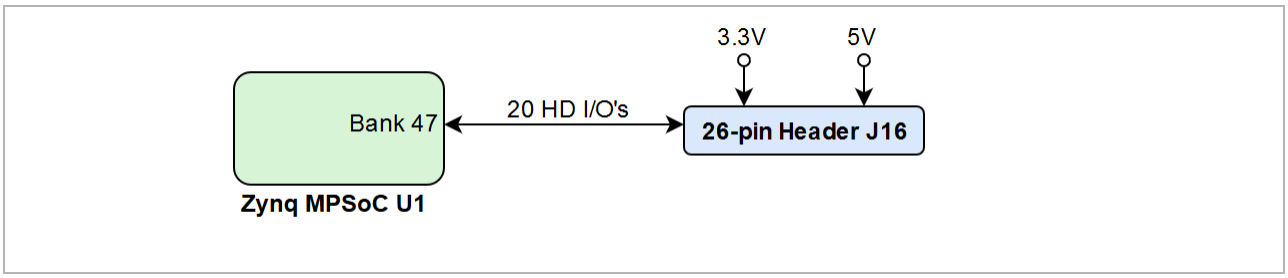
The TI THS4631D digital to analog converter wired to the operational amplifier circuitry creating the DAC unit with a voltage output range from -0.5V ... 0.5 V. See TI THS5641 datasheet and schematic how to control the DAC unit and to set the analog output voltages on connector J15.



4x 8bit DAC units

26-Pin IDC Header

There is a 26-pin IDC header (2x13, 1.27mm grid size) J16 available on the TEC0850 board which exposes the 20 FPGA HD I/O's of PL bank 47 to the user. The PL bank 47 has 3.3V VCCO bank voltage, on the header J16 there also the voltage levels 3.3V and 5V available. The I/O's can be accessed with a corresponding IDC connector.



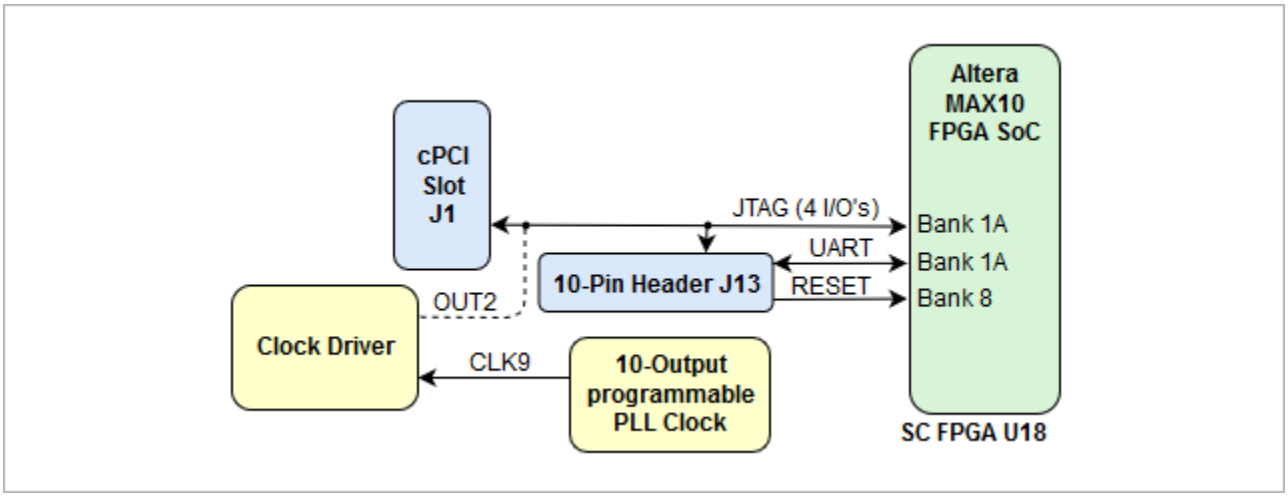
Zynq MPSoC PL I/O's IDC pin-header

10-Pin Header

On the TEC0850 there is a 10-pin SMT header (2x5, 2.54mm grid size) J13 present which provides access to the JTAG and UART interface of Altera MAX10 System Controller FPGA. The header J13 has a compatible pin assignment to the TEI0004 JTAG programmer for Altera FPGAs, the voltage levels 3.3V is on the header available as a reference I/O-voltage for JTAG and UART.

The 4 JTAG pins of the header J13 are also connected to the cPCI connector J1 and can be used as user GPIO's of the SC FPGA U18 with other functionalities then JTAG.

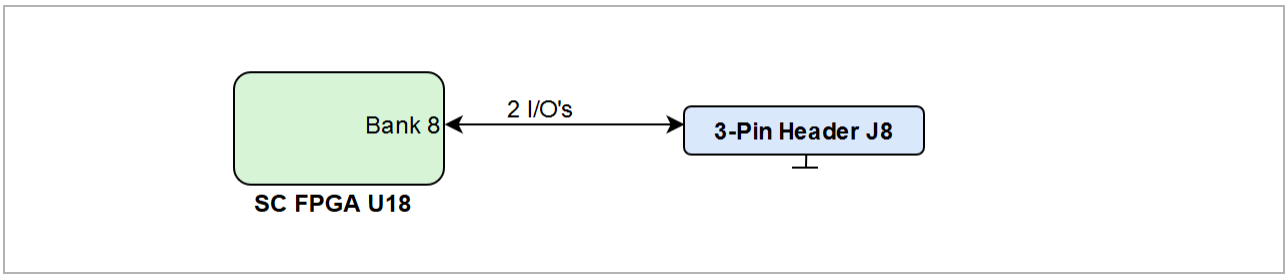
On the header J13, there is also a optional reference clock signal from PLL clock U14 available, if the necessary resistors and capacitors are fitted on board. The clock can also be used for the SC FPGA U18 and on the cPCI connector J1.



10-pin JTAG/UART header

3-Pin PicoBlade Header

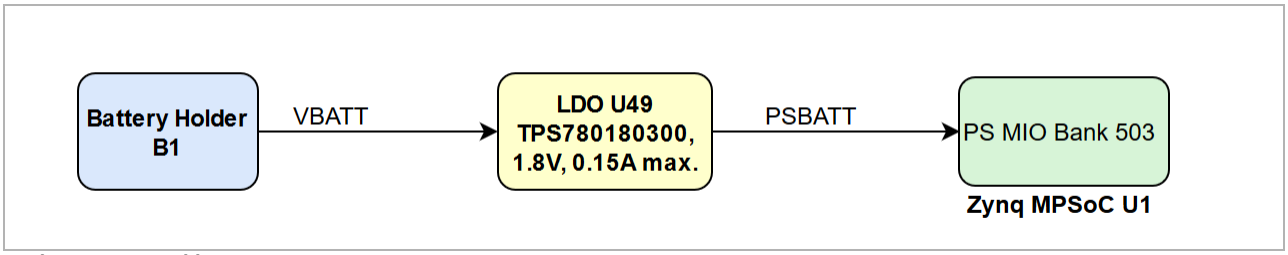
2 I/O's of the SC FPGA U18 are exposed to the on-board 3-Pin PicoBlade header J8 available to the user or for future use of upcoming versions of SC FPGA firmware.



3-pin PicoBlade header

Battery Holder

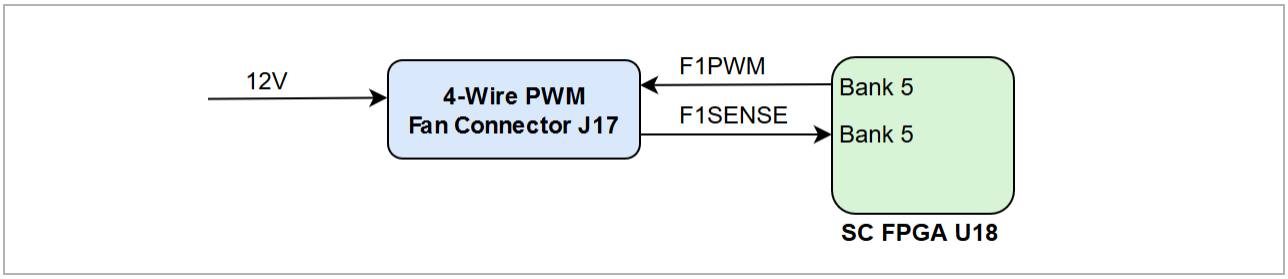
There is a CR1220 battery holder available to the supply the voltage for the Zynq MPSoC's Battery Power Domain (BBRAM and RTC). The battery voltage VBATT should be in the range of 2.2V to 5.5V, use the 3.0V CR1220 battery.



Backup-Battery Holder

4-Wire PWM FAN Connectors

The TEC0850 offers one 4-wire PWM FAN connector FPGA cooling fan controlled by SC FPGA U18:



4-wire PWM FAN connector

Onboard Peripherals

Zynq UltraScale XCZU15EG MPSoC

The TEC0850 board is populated with the Zynq UltraScale+ XCZU15EG-1FFVB1156E MPSoC.

The PS MIO pins are routed to the onboard peripherals as follows:

PS MIO	Function	Connected to
0	QSPI*	U24-B2, CLK
1	QSPI*	U24-D2, DO/IO1
2	QSPI*	U24-C4, WP/IO2
3	QSPI*	U24-D4, HOLD/IO3
4	QSPI*	U24-D3, DI/IO0

5	QSPI*	U24-C2, CS
6	-	not connected
7	QSPI*	U25-C2, CS
8	QSPI*	U25-D3, DI/IO0
9	QSPI*	U25-D2, DO/IO1
10	QSPI*	U17-C4, WP/IO2
11	QSPI*	U25-D4, HOLD/IO3
12	QSPI*	U25-B2, CLK
13 ... 15	-	not connected
16	USB2 PHY Reset	USB2 PHY U11, pin27
17	USB2 PHY Reset	USB2 PHY U13, pin27 (optional, PHY not fitted by default)
18 ... 19	-	not connected
20 ...21	PS MIO I²C	I²C peripherals
22 ... 25	user MIO	SC FPGA U18, bank 2
26 ... 38	RGMII	GbE PHY U20
39 ... 44	-	not connected
45 ... 51	SD IO	MicroSD Card socket J11
52 ... 63	USB2 ULPI	USB2 PHY U11
64 ... 75	USB2 ULPI	USB2 PHY U13 (optional, PHY not fitted by default)
76 ... 77	ETH MDC / MDIO	GbE PHY U20

* Flash is used as QSPI dual parallel
Default MIO Configuration

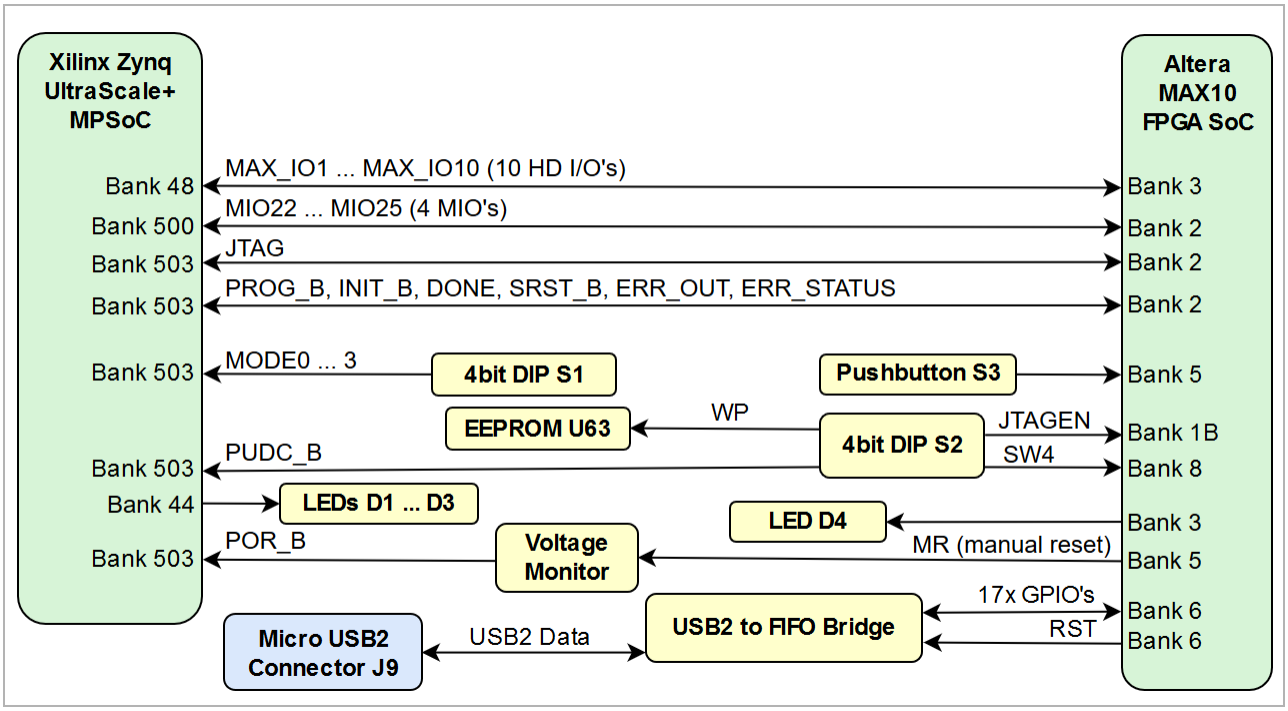
MAX10 System Controller FPGA

The TEC0850 board is equipped with one System Controller FPGA (Intel MAX10 10M08SAU169C8G) with the schematic designators U18. The SC FPGA is the central system management unit where essential control signals are logically linked by the implemented logic in FPGA firmware, which generates output signals to control the system, the onboard peripherals, and the interfaces. Interfaces like JTAG and UART between the FTDI FT2232H chip and to the Zynq MPSoC are by-passed, forwarded and controlled by the System Controller FPGA.

Other tasks of the System Controller FPGA are the monitoring of the power-on sequence and to display the programming state of the FPGA module. The functionalities and configuration of the pins depending on the SC FPGA's firmware. The documentation of the firmware of SC FPGA U18 contains detailed information on this matter.

The System Controller FPGA is connected to the Zynq Ultrascale+ MPSoC through MIO and PL pins. The signals of these pins are forwarded by the SC FPGA to control some of the onboard peripherals.

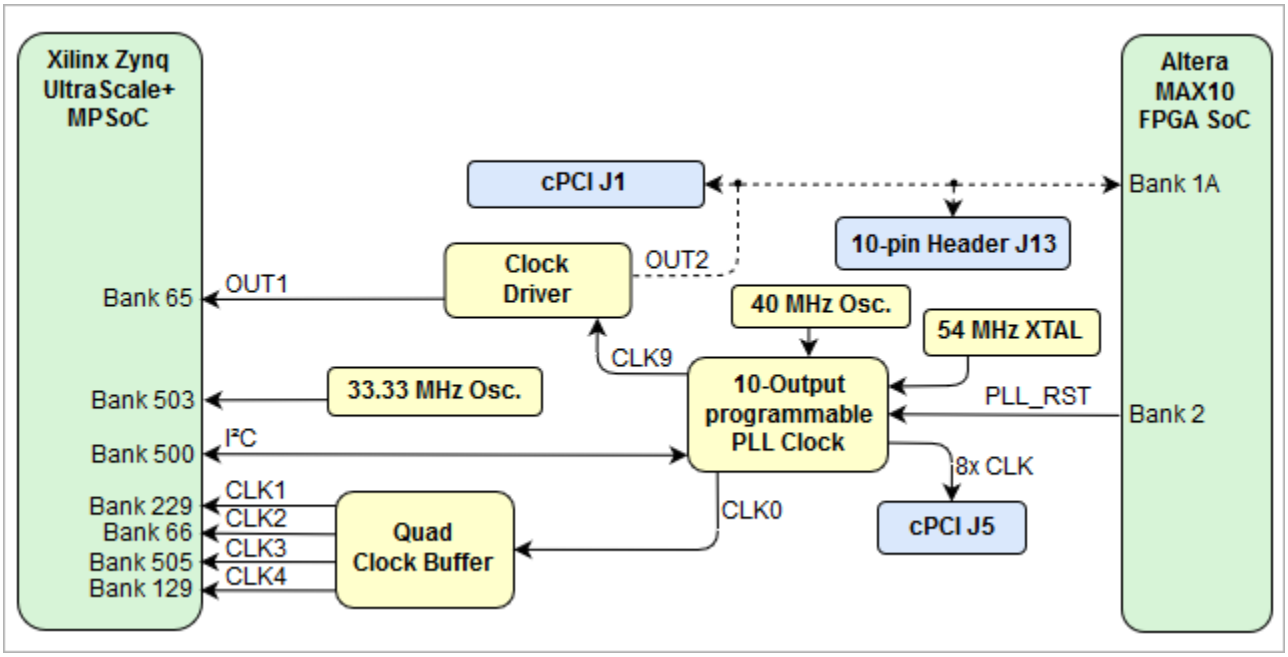
Following block diagram visualizes the connection of the SC FPGA with the Zynq Ultrascale+ MPSoC via 4 PS MIO pins (MIO22 ... 25), PS Config control signals and 10 singled ended PL HD bank 48 I/O pins (MAX_IO1 ... MAX_IO10):



TEC0850 MAX10 System Controller FPGA

Programmable Clock Generator

There is a Si5345A U14, Silicon Labs I^{2}C programmable 10-output PLL clock generator on-board to generate various reference clocks for the Zynq MPSoC MGT banks and onboard peripherals.



10-output I²C programmable clock generator

Following table shows onboard Silicon Labs I^2C programmable Si5345A U17 10-output programmable PLL reference clock generator inputs and outputs:

Si5345A U14 Pin	Signal Schematic Name	Connected to	Signal Direction	Note
IN0	• IN0_P	40.000 MHz Oscillator U75	Input	external reference clock input
	• IN0_N	GND		
IN1	-	not connected	Input	not used
	-	not connected		
IN2	-	not connected	Input	not used
	-	not connected		
IN3	-	not connected	Input	not used
	-	not connected		
OUT0	• CLK0_P	Quad clock buffer Si53340 U16	Output	reference clock input to Quad clock buffer
	• CLK0_N			
OUT1	• PE1_CLK_N	cPCI J5, pin B5	Output	reference clock output to cPCI connector J5
	• PE1_CLK_P	cPCI J5, pin A5		
OUT2	• PE5_CLK_N	cPCI J5, pin C6	Output	
	• PE5_CLK_P	cPCI J5, pin B6		
OUT3	• PE2_CLK_N	cPCI J5, pin E5	Output	
	• PE2_CLK_P	cPCI J5, pin D5		
OUT4	• PE3_CLK_N	cPCI J5, pin H5	Output	
	• PE3_CLK_P	cPCI J5, pin G5		
OUT5	• PE4_CLK_N	cPCI J5, pin K5	Output	
	• PE4_CLK_P	cPCI J5, pin J5		

OUT6	• PE6_CLK_N	cPCI J5, pin F6	Output	
	• PE6_CLK_P	cPCI J5, pin E6		
OUT7	• PE8_CLK_N	cPCI J5, pin L6	Output	
	• PE8_CLK_P	cPCI J5, pin K6		
OUT8	• PE7_CLK_N	cPCI J5, pin I6	Output	
	• PE7_CLK_P	cPCI J5, pin H6		
OUT9	• CLK9_P	Clock Driver LTC6975 U73	Output	reference clock input to dual clock driver U73
	• CLK9_N			
XA/XB	• XAXB_P	54.000 MHz quartz oscillator Y3	Input	Differential quartz oscillator clock input
	• XAXB_N			
SCLK, SDA/SDIO	• I2C_SCL • I2C_SDA	• MIO20 • MIO21	BiDir	I²C address 0x69

SI5345 Clock Outputs

The clock outputs OUT1 and OUT9 are distributed via clock buffer U16 and clock driver U14 to several PL and MGT banks:

Si53340 U16 Pin	Signal Schematic Name	Connected to	Signal Direction	Note
Q0	• CLK1_P • CLK1_N	U1, pin G8 U1, pin G7	Output	GTH bank 229 reference clock input
Q1	• CLK2_P • CLK2_N	U1, pin Y8 U1, pin Y7	Output	PL HP bank 66 reference clock input
Q2	• CLK3_P • CLK3_N	U1, pin U27 U1, pin U28	Output	PS GTR Bank 505 reference clock input
Q3	• CLK4_P • CLK4_N	U1, pin L27 U1, pin L28	Output	GTH bank 129 reference clock input
LTC6957 U73 Pin				

OUT1	• CK_PLL_P • CK_PLL_N	U1, pin AG5 U1, pin AG4	Output	PL HP bank 65 reference clock input
OUT2	• CK_P • CK_N	Signal 'SATA_SL' Signal 'SATA_SCL'	Output	optional reference clock input to cPCI connector J1, if decoupling capacitors and resistors are fitted (see schematic), also shared with SC FPGA and header J13

Clock driver and buffer outputs

The clock generator U14 is programmable via the onboard I²C bus connected to MIO 20...21 pins. The I²C address is shown in the table below.

I2C address	Chip	Description
0x69	U14 Si5345	Clock generator and distributor

SI5345 I2C address

Oscillators

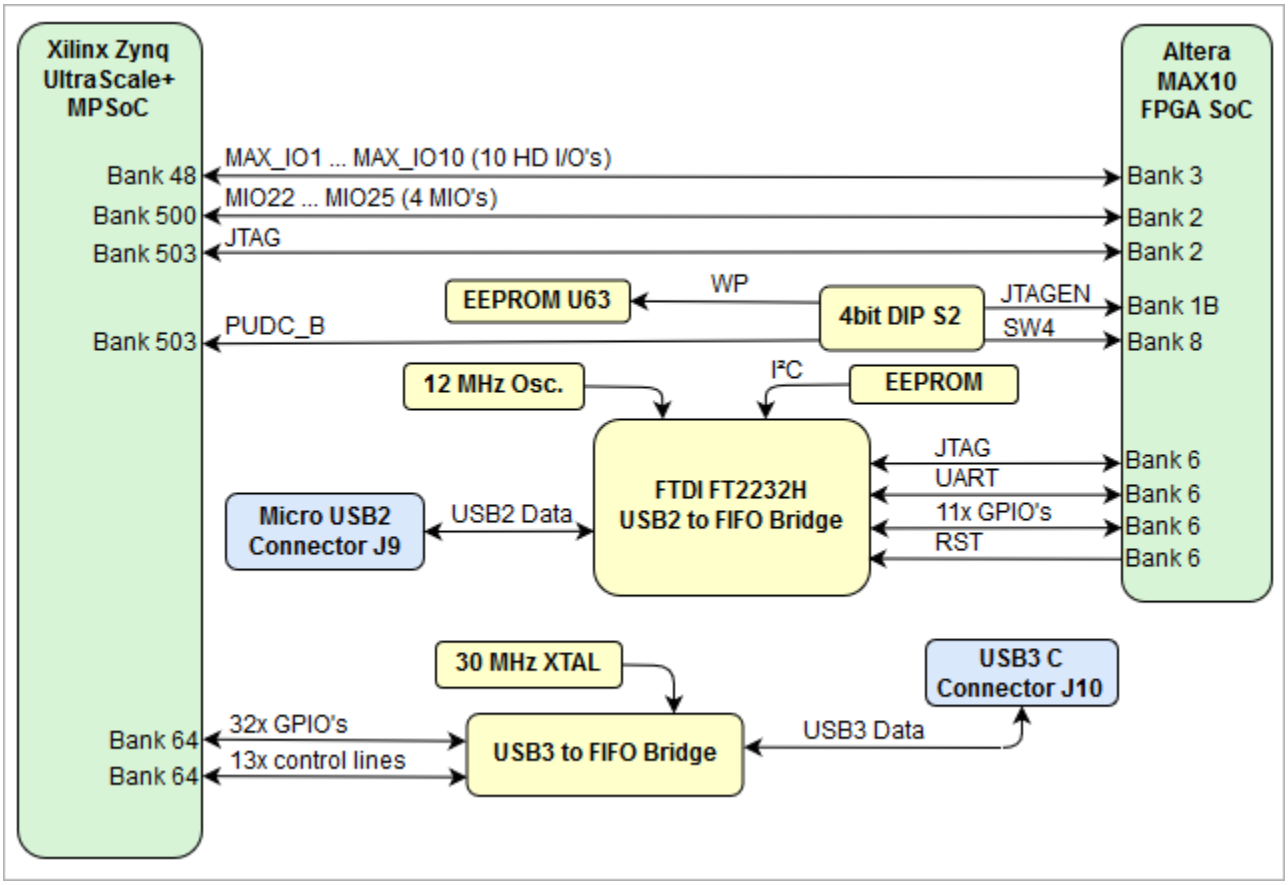
The TEC0850 board is equipped several onboard oscillators to provide the Zynq Ultrascale+ MPSoC's PS and PL banks and the onboard peripherals with reference clock-signals:

Clock Source	Signal Schematic Name	Frequency	Clock Input Destination
SiTime SiT8008BI oscillator, U22	• PS_CLK	33.333333 MHz	Zynq MPSoC U1 PS Config Bank 503, pin U24
SiTime SiT8008AI oscillator, U12	• USB0_CLK	52.000000 MHz	USB2 transceiver PHY U11, pin 26
SiTime SiT8008AI oscillator, U16	• OSCI	12.000000 MHz	FTDI FT2232H U4, pin 3
Kyocera CX3225SB30000, Y1	-	30.000 MHz	FTDI FT601Q U9, pin 21/22
CM-2012-2pad, Y2	-	32.768000 kHz	Zynq MPSoC U1 PS Config Bank 503, pin V21/V22
Kyocera CX3225SB26000, Y3	• XAXB_P • XAXB_N	54.000 MHz	10-output PLL clock generator U14, pin 8/9
SiTime SiT8008BI oscillator, U21	• ETH_CLKIN	25.000000 MHz	Gigabit Ethernet PHY U20, pin 34
ASVTX-12-A oscillator, U75	• IN0_P	40.000 MHz	10-output PLL clock generator U14, pin 63

TEC0850 on-board oscillators

FTDIs

The TEC0850 board is equipped with 2 FTDI chips FT2232H (U4) and FT601Q (U9). Both chips are USB to Multipurpose UART/FIFO bridges which converts signals from USB2 or USB3 to a variety of standard serial and parallel interfaces.



TEC0850 on-board FTDI chips

FT2232H

The TEC0850 board is equipped with the FTDI FT2232H USB2 to JTAG/UART adapter controller connected to micro-USB2 connector J9 to provide JTAG and UART access to the Xilinx UltraScale+ Zynq SoC or Intel MAX10 (switchable over DIP) . There is also a 256-byte configuration EEPROM U6 wired to the FT2232H chip via Microwire bus which holds pre-programmed license code to support Xilinx programming tools. Refer to the FTDI datasheet to get information about the capacity of the FT2232H chip.

> Do not access the FT2232H EEPROM using FTDI programming tools, doing so will erase normally invisible user EEPROM content and invalidate stored Xilinx JTAG license. Without this license, the onboard JTAG will not be accessible anymore with any Xilinx tools. Software tools from the FTDI website do not warn or ask for confirmation before erasing user EEPROM content.

Channel A of the FTDI IC is configured as JTAG interface (MPSSE) connected to the SC FPGA U18, the JTAG signals are forwarded to the JTAG interface of the Zynq MPSoC on PS config bank 503.

Channel B can be used as UART Interface routed to SC FPGA U18, 11 I/O's of Channel B is routed to are usable for example as GPIOs and other standard interfaces.

FT2232H U3 Pin	Signal Schematic Name	Connected to	Notes
Pin 12, ADBUS0	ADBUS0	SC FPGA U18 bank 6, pin G9	JTAG interface
Pin 13, ADBUS1	ADBUS1	SC FPGA U18 bank 6, pin F10	
Pin 14, ADBUS2	ADBUS2	SC FPGA U18 bank 6, pin E10	

Pin 15, ADBUS3	ADBUS3	SC FPGA U18 bank 6, pin D9	
Pin 32, BDBUS0	BDBUS0	SC FPGA U18 bank 6, pin B11	UART and user configurable GPIO's
Pin 33, BDBUS1	BDBUS1	SC FPGA U18 bank 6, pin A12	
Pin 34, BDBUS2	BDBUS2	SC FPGA U18 bank 6, pin B12	
Pin 35, BDBUS3	BDBUS3	SC FPGA U18 bank 6, pin C11	
Pin 37, BDBUS4	BDBUS4	SC FPGA U18 bank 6, pin B13	
Pin 38, BDBUS5	BDBUS5	SC FPGA U18 bank 6, pin C12	
Pin 39, BDBUS6	BDBUS6	SC FPGA U18 bank 6, pin C13	
Pin 40, BDBUS7	BDBUS7	SC FPGA U18 bank 6, pin D11	
Pin 42, BCBUS0	BCBUS0	SC FPGA U18 bank 6, pin D12	
Pin 46, BCBUS1	BCBUS1	SC FPGA U18 bank 6, pin E13	
Pin 47, BCBUS2	BCBUS2	SC FPGA U18 bank 6, pin E12	
Pin 48, BCBUS3	BCBUS3	SC FPGA U18 bank 6, pin F13	
Pin 49, BCBUS4	BCBUS4	SC FPGA U18 bank 6, pin F12	
Pin 11, nRESET	FTDI_RST	SC FPGA U18 bank 6, pin E9	control signals

FT2232H interface connections

FT601Q

The TEC0850 board is equipped with the FTDI FT601Q USB3 to 32bit-FIFO adapter controller connected to USB-C connector J10 to provide access to the Zynq MPSoC PL HP I/O's of bank 64. Also, 13 control signals of the FTDI FT601Q are connected to the HP bank 64.

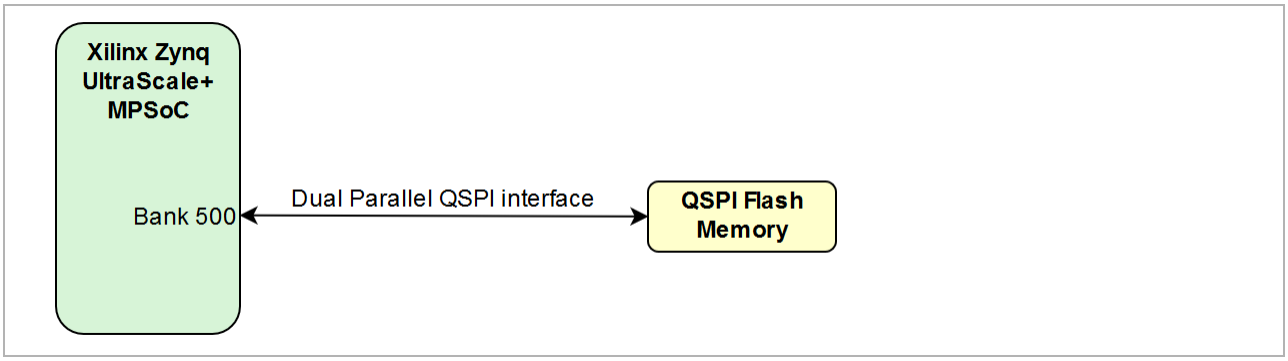
FT601Q U9 Pin	Signal Schematic Name	Connected to	Notes
Pin 40, DATA0	DATA0	PL HP bank 64, pin AK1	user GPIO's
Pin 41, DATA1	DATA1	PL HP bank 64, pin AJ10	
Pin 42, DATA2	DATA2	PL HP bank 64, pin AJ9	
Pin 43, DATA3	DATA3	PL HP bank 64, pin AK7	
Pin 44, DATA4	DATA4	PL HP bank 64, pin AK5	
Pin 45, DATA5	DATA5	PL HP bank 64, pin AM1	
Pin 46, DATA6	DATA6	PL HP bank 64, pin AL2	
Pin 47, DATA7	DATA7	PL HP bank 64, pin AK4	
Pin 50, DATA8	DATA8	PL HP bank 64, pin AN1	
Pin 51, DATA9	DATA9	PL HP bank 64, pin AL3	
Pin 52, DATA10	DATA10	PL HP bank 64, pin AK8	
Pin 53, DATA11	DATA11	PL HP bank 64, pin AN2	
Pin 54, DATA12	DATA12	PL HP bank 64, pin AP2	
Pin 55, DATA13	DATA13	PL HP bank 64, pin AL7	
Pin 56, DATA14	DATA14	PL HP bank 64, pin AL5	
Pin 57, DATA15	DATA15	PL HP bank 64, pin AM4	
Pin 60, DATA16	DATA16	PL HP bank 64, pin AN4	
Pin 61, DATA17	DATA17	PL HP bank 64, pin AM5	
Pin 62, DATA18	DATA18	PL HP bank 64, pin AM6	

Pin 63, DATA19	DATA19	PL HP bank 64, pin AN3	
Pin 64, DATA20	DATA20	PL HP bank 64, pin AP3	
Pin 65, DATA21	DATA21	PL HP bank 64, pin AP4	
Pin 66, DATA22	DATA22	PL HP bank 64, pin AP5	
Pin 67, DATA23	DATA23	PL HP bank 64, pin AN6	
Pin 69, DATA24	DATA24	PL HP bank 64, pin AN7	
Pin 70, DATA25	DATA25	PL HP bank 64, pin AP6	
Pin 71, DATA26	DATA26	PL HP bank 64, pin AP7	
Pin 72, DATA27	DATA27	PL HP bank 64, pin AP11	
Pin 73, DATA28	DATA28	PL HP bank 64, pin AP10	
Pin 74, DATA29	DATA29	PL HP bank 64, pin AP9	
Pin 75, DATA30	DATA30	PL HP bank 64, pin AN9	
Pin 76, DATA31	DATA31	PL HP bank 64, pin AP8	
Pin 58, CLK	FIFO_CLK	PL HP bank 64, pin AL6	control signals
Pin 4, BE0	BE_0	PL HP bank 64, pin AM10	
Pin 5, BE1	BE_1	PL HP bank 64, pin AK10	
Pin 6, BE2	BE_2	PL HP bank 64, pin AM11	
Pin 7, BE3	BE_3	PL HP bank 64, pin AL11	
Pin 13, nOE	OE_N	PL HP bank 64, pin AL8	
Pin 12, nRD	RD_N	PL HP bank 64, pin AK9	
Pin 11, nWR	WR_N	PL HP bank 64, pin AM9	
Pin 8, nTXE	TXE_N	PL HP bank 64, pin AK12	
Pin 9, nRXN	RXF_N	PL HP bank 64, pin AJ12	
Pin 10, nSIWU	SIWU_N	PL HP bank 64, pin AL10	
Pin 15, nRESET	FTDI_RESET_N	PL HP bank 64, pin AM8	
Pin 16, nWAKEUP	WAKEUP_N	PL HP bank 64, pin AN8	

FT601Q interface connections

Quad-SPI Flash Memory

On-board QSPI flash memory U24 and U25 on the TEC0850 board is provided by Micron Serial NOR Flash Memory N25Q256A with 256 Mbit (32 MByte) storage capacity each, 64 MByte total QSPI Flash memory. The QSPI Flash memory ICs are connected to the PS MIO bank (Dual QSPI MIO0 ... MIO12) of the Zynq Ultrascale+ MPSoC, enabling dual parallel booting from QSPI Flash memory. This nonvolatile memory is used to store an initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the Zynq MPSoC allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.



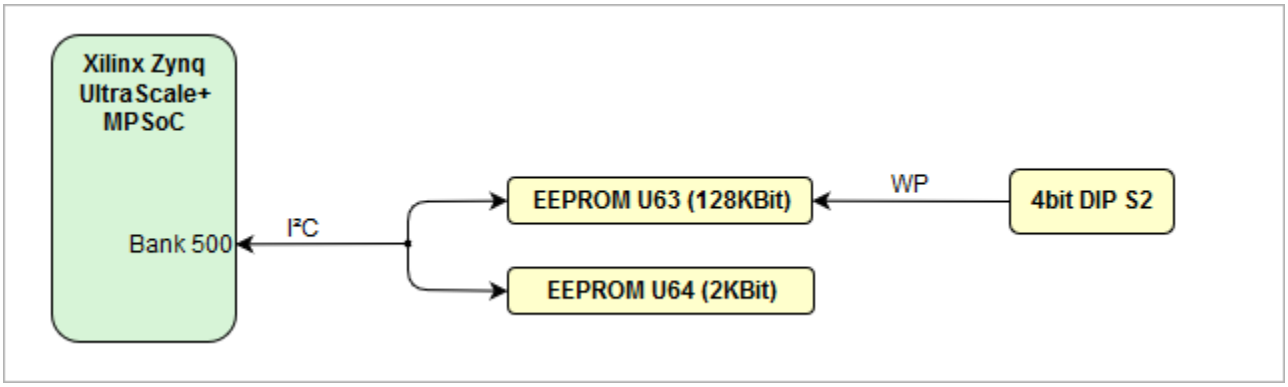
Quad-SPI Flash Memory

IC	Memory Density	MIO	Signal Schematic Name	Flash Memory Pin
QSPI Flash U24, N25Q256A11E1240E	256 Mbit (32 MByte)	0	MIO0	B2
		1	MIO1	D2
		2	MIO2	C4
		3	MIO3	D4
		4	MIO4	D3
		5	MIO5	C2
QSPI Flash U25, N25Q256A11E1240	256 Mbit (32 MByte)	7	MIO7	C2
		8	MIO8	D3
		9	MIO9	D2
		10	MIO10	C4
		11	MIO11	D4
		12	MIO12	B2

Quad-SPI Flash memory interface connections

EEPROMs

The TEC0850 board contains several EEPROMs for configuration and general user purposes. The EEPROMs are provided by Microchip, the I²C interfaces are connected to Zynq MPSoC bank 502 MIO 20...21 pins:



On-board configuration EEPROMs

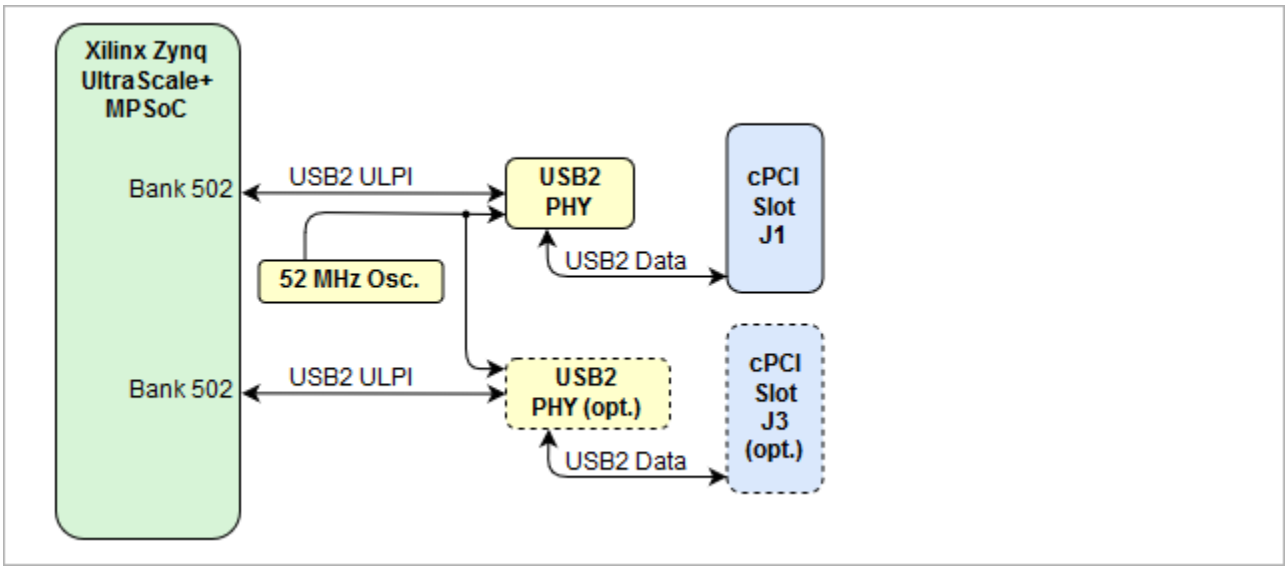
The EEPROMs U63 and U64 are programmable via the onboard I²C bus connected to MIO 20...21 pins. The I²C address is shown in the table below.

I2C address	Chip	Description
0x50	U63 24AA128T-I/ST	128K Serial EEPROM
0x53	U64 24AA025E48T-I/OT	2K Serial EEPROM with EUI-48™ or EUI-64™ Node Identity

EEPROMs I²C Addresses

USB2 PHY

USB2 PHY U11 is provided by USB3320 from Microchip. The ULPI interface is connected to the Zynq Ultrascale+ PS USB0. I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 52.000000 MHz oscillator U12. There is also the option to equip the TEC0850 board with a second USB2 PHY U13 connected to the optional cPCI backplane connector J3. Both, the optional USB2 PHY U13 and cPCI connector J3 are not fitted by default.



TEC0850 cPCI USB2 interface

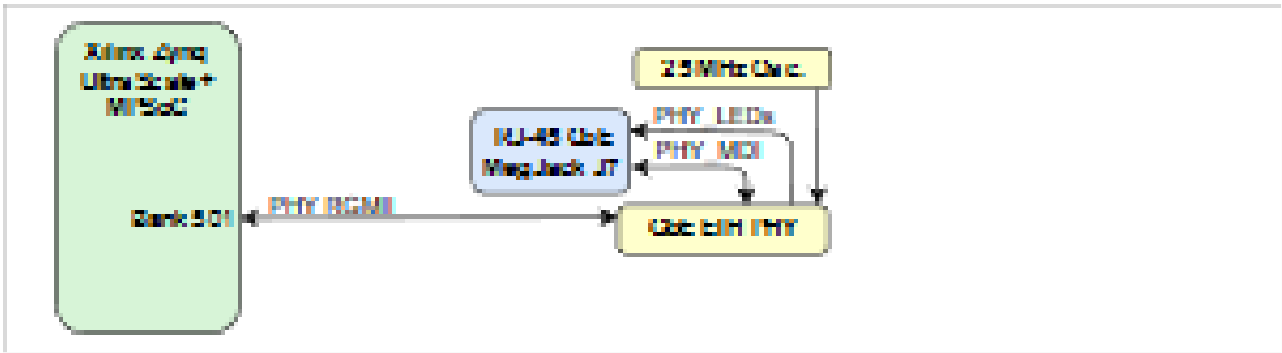
USB2 PHY U11 Pin	Connected to	Notes
ULPI	PS bank MIO52 ... MIO63	Zynq Ultrascale+ USB0 MIO pins are connected to the PHY
REFCLK	-	52MHz from onboard oscillator U12
REFSEL[0..2]	-	All pins set to GND selects the external reference clock frequency (52.000000 MHz)
RESETB	Zynq MPSoC MIO16, pin AM16	Low active USB2 PHY Reset
DP, DM	cPCI connector J1	USB2 data lane
CPEN	-	External USB power switch active-high enable signal
VBUS	5V	Connected to onboard 5V voltage level via a series of resistors, see schematic
ID	3.3V	USB2 OTG A-Device (host)

optional USB2 PHY U13 Pin	Connected to	Notes
ULPI	PS bank MIO64 ... MIO75	Zynq Ultrascale+ USB1 MIO pins are connected to the PHY
REFCLK	-	52MHz from onboard oscillator U12
REFSEL[0..2]	-	All pins set to GND selects the external reference clock frequency (52.000000 MHz)
RESETB	Zynq MPSoC MIO17, pin AP16	Low active USB2 PHY Reset
DP, DM	optional cPCI connector J3	USB2 data lane
CPEN	-	External USB power switch active-high enable signal
VBUS	5V	Connected to onboard 5V voltage level via a series of resistors, see schematic
ID	3.3V	USB2 OTG A-Device (host)

USB2 ULPI interface description

Gigabit Ethernet PHY

Onboard Gigabit Ethernet PHY U20 is provided with Marvell Alaska 88E1512, which use MDIO address 1. The Ethernet PHY RGMII interface is connected to the Zynq Ultrascale+ Ethernet0 PS GEM3. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from the on-board 25.000000 MHz oscillator U21.



TEC0850 GbE interface with RJ-45 MegJack

8bit DACs

The TEC0850 Board has 4 8-bit parallel Texas Instruments THS5641AIPW digital to analog converter (DAC) with up to 100 MSPS update rate connected to TI THS4631D operational amplifiers. See Schematic circuitry and TI THS5641 data sheet for proper operation of the on-board DAC units.

DAC unit	Signal Schematic Name	Connected to	Functionality
DAC1	DAC1_D0	PL HD bank 50, pin D11	Digital input bits D[7:0]
U28	DAC1_D1	PL HD bank 50, pin D10	
	DAC1_D2	PL HD bank 50, pin G11	D7 is the most significant data bit (MSB), D0 is the least significant data bit (LSB).
	DAC1_D3	PL HD bank 50, pin J11	
	DAC1_D4	PL HD bank 50, pin G10	
	DAC1_D5	PL HD bank 50, pin H10	
	DAC1_D6	PL HD bank 50, pin J10	
	DAC1_D7	PL HD bank 50, pin E10	

	DAC1_CLK	PL HD bank 50, pin F12	External clock input, input data latched on rising edge of the clock.
	DAC1_MODE	PL HD bank 50, pin F10	Input code format (binary, twos complement)
	EN_DAC1	SC FPGA U18 bank 8, pinE6	generate 3.3V voltages LDO U35, U34
DAC2 U31	DAC2_D0	PL HD bank 50, pin G15	Digital input bits D[7:0] D7 is the most significant data bit (MSB), D0 is the least significant data bit (LSB).
	DAC2_D1	PL HD bank 50, pin H14	
	DAC2_D2	PL HD bank 50, pin J14	
	DAC2_D3	PL HD bank 50, pin G14	
	DAC2_D4	PL HD bank 50, pin G13	
	DAC2_D5	PL HD bank 50, pin H13	
	DAC2_D6	PL HD bank 50, pin H12	
	DAC2_D7	PL HD bank 50, pin J12	
	DAC2_CLK	PL HD bank 50, pin F12	External clock input, input data latched on rising edge of the clock.
	DAC2_MODE	PL HD bank 50, pin F11	Input code format (binary, twos complement)
	EN_DAC2	SC FPGA U18 bank 8, pin E8	generate 3.3V voltages LDO U32, U60
DAC3 U29	DAC3_D0	PL HD bank 44, pin AG14	Digital input bits D[7:0] D7 is the most significant data bit (MSB), D0 is the least significant data bit (LSB).
	DAC3_D1	PL HD bank 44, pin AE13	
	DAC3_D2	PL HD bank 44, pin AG13	
	DAC3_D3	PL HD bank 44, pin AJ15	
	DAC3_D4	PL HD bank 44, pin AJ14	
	DAC3_D5	PL HD bank 44, pin AH14	
	DAC3_D6	PL HD bank 44, pin AL13	
	DAC3_D7	PL HD bank 44, pin AM13	
	DAC3_CLK	PL HD bank 44, pin AK15	External clock input, input data latched on rising edge of the clock.
	DAC3_MODE	PL HD bank 44, pin AK14	Input code format (binary, twos complement)
	EN_DAC3	SC FPGA U18 bank 8, pin B6	generate 3.3V voltages LDO U66, U68
DAC4 U33	DAC4_D0	PL HD bank 44, pin AP14	Digital input bits D[7:0] D7 is the most significant data bit (MSB), D0 is the least significant data bit (LSB).
	DAC4_D1	PL HD bank 44, pin AN14	
	DAC4_D2	PL HD bank 44, pin AM14	
	DAC4_D3	PL HD bank 44, pin AN13	
	DAC4_D4	PL HD bank 44, pin AP12	
	DAC4_D5	PL HD bank 44, pin AN12	
	DAC4_D6	PL HD bank 44, pin AF13	
	DAC4_D7	PL HD bank 44, pin AH13	
	DAC4_CLK	PL HD bank 44, pin AK13	External clock input, input data latched on rising edge of the clock.
	DAC4_MODE	PL HD bank 44, pin AK13	Input code format (binary, twos complement)
	EN_DAC4	SC FPGA U18 bank 8, pin A6	generate 3.3V voltages LDO U70, U72

DAC units interface description

DIP-Switches

There are two 4-bit DIP-witches S3 and S4 present on the TEC0850 board to configure options and set parameters. The following section describes the functionalities of the particular switches.

The table below describes the functionalities of the switches of DIP-switches S1 and S2 at their every position:

DIP-switch S1	Signal Schematic Name	Connected to	Functionality	Notes
S1-1	JTAGEN	SC FPGA U18, bank 1B, pin E5	Positions: OFF: SC FPGA's JTAG enabled ON: Zynq MPSoC's JTAG enabled	to switch the JTAG interface between SC FPGA and Zynq MPSoC
S1-2	WP	EEPROM U63, pin 7	Positions: OFF: Write Protect is enabled ON: Write Protect is disabled	-
S1-3	PUDC_B	Zynq MPSOC PS Config Bank 503, pin AD15	Positions: ON: PUDC_B is Low OFF: PUDC_B is HIGH	Internal pull-up resistors during configuration are enabled at ON-position, means I/O's are 3-stated until the configuration of the FPGA completes.
S1-4	SW4	SC FPGA U18, bank 8, pin A5	SC Switch (Reserved for future use)	low active logic
DIP-switch S2	**Signal Schematic Name**	**Connected to**	**Functionality**	**Notes**
S2-1	MODE3	Zynq MPSOC PS Config Bank 503, pin R23	set 4-bit code for boot mode selection	See Zynq UltraScale+ Device Technical Reference Manual page 236 for full boot modes description Set DIP-switches as bit pattern of S2
S2-2	MODE2	Zynq MPSOC PS Config Bank 503, pin T23		
S2-3	MODE1	Zynq MPSOC PS Config Bank 503, pin R22		
S2-4	MODE0	Zynq MPSOC PS Config Bank 503, pin T22		

BOOT Mode	1	2	3	4
Quad-SPI (32b	ON	ON	OFF	ON
SD1 (2.0)	ON	OFF	ON	OFF
JTAG	ON	ON	ON	ON

TEC0850 DIP-switches description

Buttons

There is one switch button available to the user connected to the SC FPGA U18:

Button	Signal Schematic Name	Connected to	Notes
S3	USR_BTN	SC FPGA U18, bank 5, pin J10	low active logic Refer documentation of the firmware of SC FPGA U18.

On-board Push-Button

LEDs

The TEC0850 board is equipped with several LEDs to signal current states and activities.

LED	Color	Connected to	Description and Notes
Front panel LED D1	Red	Zynq MPSoC PL bank 11, pin AF15	PL User defined LED
Front panel LED D2	Green	Zynq MPSoC PL bank 11, pin AG15	PL User defined LED
Front panel LED D3	Green	Zynq MPSoC PL bank 11, pin AE15	PL User defined LED
Front panel LED D4	Green	SC FPGA U18 bank 3, pin M4	Power Good

On-board LEDs description

Power and Power-On Sequence

Power Consumption

The maximum power consumption of a module mainly depends on the design running on the FPGA.

Xilinx provides a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input	Typical Current
VIN_12V	TBD*

Typical power consumption

Power supply with a minimum current capability of 5A (60W@12V, CompactPCI Serial spec.) for system startup is recommended.

The TEC0850 board is equipped with the Xilinx Zynq UltraScale+ MPSoC delivers a heterogeneous multi-processing system with integrated programmable logic and independently operable elements and is designed to meet an embedded system power management requirement by advanced power management features. These features allow offsetting the power and heat constraints against overall performance and operational efficiency.

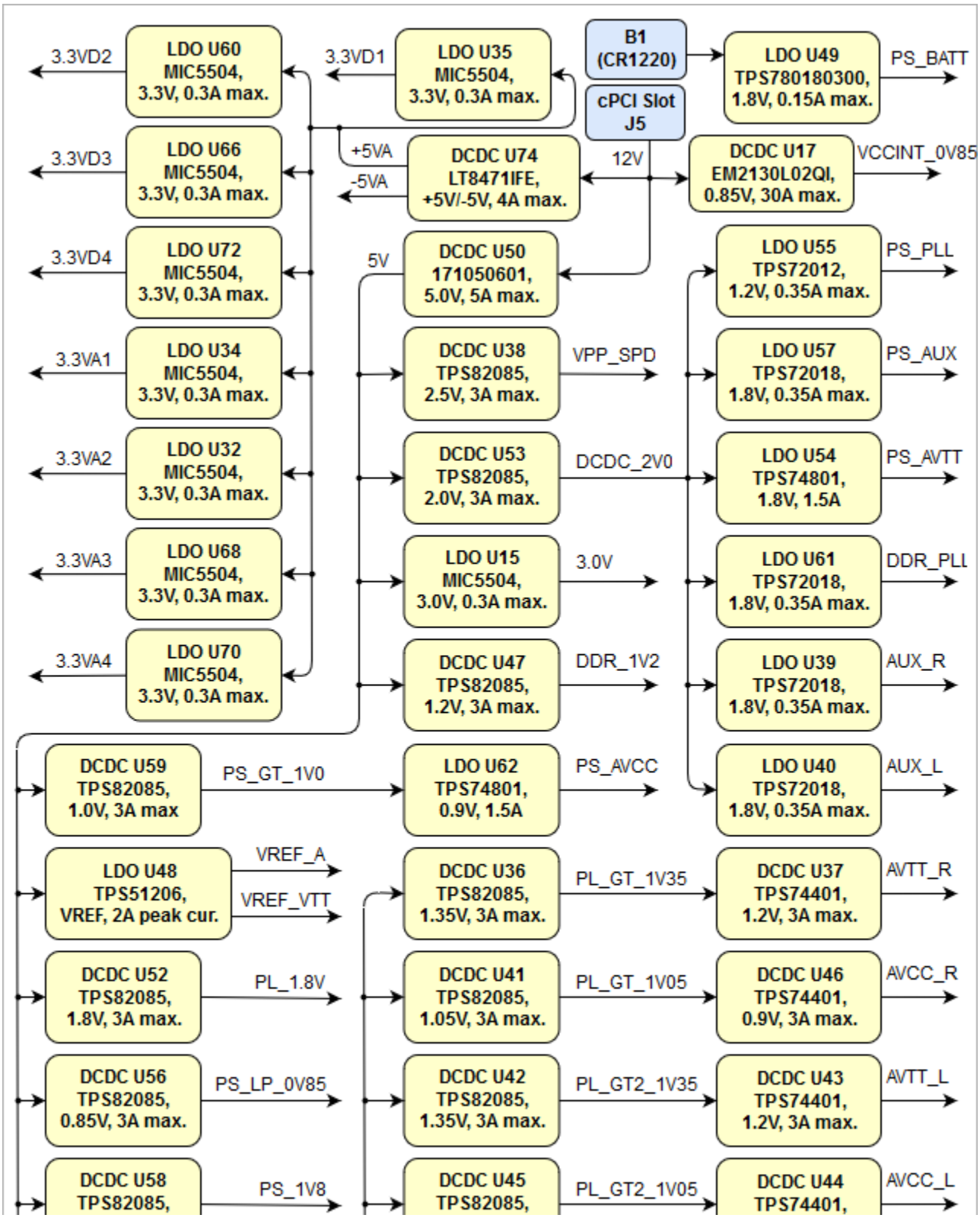
This features allowing highly flexible power management are achieved by establishing Power Domains for power isolation. The Zynq UltraScale+ MPSoC has multiple power domains, whereby each power domain requires its own particular on-board DC-DC converters.

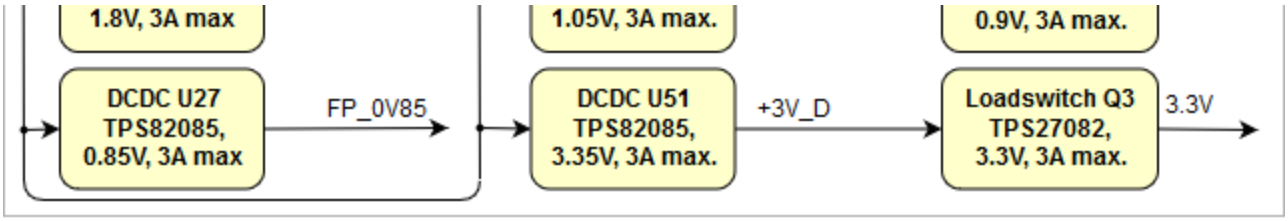
The Processing System contains three Power Domains:

- Battery Power Domain (BBRAM and RTC)
- Full-Power Domain (Application Processing Unit, DDR Controller, Graphics Processing Unit and High-Speed Connectivity)
- Low-Power Domain (Real-Time Processing Unit, Security and Configuration Unit, Platform Management Unit, System Monitor and General Connectivity)
- Programmable Logic (PL)

Power Distribution Dependencies

There are following dependencies how the initial 24V voltage from the main power pins on cPCI slot J1 is distributed to the onboard DC-DC converters, which power up further DC-DC converters and the particular on-board voltages:


B1
(CR1220)
cPCI Slot
J5
LDO U60
MIC5504,
3.3V, 0.3A max.
3.3VD2
LDO U35
MIC5504,
3.3V, 0.3A max.
3.3VD1
LDO U49
TPS780180300,
1.8V, 0.15A max.
PS_BATT
LDO U66
MIC5504,
3.3V, 0.3A max.
3.3VD3
+5VA
-5VA
DCDC U74
LT8471IFE,
+5V/-5V, 4A max.
12V
DCDC U17
EM2130L02QI,
0.85V, 30A max.
VCCINT_0V85
LDO U72
MIC5504,
3.3V, 0.3A max.
3.3VD4
5V
DCDC U50
171050601,
5.0V, 5A max.
LDO U55
TPS72012,
1.2V, 0.35A max.
PS_PLL
LDO U34
MIC5504,
3.3V, 0.3A max.
3.3VA1
DCDC U38
TPS82085,
2.5V, 3A max.
VPP_SPD
LDO U57
TPS72018,
1.8V, 0.35A max.
PS_AUX
LDO U32
MIC5504,
3.3V, 0.3A max.
3.3VA2
DCDC U53
TPS82085,
2.0V, 3A max.
DCDC_2V0
LDO U54
TPS74801,
1.8V, 1.5A
PS_AVTT
LDO U68
MIC5504,
3.3V, 0.3A max.
3.3VA3
LDO U15
MIC5504,
3.0V, 0.3A max.
3.0V
LDO U61
TPS72018,
1.8V, 0.35A max.
DDR_PLL
LDO U70
MIC5504,
3.3V, 0.3A max.
3.3VA4
DCDC U47
TPS82085,
1.2V, 3A max.
DDR_1V2
LDO U39
TPS72018,
1.8V, 0.35A max.
AUX_R
DCDC U59
TPS82085,
1.0V, 3A max
PS_GT_1V0
LDO U62
TPS74801,
0.9V, 1.5A
PS_AVCC
LDO U40
TPS72018,
1.8V, 0.35A max.
AUX_L
LDO U48
TPS51206,
VREF, 2A peak cur.
VREF_A
VREF_VTT
DCDC U36
TPS82085,
1.35V, 3A max.
PL_GT_1V35
DCDC U37
TPS74401,
1.2V, 3A max.
AVTT_R
DCDC U52
TPS82085,
1.8V, 3A max.
PL_1.8V
DCDC U41
TPS82085,
1.05V, 3A max.
PL_GT_1V05
DCDC U46
TPS74401,
0.9V, 3A max.
AVCC_R
DCDC U56
TPS82085,
0.85V, 3A max.
PS_LP_0V85
DCDC U42
TPS82085,
1.35V, 3A max.
PL_GT2_1V35
DCDC U43
TPS74401,
1.2V, 3A max.
AVTT_L
DCDC U58
TPS82085,
PS_1V8
DCDC U45
TPS82085,
PL_GT2_1V05
DCDC U44
TPS74401,
AVCC_L



Power Distribution

Power-On Sequence

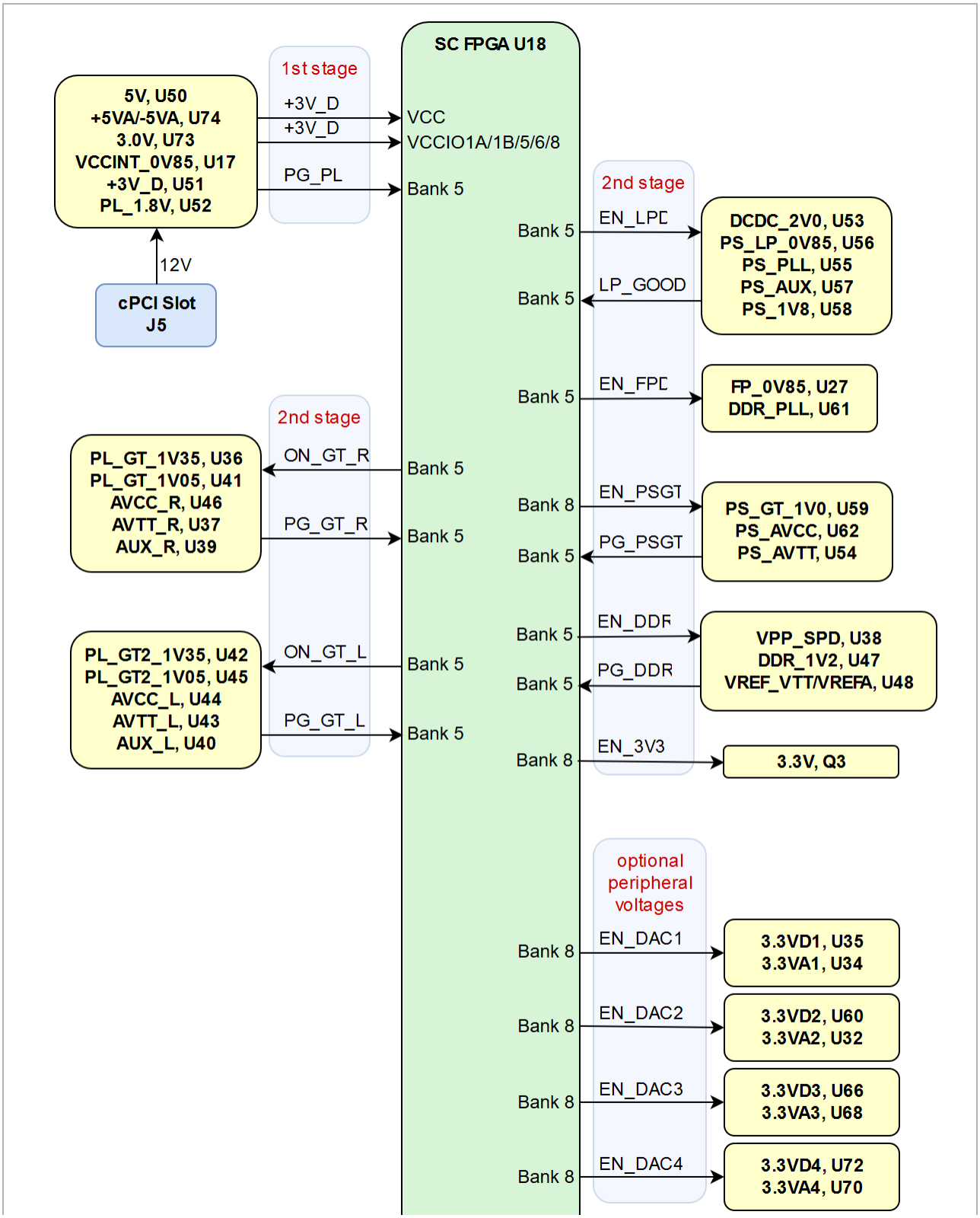
The TEC0850 board meets the recommended criteria to power up the Xilinx Zynq UltraScale+ MPSoC properly by keeping a specific sequence of enabling the onboard DC-DC converters dedicated to the particular Power Domains and powering up the onboard voltages.

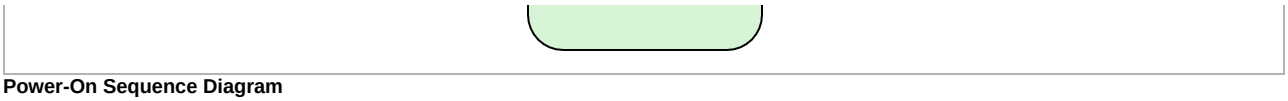
On the TEB0911 UltraRack board following Power Domains will be powered up in a certain sequence with by enable and power-good signals of the DC-DC converters, which are controlled by the System Controller FPGA U18:

1. Main Power and Programmable Logic (PL)
2. Low-Power Domain (LPD)
3. Full-Power Domain (FPD)
4. GTH, PS GTR transceiver and DDR memory
5. Optional DAC voltages

Hence, those three power instances will be powered up consecutively when the Power-Good signals of the previous instance are asserted.

Following diagram describes the sequence of enabling the three power instances utilizing the DC-DC converter control signals (Enable, Power-Good), which will power-up in descending order as listed in the blocks of the diagram.


SC FPGA U18
1st stage
5V, U50
+5VA/-5VA, U74
3.0V, U73
VCCINT_0V85, U17
+3V_D, U51
PL_1.8V, U52
12V
cPCI Slot
J5
+3V_D
+3V_D
PG_PL
VCC
VCCIO1A/1B/5/6/8
Bank 5
2nd stage
EN_LPD
LP_GOOD
DCDC_2V0, U53
PS_LP_0V85, U56
PS_PLL, U55
PS_AUX, U57
PS_1V8, U58
EN_FPD
FP_0V85, U27
DDR_PLL, U61
2nd stage
ON_GT_R
PG_GT_R
PL_GT_1V35, U36
PL_GT_1V05, U41
AVCC_R, U46
AVTT_R, U37
AUX_R, U39
EN_PSGT
PG_PSGT
PS_GT_1V0, U59
PS_AVCC, U62
PS_AVTT, U54
EN_DDR
PG_DDR
VPP_SPD, U38
DDR_1V2, U47
VREF_VTT/VREFA, U48
ON_GT_L
PG_GT_L
PL_GT2_1V35, U42
PL_GT2_1V05, U45
AVCC_L, U44
AVTT_L, U43
AUX_L, U40
EN_3V3
3.3V, Q3
optional peripheral voltages
EN_DAC1
3.3VD1, U35
3.3VA1, U34
EN_DAC2
3.3VD2, U60
3.3VA2, U32
EN_DAC3
3.3VD3, U66
3.3VA3, U68
EN_DAC4
3.3VD4, U72
3.3VA4, U70



Power-On Sequence Diagram

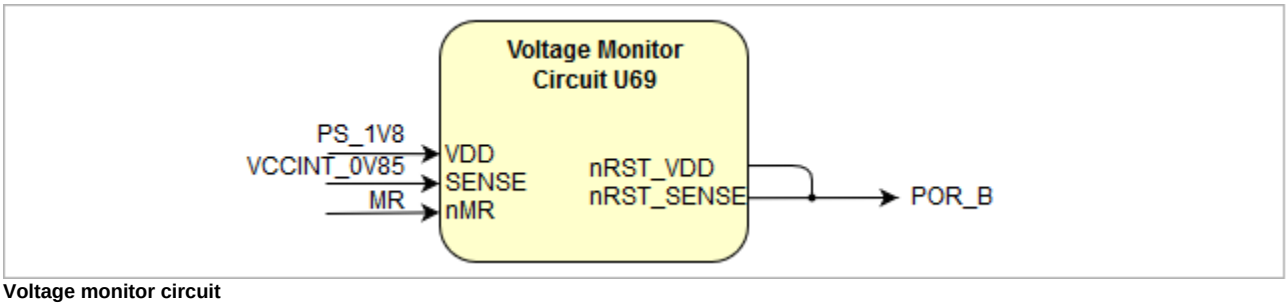
> To avoid any damage to the MPSoC module, check for stabilized onboard voltages in a steady state before powering up the MPSoC's I/O bank voltages VCCOx. All I/Os should be tri-stated during the power-on sequence.

It is important that all PS and PL I/Os are tri-stated at power-on until the "Power Good"-signals are high, meaning that all onboard voltages have become stable and the module is properly powered up.

See Xilinx datasheet DS925 for additional information.

Voltage Monitor Circuit

The voltages PS_1V8 and VCCINT_0V85 are monitored by the voltage monitor circuit U69, which generates the POR_B reset signal at power-on. A manual reset is also possible by driving the low active MR-pin connected to MAX10 FPGA U18 (bank5, pin K10) to GND.



Voltage monitor circuit

Power Rails

Connector / Pin	Voltage	Direction	Notes
J1, pin A1, D1, E1, G1, H1, J1, K1	VIN_12V	Input	Main power supply pins
J17, pin 2	12V	Output	4-wire PWM fan connector supply voltage
J13, pin 4	+3V_D	Output	JTAG/UART reference VCCIO voltage
B1, pin +	VBATT	Input	3.0V CR1220 battery
J16, pin 2	5V	Output	I/O header VCCIO
J16, pin 1	3.3V	Output	I/O header VCCIO
J9, pin 4	VBUS	Input	USB2 VBUS (5.0V nominal)
J10, pin A4, B9	VBUS30	Input	USB3 VBUS (5.0V nominal)
J11, pin 4	3.3V	Output	MicroSD Card VDD
J15, pin 2	DAC1_OUT	Output	DAC output
J15, pin 3	DAC2_OUT	Output	DAC output
J15, pin 4	DAC3_OUT	Output	DAC output
J15, pin 5	DAC4_OUT	Output	DAC output

TEC0850 power rails description

Bank Voltages

Zynq MPSoC Bank	Type	Schematic Name	Voltage	Voltage Range
44	HD	3.3V	3.3V	fixed to 3.3V
47	HD	3.3V	3.3V	fixed to 3.3V
48	HD	3.3V	3.3V	fixed to 3.3V
49	HD	3.3V	3.3V	fixed to 3.3V
50	HD	3.3V	3.3V	fixed to 3.3V
64	HP	PL_1V8	1.8V	fixed to 1.8V
65	HP	PL_1V8	1.8V	fixed to 1.8V
66	HP	PL_1V8	1.8V	fixed to 1.8V
67	HP	PL_1V8	1.8V	fixed to 1.8V
500	MIO	PS_1V8	1.8V	fixed to 1.8V
501	MIO	PS_1V8	1.8V	fixed to 1.8V
502	MIO	PS_1V8	1.8V	fixed to 1.8V
503	CONFIG	PS_1V8	1.8V	fixed to 1.8V
504	PSDDR	DDR_1V2 DDR_PLL	1.2V 1.8V	fixed bank voltages
128	GTH	AVCC_L	0.9V	fixed bank voltages
129		AUX_L	1.8V	
130		AVTT_L	1.2V	
228	GTH	AVCC_R	0.9V	fixed bank voltages
229		AUX_R	1.8V	
230		AVTT_R	1.2V	
MAX10 FPGA Bank	**Type**	**Schematic Name**	**Voltage**	**Voltage Range**
1A	-	+3V_D	3.3V	fixed to 3.3V
1B	-	+3V_D	3.3V	fixed to 3.3V
2	-	PS_1V8	1.8V	fixed to 1.8V
3	-	3.3V	3.3V	fixed to 3.3V
5	-	+3V_D	3.3V	fixed to 3.3V
6	-	+3V_D	3.3V	fixed to 3.3V
8	-	+3V_D	3.3V	fixed to 3.3V

TEC0850 Zynq MPSoC and SC FPGA bank voltages

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Unit	Reference Document	Notes
VIN_12V	-0.3	16	V	Intel Enpirion EM2130 data sheet / Fuse F1	Fuse F1 @16V/2.5A
VBATT	-0.3	6	V	TPS780180300 data sheet	1.8V typical output

VCCO for HD I/O banks	-0.5	3.4	V	Xilinx document DS925	-
VCCO for HP I/O banks	-0.5	2	V	Xilinx document DS925	-
I/O input voltage for HD I/O banks	-0.55	VCCO + 0.55	V	Xilinx document DS925	-
I/O input voltage for HP I/O banks	-0.55	VCCO + 0.55	V	Xilinx document DS925	-
PS I/O input voltage (MIO pins)	-0.5	VCCO_PSIO + 0.55	V	Xilinx document DS925	VCCO_PSIO 1.8V nominally
PS GTR reference clocks absolute input voltage	-0.5	1.1	V	Xilinx document DS925	-
PS GTR absolute input voltage	-0.5	1.1	V	Xilinx document DS925	-
MGT clock absolute input voltage	-0.5	1.3	V	Xilinx document DS925	-
MGT Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	-0.5	1.2	V	Xilinx document DS925	-
SC FPGA U18 I/O input voltage	-0.5	VCC + 0.5	V	Intel MAX 10 data sheet	VCC 3.3V nominally
A voltage on input I/O pins of DC-DC U17 EM2130 on header J12	-0.3	3.6	V	Intel Enpirion EM2130 datasheet	-
Storage temperature (ambient)	-40	85	°C	ASVTX-12 datasheet	-

Module absolute maximum ratings

Recommended Operating Conditions

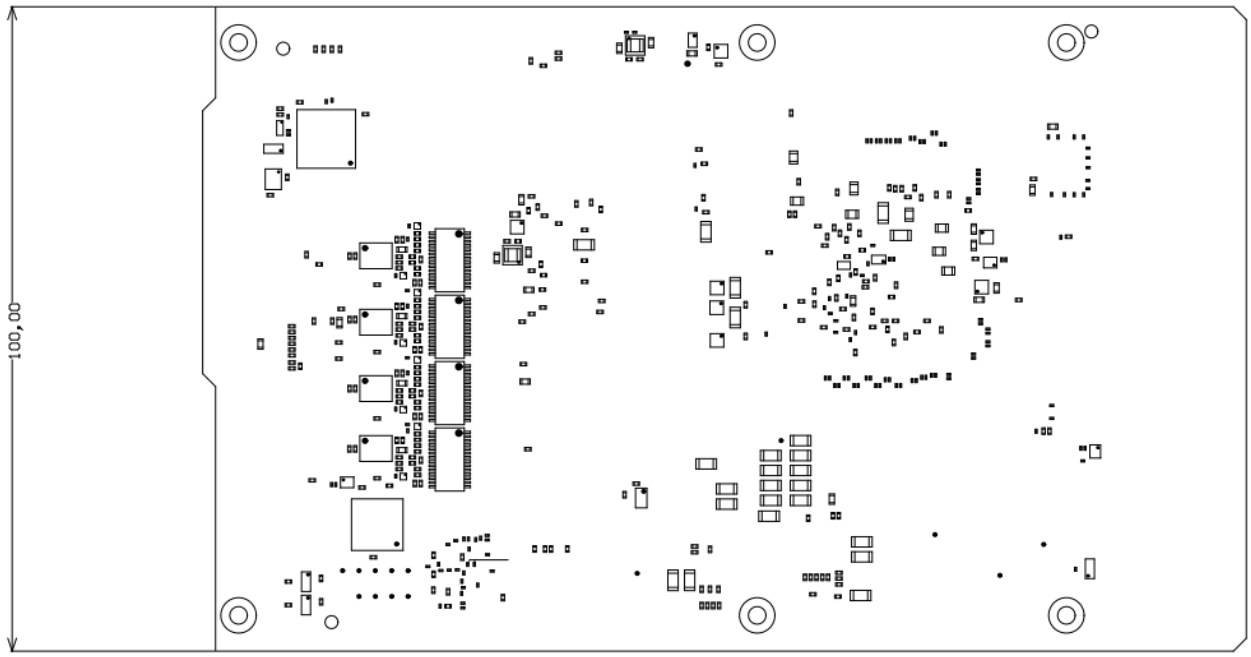
Parameter	Min	Max	Unit	Reference Document	Notes
VIN_12V	12	14	V	Intel Enpirion EM2130 datasheet	12V nominally input voltage
VBATT	2.2	5.5	V	TPS780180300 data sheet	supplied by 3.0V CR1220 battery
VCCO for HD I/O banks	1.14	3.4	V	Xilinx document DS925	-
VCCO for HP I/O banks	0.95	1.9	V	Xilinx document DS925	-
I/O input voltage for HD I/O banks	-0.2	VCCO + 0.2	V	Xilinx document DS925	-
I/O input voltage for HP I/O banks	-0.2	VCCO + 0.2	V	Xilinx document DS925	-
PS I/O input voltage (MIO pins)	-0.2	VCCO_PSIO + 0.2	V	Xilinx document DS925	VCCO_PSIO 1.8V nominally
SC FPGA U18 I/O input voltage	0	VCC	V	Intel MAX 10 data sheet	VCC 3.3V nominally
Board Operating Temperature Range [1), 2)]	0	85	°C	Xilinx document DS925	extended grade Zynq MPSoC temperature range

Module absolute maximum ratings

1) Temperature range may vary depending on assembly options

2) The operating temperature range of the Zynq MPSoC, SC FPGA SoC and onboard peripherals are a junction and also ambient operating temperature ranges

Physical Dimensions



Physical dimensions drawing

Variants Currently In Production

Trenz shop TE0xxx overview page	
English page	German page

Shop Overview

Revision History

Hardware Revision History

Date	Revision	PCN	Documentation Link	Notes
-	02	-	TEC0850-02	current available board revision
-	01	-	-	Prototypes

Module hardware revision history

Document Change History

Date	Revision	Constributor	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• boot mode bugfix
2018-10-26	v.103	John Hartfiel	• change" Compact PCI" to "Compact PCI Serial"
26 Sept 2018	v.102	Ali Naseri	• small corrections
25 Sept 2018	v.101	John Hartfiel	• style changes

20 Sept 2018	v.97	Ali Naseri	• added information about the optional second USB2 PHY and cPCI connector J2 (not fitted by default)
19 Sept 2018	v.94	John Hartfiel	• small style changes and typo correction
18 Sept 2018	v.93	Ali Naseri , Oleksandr Kiyenko , John Hartfiel	• initial release

--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• --

Document change history

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