TE0741 CPLD

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Overview

Firmware for PCB CPLD with designator U7. CPLD Device in Chain: LCMX02-256HC

Feature Summary

- Power Monitoring
- Reset
- LED
- JTAG routing

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Pullup/Down	Bank Power	Description
C_LED	out	17	none	3.3V	Green LED D4, blinking pattern according to different states
DONE	in	28	up	3.3V	FPGA Done signal, also connected to green LED D3. Is OFF when FPGA configured.
F_TCK / C_TCK	out	9	none	3.3V	FPGA JTAG
F_TDI / C_TDI	out	21	none	3.3V	FPGA JTAG
F_TDO / C_TDO	in	5	none	3.3V	FPGA JTAG
F_TMS / C_TMS	out	4	none	3.3V	FPGA JTAG
GND		10		3.3V	GND
GND		11		3.3V	GND
GND		12		3.3V	GND
GND		13		3.3V	GND
GND		14		3.3V	connected to GND
JTAGMODE		26		3.3V	Enable JTAG access to CPLD for Firmware update (LOW-'0' : JTAG signales routed to module, HIGH-'1' : CPLD access)

MODE	in	16		3.3V	/ currently_not_used
PG_ALL	in	27	up	3.3V	Power sense from 1V/1.8V/3.3V/3.3VIN
PGOOD	inout	25	up	3.3V	Power Good. Low, if power failed, internal pullup activated
PROG_B	out	23	none	3.3V	FPGA Prog_B
RESIN	in	8	up	3.3V	external reset from B2B
TCK / M_TCK	in	30	none	3.3V	B2B JTAG
TDI / M_TDI	in	32	up	3.3V	B2B JTAG
TDO / M_TDO	out	1	none	3.3V	B2B JTAG
TMS / M_TMS	in	29	up	3.3V	B2B JTAG
XIO	in	20	none	3.3V	FPGA IO from Bank14 H26, Can be used to control LED D4 if no error state occurs

Functional Description

JTAG

JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA can be multiplexed via JTAGEN (logical one for CPLD, logical zero for FPGA) on JM1-89.

Reset

PROG_B is triggered by RESIN or PG_ALL.

Power

PG_ALL is used to trigger PROG_B Reset in case of power failure. This case is also indicated by the green LED D4.

PGOOD is set low, if PG_ALL failed otherwise high impedance. Internal pullup is activated.

PGOOD can be drive to low from carrier, this will be indicated by LED subsequency only.

LED

LED D4 Green			
Status	**Blink Sequence**	**Priority**	**Comment**
Reset	******** ~3Hz	1	external Reset is set
Power failed	*****ooo	2	PG_ALL Problem (1.8V or 3.3V)
PGOOD Low	****oooo	3	PGOOD is set low from carrier or the power monitor U11 noticed a power failure
DONE	*ooooooo	4	Module not programmed

idle	OFF	5	Module ready and programmed. In this case LED D4 can be controlled by FPGA - XIO Signal

Appx. A: Change History and Legal Notices

Revision Changes

CPLD REV2 to REV03

- added JTAG DELAY and Pullmode constraints
- XIO can be used to control LED D4

CPLD REV01 to REV02

- add PGOOD functionality
- new LED status sequence

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description	Firmware release
Error r **ge-info'** Ambigu	**Error rendering macro 'page-info'** ding for method jdk.proxy279.$Proxy4022#h Ambiguous method overloading for method jdk.pr	REV03	REV02 - REV05	**Error rendering macro 'page-info'** mission. Cannot resolve which method to invoke for [null, class java.lang.String, class Ambiguous method overloading for method jdk.proxy279.$Proxy4022#invokeContentLevelRe	• Update Document Style	
2023-12-13	v.7	REV03	REV02 - REV05	Waldemar Hanemann	• Revision 03	2023-12-13 SC-PGM-(TE0741-005_SC0741-003_20231213.zip)
2018-08-29	v.4	REV02	REV02,REV03	John Hartfiel	• Revision 02 released	2018-08-29 (SC-PGM-TE0741-0203_SC0741-02_20180829.zip)
2028-03-08	v.2	REV01	REV02,REV03	John Hartfiel	• Revision 01	2014-07-02

	All			**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPe		

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