TEI0010 TRM

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Overview

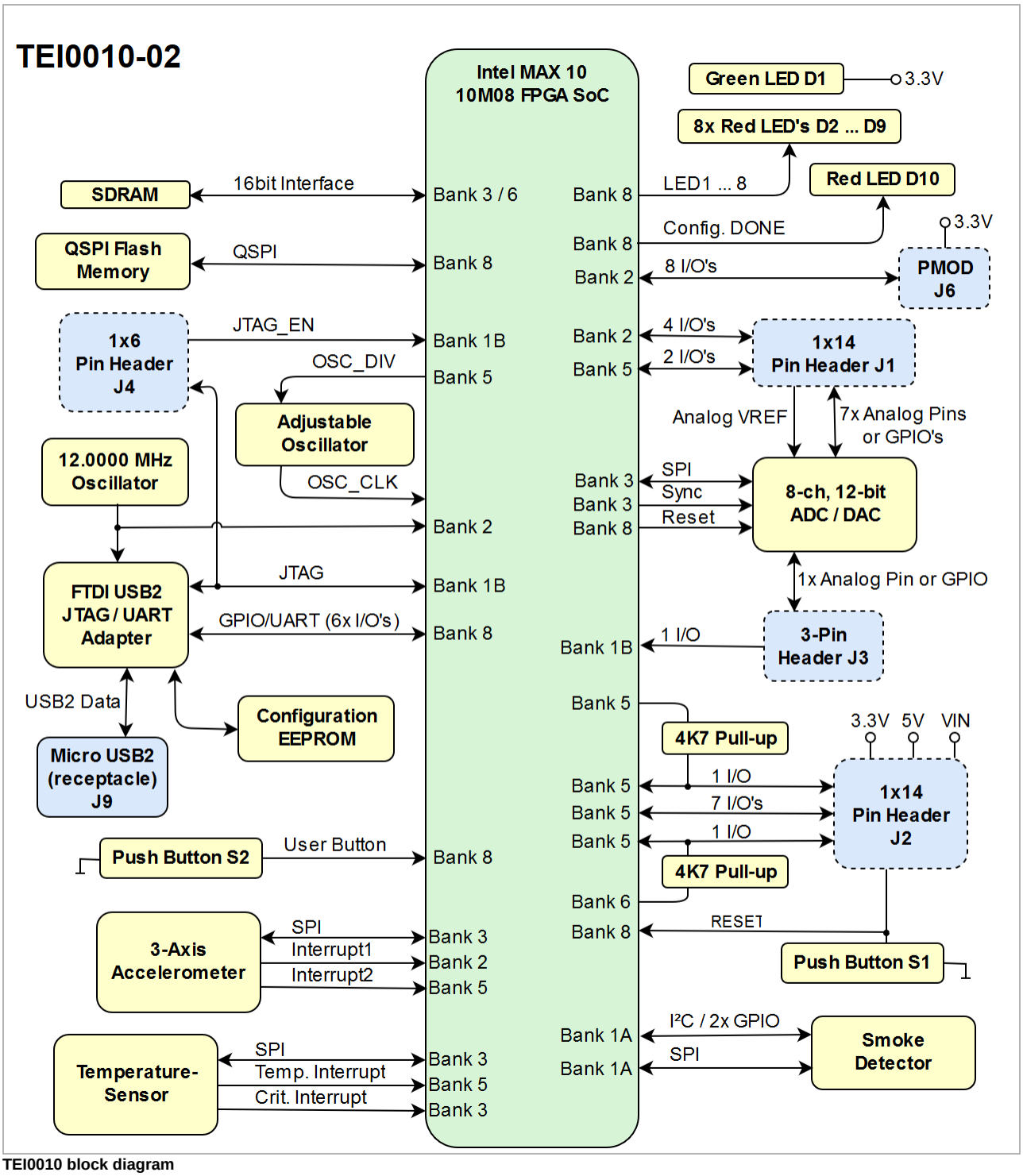
The Trenz Electronic TEI0010 AnalogMax is a low cost small-sized FPGA module integrating an Intel MAX 10 FPGA SoC, 8 MByte serial memory for configuration and operation and 8 MByte SDRAM. The board is equipped with several sensors for analog values like a 3-axis accelerometer, temperature sensor, smoke detector and a 8-channel 12bit ADC/DAC.

Refer to http://trenz.org/analogmax-info for the current online version of this manual and other available documentation.

Key Features

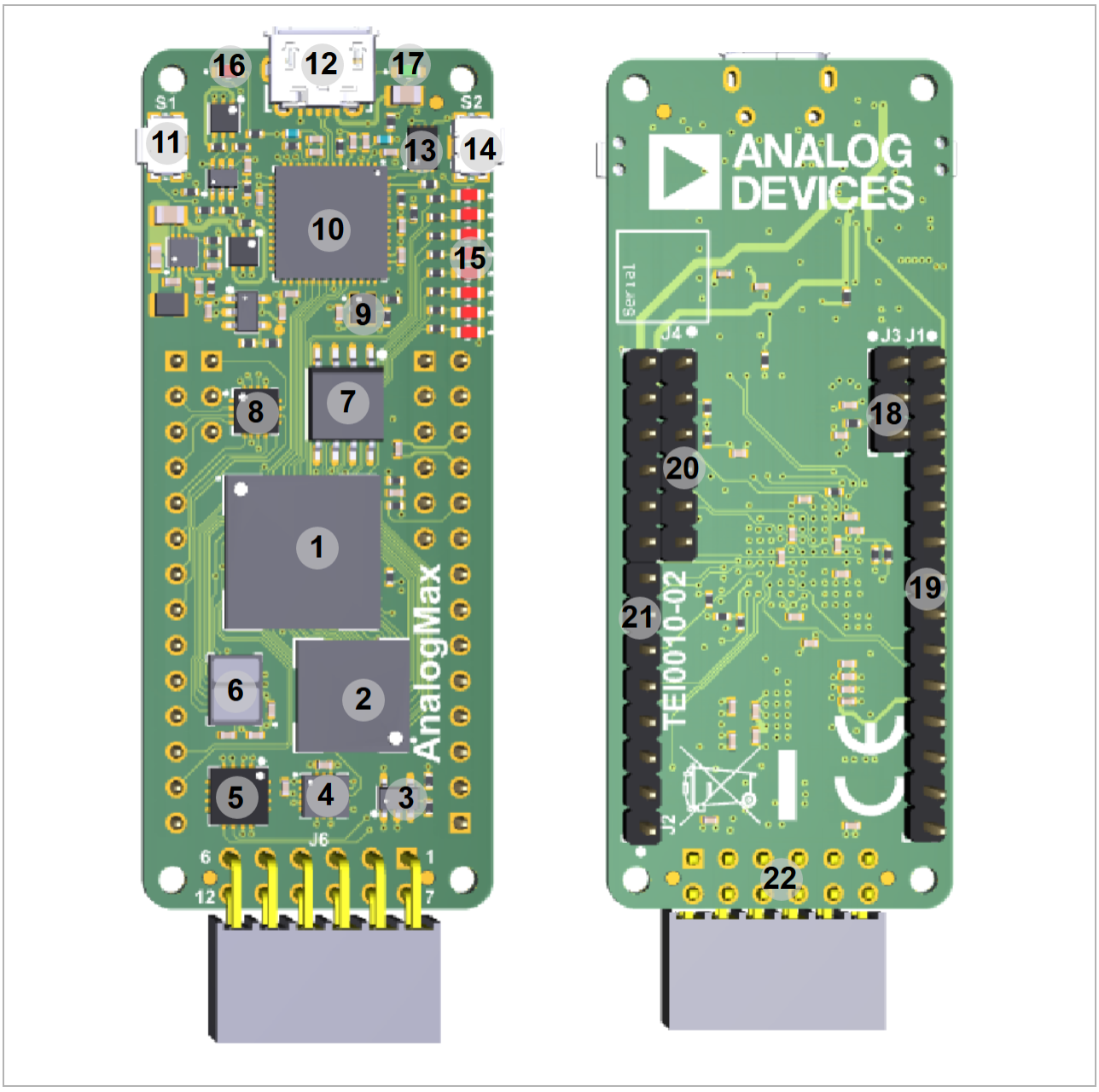
- Intel MAX 10 10M08 FPGA SoC
- 8 MByte SDRAM
- 8 MByte QSPI Flash memory
- Onboard oscillator with 3 selectable frequencies
- Analog Devices ADXL362 MEMS 3-axis accelerometer
- Analog Devices ADT7320 temperature sensor
- Analog Devices ADPD188BI smoke detector
- Analog Devices AD5592R ADC/DAC
- JTAG and UART over Micro USB2 connector
- 1x6 pin header for JTAG access to FPGA SoC
- 1x PMOD header providing 8 I/O
- 2x 14-pin headers (2,54 mm pitch) providing I/O with 7 analog inputs as alternative function
- 1x 3-pin header providing 2 analog inputs or 1 digital I/O
- 8x user LEDs
- 1x user push button
- 5.0V single power supply with on-board voltage regulators
- Size: 61.5 x 25 mm

Block Diagram



TEI0010 block diagram

Main Components



TEI0010 main components

1. Intel MAX 10 10M08 FPGA SoC, U1
2. 8 Mbyte SDRAM 166MHz, U2
3. LT LTC1799 oscillator, U10
4. Analog Devices ADXL362BCCZ MEMS 3-axis accelerometer, U11
5. Analog Devices ADT7320UCPZ temperature sensor, U8
6. Analog Devices ADPD188BI smoke detector, U14
7. Winbond W74M64FV QSPI Flash memory, U5
8. Analog Devices AD5592RBCPZ ADC/DAC, U12
9. 12.0000 MHz MEMS oscillator, U7

10. FTDI USB2 to JTAG/UART adapter, U3
11. Push button (reset), S1
12. Micro USB2 B socket (receptacle), J9
13. Configuration EEPROM for FTDI chip, U9
14. Push button (user), S2
15. 8x red user LEDs, D2 ... D9
16. Red LED (Conf. DONE), D10
17. Green LED (indicating 3.3V supply voltage), D1
18. 3-pin header (2.54mm pitch), J3
19. 1x14 pin header (2.54mm pitch), J1
20. 1x6 pin header (2.54mm pitch), J4
21. 1x14 pin header (2.54mm pitch), J2
22. 2x6 Pmod connector, J6

Initial Delivery State

Storage device name	Content	Notes
Quad SPI Flash, U5	Empty	-
FTDI chip configuration EEPROM, U9	Programmed	Arrow Blaster identification

Initial delivery state of programmable devices on the module

Control Signals

To get started with TEI0010 board, some basic signals are essential and are described in the following table:

Control signal	Switch / Button / LED / Pin	Signal Schematic Names	Connected to	Functionality	Notes
MAX10 FPGA U1 JTAGEN	header J4, pin 2	JTAGEN	MAX10 FPGA U1, bank 1B, pin E5	high or floating: MAX 10 JTAG enabled, low: MAX 10 JTAG disabled	switch the JTAG pins to user I/O if pin is driven low
MAX10 FPGA U1 Reset	header J2, pin 10	RESET	MAX10 FPGA U1, bank 8, pin E7	low active reset line	also connected to Reset push button S1
Supply voltage indicator	Green LED D1	3.3V	DC-DC converter U4	indicating 3.3V voltage level	-
Configuration DONE indicator	Red LED D10	CONF_DONE	MAX10 FPGA U1, bank 8, pin C5	indicating FPGA configuration completed	OFF: configuration completed, ON: FPGA not configured
Reset Push button	S1	RESET	MAX10 FPGA U1, bank 8, pin E7	low active logic	-
User Push button	S2	USER_BTN	MAX10 FPGA U1, bank 8, pin E6	low active logic	available to user

Control Signals

Boot Process

The FPGA configuration for Intel MAX 10 FPGAs can be stored through JTAG interface (using a POF file) on the FPGA itself since the Intel MAX 10 FPGA offers non-volatile memory on chip. The FPGA configuration is loaded from the MAX10 non-volatile CFM memory when the board is powered up.

To configure the FPGA directly, the JTAG interface can be used to configure the FPGA SRAM (using a SOF file), then the configuration is lost after power off.

Signals, Interfaces and Pins

I/Os on Pin Headers and Connectors

I/O signals of the FPGA SoC's I/O banks connected to the board's pin headers and connectors:

Bank	Connector Designator	I/O Signal Count	Bank Voltage	Notes
2	J1	4 I/O's	3.3V	-
	J6	8 I/O's		Pmod connector
5	J1	2 I/O's	3.3V	-
	J2	9 I/O's		2 I/O's of bank 5 can be pulled-up to 3.3V (4K7 resistors)
1B	J4	JTAG interface and 'JTAGEN' signal (5 I/O's)	3.3V	JTAG enable signal (JTAGEN) on pin J4-2, switch between user I/O pins and JTAG pin functions
	J3	1 I/O		-

General overview of single ended I/O's on board headers

JTAG Interface

Primary JTAG access to the FPGA SoC device U1 is provided through Micro USB2 B connector J9. The JTAG interface is created by the FTDI FT2232H USB2 to JTAG/UART adapter IC U3.

Optionally 1x6 male pin header J4 can be fitted on board for access to the JTAG interface between FTDI and FPGA on board. The pin assignment of header J4 is shown on table below:

JTAG Signal	Pin on Header J4	Note
TCK	3	-
TDI	5	-
TDO	4	-
TMS	6	-
JTAGEN	2	leave open for normal operation

Optional JTAG pin header

Micro-USB2 Connector

The Micro-USB2 connector J9 provides an interface to access the UART and JTAG functions via FTDI FT2232 chip. The use of this feature requires that USB driver is installed on your host PC.

FPGA I/O banks

Table below contains the signals and interfaces of the FPGA banks connected to pins and peripherals of the board:

Bank	I/O's Count	Connected to	Notes
2	4	1x14 pin header, J1	user GPIO's
	8	Pmod connector, J6	user GPIO's
	1	clock oscillator, U7	12.0000 MHz reference clock input

	1	clock oscillator, U10	reference clock input from optional oscillator U10
	1	accelerometer IC, U11	interrupt 1 line of Analog Devices MEMS accelerometer
5	9	1x14 pin header, J2	2 I/O's (D11, D12) of bank 5 can be pulled-up to 3.3V (4K7 resistors) with 1 I/O (D12_R) of same bank and 1 I/O (D11_R) of bank 6
	1	accelerometer IC, U11	interrupt 2 line of Analog Devices MEMS accelerometer
	1	clock oscillator, U10	control line to select adjustable oscillator output frequency
	1	temperature sensor IC, U8	interrupt line of temperature thresholds
6	18	SDRAM, U2	16bit SDRAM memory interface
3	22	SDRAM, U2	16bit SDRAM memory interface
	3	SPI interface connected to IC U8, U11, U12	SPI interface (MISO, MOSI, MCLK) for temperature sensor U8, 3-axis accelerometer U11 and ADC/DAC U12
	1	temperature sensor IC, U8	chip-select line for SPI interface
	1	accelerometer IC, U11	chip-select line for SPI interface
	1	ADC/DAC IC , U12	data input frame synchronization line of ACD/DAC IC (active low control input)
	1	temperature sensor IC, U8	interrupt line of critical temperature
1A	8	smoke detector IC, U14	SPI, I²C interface and GPIO's of smoke detector IC U14
1B	1	pin header J3	1 x digital I/O
	5	FTDI FT2232H IC U3 (4 JTAG I/O's) and pin header J4 (5 I/O's)	4 I/O's JTAG interface and 1x 'JTAGEN' signal to switch the JTAG pins to user I/O if drive this pin to GND
8	8	LEDs D2 ... D9	Red user LEDs
	6	QSPI Flash memory, U5	6 pins Quad SPI interface (2 pins have are shared function)
	6	FTDI FT2232H JTAG/UART adapter, U3	6 pins configurable as GPIO or UART
	1	Red LED, D10	Configuration DONE Led (ON when configuration in progress, OFF when configuration is done)
	1	User button S2	user configurable
	1	Reset button S1 and pin J2-10	low active reset line for FPGA reconfiguration

General overview of single ended FPGA bank I/O's

On-board Peripherals

Serial Configuration Memory

On-board serial configuration memory (U5) is provided by Winbond W74M64FVSSIQ with 64 MBit (8 MByte) storage capacity. This non volatile memory is used to store initial FPGA configuration via JTAG interface. The memory is connected to FPGA bank 1 via SPI interface.

Serial Memory U5 Pin	Signal Schematic Name	Connected to	Notes
Pin 1, CS	F_CS	FPGA bank 8, pin B3	chip select
Pin 6, CLK	F_CLK	FPGA bank 8, pin A3	clock
Pin 5, SI/IO0	F_DI	FPGA bank 8, pin A2	data in / out
Pin 7, HOLD/IO3	NSTATUS	FPGA bank 8, pin C4	data in / out (configuration dual-purpose pin of FPGA)
Pin 3, WP/IO2	DEVCLRN	FPGA bank 8, pin B9	data in / out (configuration dual-purpose pin of FPGA)
Pin 2, SO/IO1	F_DO	FPGA bank 8, pin B2	data in / out

Quad SPI Flash memory interface

SDRAM

The FPGA module is equipped with a Winbond W9864G6JT 64 MBit (8 MByte) SDRAM chip U2 in standard configuration, variants with 256 Mbit (32 MByte) memory density are also available. The SDRAM chip is connected to the FPGA bank 3 and 6 via 16-bit memory interface with 166MHz clock frequency and CL3 CAS latency.

SDRAM I/O Signals	Signal Schematic Name	Connected to	Notes
Address inputs	A0 ... A13	bank 3	-
Bank address inputs	BA0 / BA1	bank 3	-
Data input/output	DQ0 ... DQ15	bank 6	-
Data mask	DQM0 ... DQM1	bank 6	-
Clock	CLK	bank 3	
Control Signals	CS	bank 3	Chip select
	CKE	bank 3	Clock enable
	RAS	bank 3	Row Address Strobe
	CAS	bank 3	Column Address Strobe
	WE	bank 3	Write Enable

16bit SDRAM memory interface

FTDI FT2232H Chip

The FTDI chip U3 converts signals from USB2 to a variety of standard serial and parallel interfaces. Refer to the FTDI data sheet to get information about the capacity of the FT2232H chip.

The configuration of FTDI FT2232H chip is pre-programmed on the EEPROM U9.

Channel A of the FTDI chip is configured as JTAG interface (MPSSE) connected to the bank 1B of MAX10 FPGA U1.

Channel B is routed via 6 I/O's to bank 8 of MAX10 FPGA U1 and are usable as UART, GPIO, SPI or bit-banged I2C.

FTDI Chip U3 Pin	Signal Schematic Name	Connected to	Notes
Pin 12, ADBUS0	TCK	FPGA bank 1B, pin G2	JTAG interface
Pin 13, ADBUS1	TDI	FPGA bank 1B, pin F5	
Pin 14, ADBUS2	TDO	FPGA bank 1B, pin F6	
Pin 15, ADBUS3	TMS	FPGA bank 1B, pin G1	
Pin 32, BDBUS0	BDBUS0	FPGA bank 8, pin A4	user configurable
Pin 33, BDBUS1	BDBUS1	FPGA bank 8, pin B4	user configurable
Pin 34, BDBUS2	BDBUS2	FPGA bank 8, pin B5	user configurable
Pin 35, BDBUS3	BDBUS3	FPGA bank 8, pin A6	user configurable
Pin 37, BDBUS4	BDBUS4	FPGA bank 8, pin B6	user configurable
Pin 38, BDBUS5	BDBUS5	FPGA bank 8, pin A7	user configurable

FTDI chip interfaces and pins

ADC/DAC

The TEI0010 board is equipped with the Analog Devices AD5592R 8-channel, 12-bit ADC/DAC which provides eight I/O pins that can be independently configured as digital-to-analog converter (DAC) outputs, analog-to-digital converter (ADC) inputs, digital outputs, or digital inputs. The DAC has a sample frequency up to 50MHz, while ADC and digital GPIO's can be operated at 20MHz.

The ADC/DAC chip has following pin assignment with the FPGA and the board pin-headers, where its I/O pins are available:

ADC/DAC U12 pin	Signal Schematic Name	Connected to	Notes
Pin 2, I/O0	AIN0	header J1, pin 2	I/O pins configurable as DAC output, ADC input or digital GPIOs
Pin 3, I/O1	AIN1	header J1, pin 3	
Pin 4, I/O2	AIN2	header J1, pin 4	
Pin 5, I/O3	AIN3	header J1, pin 5	
Pin 8, I/O4	AIN4	header J1, pin 6	
Pin 9, I/O5	AIN5	header J1, pin 7	
Pin 10, I/O6	AIN6	header J1, pin 8	
Pin 11, I/O7	AIN7	header J3, pin 1	
Pin 6, VREF	AREF	header J1, pin 1	Analog I/O's reference voltage. Note: Internal reference voltage of 2.5V is available on this pin when enabled, else extern analog reference voltage (range: 1V ... VDD) has to be applied on this pin.
Pin 15, nRESET	ADDA_RSTN	FPGA bank 8, pin D6	IC active low reset pin
Pin 16, nSYNC	ADDA_SYNC	FPGA bank 3, pin J5	Frame synchronization signal, data is transferred in on the falling edge of the next 16 clock cycles.
Pin 14, SCLK	MCLK	FPGA bank 3, pin J7	serial clock input
Pin 13, SDI	MOSI	FPGA bank 3, pin K5	data input
Pin 7, SDO	MISO	FPGA bank 3, pin J6	data output

ADC/DAC interfaces and pins

3-Axis MEMS Accelerometer

On the TEI0010 board there is a 3-axis MEMS accelerometer present provided by Analog Devices ADXL362. This accelerometer with 12-bit internal ADC resolution offers many functions to detect motion and has also a temperature sensor integrated. It also has a FIFO buffer for storing output data. The sensor is connected to the FPGA through SPI interface and two interrupt lines.

Accelerometer U11 Pin	Signal Schematic Name	Connected to	Notes
Pin 11, INT1	MEMS_INT1	FPGA bank 2, pin L2	Interrupt lines
Pin 9, INT2	MEMS_INT2	FPGA bank 5, pin J9	
Pin 6, MOSI	MOSI	FPGA bank 3, pin K5	SPI interface
Pin 7, MISO	MISO	FPGA bank 3, pin J6	
Pin 8, nCS	MEMS_CS	FPGA bank 3, pin L5	
Pin 4, SCLK	MCLK	FPGA bank 3, pin J7	

3-axis accelerometer interfaces and pins

Smoke Detector

The TEI0010 board is equipped with the Analog Devices ADPD188BI optical module for smoke detection. The smoke detector IC has two digital GPIO's, I²C and SPI serial bus as interface for the data output and as control and configuration interface. The smoke detector IC has an integrated 128-byte FIFO buffer for conversed analog values. The values of the internal 14-bit ADC are enhanced for more precision to 20 bits, on 32-bit output register averaged ADC values with a precision of 27 bits are available. For configurable interrupts and timing signals etc., the smoke detector IC offers two GPIO's, which are routed to the FPGA.

Smoke Detector U14 pin	Signal Schematic Name	Connected to	Notes
Pin 12, SCL	IOM_SCL	FPGA bank 1A, pin F1	I²C interface
Pin 13, SDA	IOM_SDA	FPGA bank 1A, pin E1	
Pin 18, SCLK	ADP_SCK	FPGA bank 1A, pin C2	SPI interface
Pin 17, MOSI	ADP_MOSI	FPGA bank 1A, pin C1	
Pin 16, MISO	ADP_MISO	FPGA bank 1A, pin E4	
Pin 19, CSB	ADP_CS	FPGA bank 1A, pin B1	
Pin 14, GPIO0	IOM_GPIO0	FPGA bank 1A, pin E3	GPIO's
Pin 15, GPIO1	IOM_GPIO1	FPGA bank 1A, pin D1	

Smoke detector interfaces and pins

Temperature Sensor

The TEI0010 is equipped with the Analog Devices ADT7320 temperature sensor with SPI interface. The temperature sensor offers a temperature value resolution of 16-bit and high accuracy in temperature measuring. The temperature sensor has two interrupt lines which are configurable to be triggered at a programmable undertemperature/overtemperature or critical temperature value.

Temperature Sensor U8 pin	Signal Schematic Name	Connected to	Notes
Pin 1, SCLK	MCLK	FPGA bank 3, pin J7	SPI interface
Pin 3, DIN	MOSI	FPGA bank 3, pin K5	
Pin 2, DOUT	MISO	FPGA bank 3, pin J6	
Pin 4, nCS	TEMP_CS	FPGA bank 3, pin L4	
Pin 9, INT	TEMP_INT	FPGA bank 5, pin L13	Interrupt lines
Pin 10, CT	TEMP_CT	FPGA bank 3, pin N12	

Temperature sensor interfaces and pins

System Clock Oscillator

The FPGA SoC module has following reference clocking signals provided by on-board oscillators:

Clock Source	Schematic Name	Frequency	Clock Input Destination	Notes
Microchip MEMS Oscillator DSC6011ME2A, U7	CLK12M	12.0000MHz	FTDI FT2232 U3, pin 3; FPGA SoC bank 2, pin H6	-

Adjustable Oscillator LTC1799CS5, U10	OSC_CLK	8.33MHz / 833.33KHz / 83.33KHz	FPGA SoC bank 2, pin G5	Frequency is set with signal 'OSC_DIV', which is tied to FPGA bank 5, pin H9. Following settings are available: FPGA pin H9 ('OSC_DIV') open drain: 8.33MHz FPGA pin H9 ('OSC_DIV') floating: 833.33KHz FPGA pin H9 ('OSC_DIV') pulled to 3.3 V: 83.33KHz

Clock sources overview

On-board LEDs

There are 10 LEDs fitted on the FPGA module board. The LEDs are user configurable to indicate for example any system status.

LED	Color	Signal Schematic Name	FPGA	Notes
D1	Green	3.3V	-	Indicating 3.3V board supply voltage
D2	Red	'LED1'	bank 8, pin D8	user
D3	Red	'LED2'	bank 8, pin A8	user
D4	Red	'LED3'	bank 8, pin A9	user
D5	Red	'LED4'	bank 8, pin C9	user
D6	Red	'LED5'	bank 8, pin A10	user
D7	Red	'LED6'	bank 8, pin B10	user
D8	Red	'LED7'	bank 8, pin A11	user
D9	Red	'LED8'	bank 8, pin C10	user
D10	Red	'CONF_DONE'	bank 8, pin C5	indication configuration is DONE when LED is off

LEDs of the module

Push Buttons

The FPGA module is equipped with two push buttons S1 and S2:

Button	Signal Schematic Name	FPGA	Notes
S1	'USER_BTN'	bank 8, pin E6	user configurable
S2	'RESET'	bank 8, pin E7	FPGA reset

Push buttons of the module

Connectors

All connectors are are for 100mil headers, all connector locations are in 100mil (2.54mm) grid. The module's PCB provides footprints to mount and solder optional pin headers, if those are not factory-fitted on module.

Power and Power-On Sequence

Power Consumption

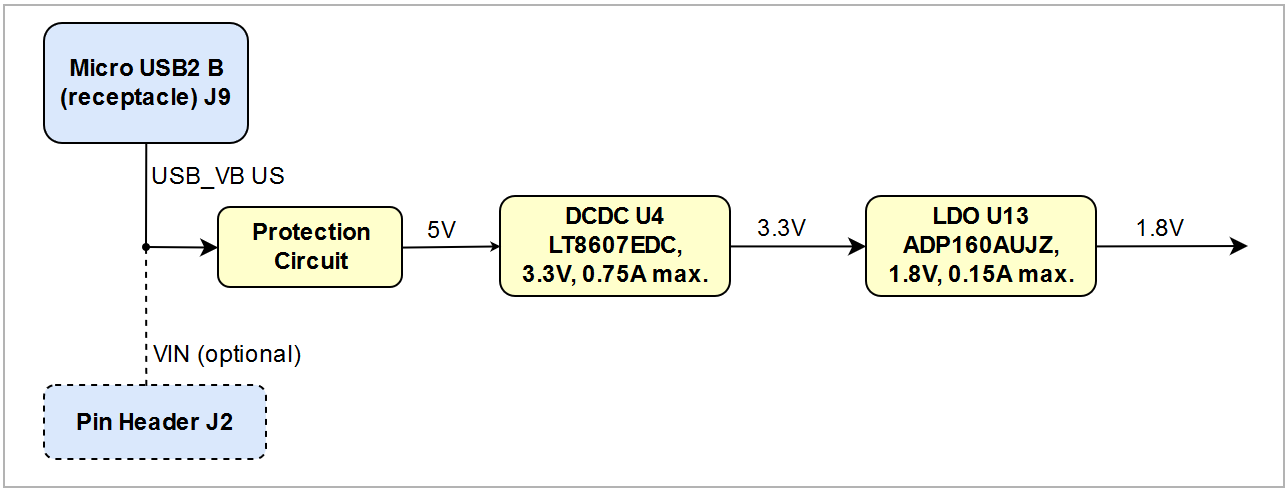
To power-up a module, power supply with minimum current capability of 1A is recommended.

Power Supply

The FPGA module can be power-supplied through Micro USB2 connector J9 with supply voltage 'USB-VBUS' or alternative through pin header J2 with supply voltage 'VIN'.

The TEI0010 module needs one single power supply of 5.0V nominal.

There are following dependencies how the initial voltage of the extern power supply is distributed to the on-board DCDC converters:



Power Distribution

Power Consumption

FPGA	Design	Typical Power, 25C ambient
Intel MAX 10 10M08 FPGA SoC	Not configured	TBD*

Module power consumption

*TBD - To Be Determined.

Actual power consumption depends on the FPGA design and ambient temperature.

Power-On Sequence

There is no specific or special power-on sequence, just one single power source is needed.

Power Rails

Connector Designator	VCC / VCCIO Schematic Name	Voltage	Direction	Pins	Notes
J2	5V	5.0V	Out	Pin 14	-
	VIN	5.0V	In	Pin 13	-

	3.3V	3.3V	Out	Pin 12	-
J6	3.3V	3.3V	Out	Pin 6, 12	-
J9	USB_VBUS	5.0V	In	Pin 1	-

Connector power pin description

Bank Voltages

Bank	Voltage	Voltage Range
2	3.3V	all bank voltages fixed
3	3.3V	
5	3.3V	
6	3.3V	
1A	1.8V	
1B	3.3V	
8	3.3V	

FPGA SoC VCCO bank voltages

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference document
VIN supply voltage (5.0V nominal)	4.75	5.25	V	
I/O Input voltage for FPGA I/O bank	-0.5	4.12	V	Intel MAX 10 datasheet
Voltage on ADC/DAC IC U12 pins	-0.3	3.6	V	AD5592R datasheet
Analog reference voltage on IC U12	-0.3	3.6	V	AD5592R datasheet
Storage Temperature	-40	+90	°C	LED R6C-AL1M2VY/3T datasheet

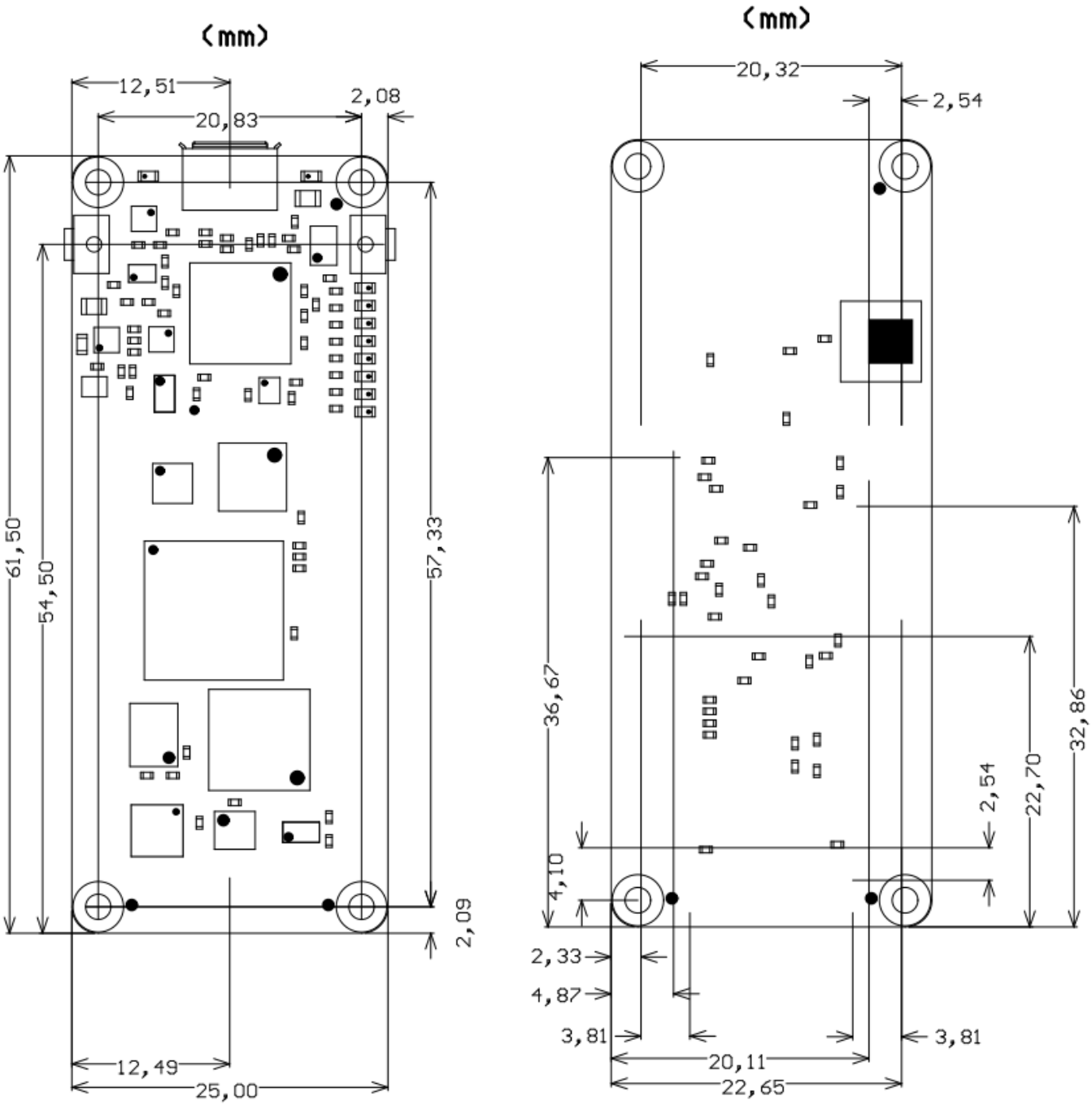
Module absolute maximum ratings

Recommended Operating Conditions

Parameter	Min	Max	Units	Reference document
VIN supply voltage (5.0V nominal)	4.75	5.25	V	
I/O Input voltage for FPGA I/O bank	–0.5	3.6	V	Intel MAX 10 datasheet
Voltage on ADC/DAC IC U12 pins	0	3.3	V	AD5592R datasheet
Analog reference voltage on IC U12	1	3.3	V	AD5592R datasheet
Operating temperature range	0	+70	°C	Winbond datasheet W9864G6GT

Recommended Operating Conditions

Physical Dimensions



Physical dimensions drawing

Variants Currently In Production

Trenz shop TE0xxx overview page	
English page	German page

Trenz Electronic Shop Overview

Revision History

Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
-	02	First Production Release	-	TEI0010-02
-	01	Prototypes	-	-

Hardware Revision History

Document Change History

Date	Revision	Contributor	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] Unknown macro: 'metadata'	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• fixed typographical and other mistakes
2018-09-27	v.22	Ali Naseri	• initial release

--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• ---

Document change history.

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Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]