TEF1001 CPLD

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Overview

Firmware for PCB-Master CPLD with designator U5: LCMX02-1200HC.

Feature Summary

- Power Management
- Reset Management
- FMC JTAG
- LED Control
- FAN Control (FPGA)
- FAN Control (FMC
- I2C MUX

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Description	Connection changes compared to REV01
200MHZCLK_EN	out	30	Enable 200MHz Osc.	
BUTTON	in	77	Reset Button	
CPLD_JTAG_TCK	in	91	optional FMC JTAG	
CPLD_JTAG_TDI	in	94	optional FMC JTAG	
CPLD_JTAG_TDO	out	95	optional FMC JTAG	
CPLD_JTAG_TMS	in	90	optional FMC JTAG	
DDR3_SCL	inout	43	I2C connected to FPGA	
DDR3_SDA	inout	42	I2C connected to FPGA	
DONE	in	18	FPGA Done	
EN_1V8	out	58	Power Enable	
EN_3V3FMC	out	60	Power Enable	
EN_FMC_VADJ	out	51	Power Enable	
F1PWM	out	98	FAN	
F1SENSE	in	99	FAN / currently_not_used	
FEX_DIR		19	/ currently_not_used	
FEX0	out	12	PERST from PCIe slot	
FEX1		15	/ currently_not_used	
FEX10		4	/ currently_not_used	
FEX11	in	10	User LED	
FEX2		13	/ currently_not_used	
FEX3		9	/ currently_not_used	
FEX4		3	/ currently_not_used	
FEX5		7	/ currently_not_used	
FEX6		24	/ currently_not_used	
FEX7		17	/ currently_not_used	
FEX8		21	/ currently_not_used	
FEX9		25	/ currently_not_used	
FAN_FMC_EN	out	78	FMC FAN Enable	not connected on REV01
FMC_PG_C2M		69	/ currently_not_used	
FMC_PG_M2C		68	/ currently_not_used	
FMC_PRSNT	in	40	FMC Present (inverted FMC_PRSNT_M2C_L)	not connected on REV01
N.C.		70	Not Connected	FMC_PRSNT_M2C_L on REV01
FMC_SCL		49	I2C connected to FPGA	
FMC_SDA		48	I2C connected to FPGA	
FMC_TCK		27	/ currently_not_used	
FMC_TDI		31	/ currently_not_used	
FMC_TDO		32	/ currently_not_used	
FMC_TMS		28	/ currently_not_used	

FMC_TRST		36	/ currently_not_used	
FPGA_IIC_OE		14	I2C FPGA	
FPGA_IIC_SCL		1	I2C FPGA	
FPGA_IIC_SDA		16	I2C FPGA	
JTAG_EN	in	82	JTAG ENABLE over DIP S1-1	constant high on REV01
LED1	out	76	Status LED D1 (green)	
LTM_1V_IO0		86	Power Good	
LTM_1V_IO1		88	Power Good	
LTM_1V5_4V_IO0		85	Power Good	
LTM_1V5_4V_IO1		83	Power Good	
LTM_1V5_RUN		74	/ currently_not_used	
LTM_4V_RUN		75	/ currently_not_used	
LTM_SCL		67	I2C connected to FPGA	
LTM_SDA		66	I2C connected to FPGA	
LTM1_ALERT		65	/ currently_not_used	
LTM2_ALERT		64	/ currently_not_used	
PCIE_RSTB	in	37	PERST from PCIe card edge connector	
PG_1V8	in	59	Power Good	
PG_3V3	in	61	Power Good	
PG_FMC_VADJ	in	52	Power Good	
PLL_SCL	inout	2	I2C SI5338	
PLL_SDA	inout	8	I2C SI5338	
PROGRAM_B	out	20	FPGA PROG_B	
VID0_FMC_VADJ	out	53	FMC EN5365QI power selection pin	
VID0_FMC_VADJ_CTRL	in	71	Power pin pre-selection for FMC VADJ through DIP SW S1-2. CPLD decides.	not connected on REV01
VID1_FMC_VADJ	out	54	FMC EN5365QI power selection pin	
VID1_FMC_VADJ_CTRL	in	63	Power pin pre-selection for FMC VADJ through DIP SW S1-3. CPLD decides.	not connected on REV01
VID2_FMC_VADJ	out	57	FMC EN5365QI power selection pin	
VID2_FMC_VADJ_CTRL	in	62	Power pin pre-selection for FMC VADJ through DIP SW S1-4. CPLD decides.	not connected on REV01

Functional Description

JTAG

CPLD JTAG is selectable with DIP S1-1. (ON FMC, OFF CPLD).

FMC JTAG is accessible with J9 JTAG Pinheader on PCB REV02 and newer only.

Power

Power sequence on will be executed over 4 States:

- State 1 IDLE: Wait until LTM_1V_IO0 (1V), LTM_1V_IO1 (1V) and LTM_1V5_4V_IO1 (4V) is available.
- State 2 PS1: Enables 1V8, 3V3FMC and VADJ. Wait until PG_1V8 (1.8V), PG_3V3 (3.3V) and PG_FMC_VADJ (FMC VADJ) is available.
- State 3 PS2: Wait until LTM_1V5_4V_IO0 (1.5V) is available
- State 4 RDY: All power on

State machine restart power sequencing, if on of the power good signal are lost.

FMC VADJ is selectable via DIP S1-2...4.

S1-4	S1-3	S1-2	Voltage
OFF	OFF	OFF	3.3V
OFF	OFF	ON	2.5V
OFF	ON	OFF	1.9V
OFF	ON	ON	1.5V
ON	OFF	OFF	1.25V
ON	OFF	ON	1.2V

Note on PCB REV01 it's fix 1.8V.

Reset

PROGRAM_B is controlled by push button after power up sequencing is ready.

CLK

200MHz CLK is enabled after power up.

I2C

Connect SI5338, LTM and FMC, SODIMM I2C and internal FAN Control to FPGA I2C Bus.

FAN1

I2C Baseaddress: 0x74 (changeable with Firmware update). I2C with 8Bit Register Address with 8Bit Data. I2C CLK currently 20 MHz supported.

Write Access:

Register Address	Name	Description
0	FAN CTRL	Enable FAN1 (Bit7)
1	FAN1 PWM	FAN1 PWM (0%-100%, Default 80%)

Read Access:

Register Address	Name	Description
0	FAN CTRL	FAN Control register
1	FAN1 RPS	FAN1 Revolutions per second

FAN FMC

Is enabled/disabled with FMC preset signal (PCB REV02 only).

Button

Button is debounced and controls PROG_B signal from FPGA.

LED

LED is used as Status LED for power management and programming. Status depends on blink sequence.

Status	Blink sequence	Comment
Error - Power IDLE state	********	Reset or Main Power Problem
Error - Power PS1 state	*****ooo	Periphery Power Problem (1.8V, 3.3V, FMC VADJ)
Error - Power PS2 state	****oooo	DDR Bank Power Problem (1.5V)
Power Ready, FPGA not programmed	***ooooo	~0,7 Hz, duty cycle 3/8
--	**oooooo	~0,7 Hz, duty cycle 2/8, currently not used
--	*ooooooo	~0,7 Hz, duty cycle 1/8, currently not used
User Mode	user defined	Power Ready, FPGA programmed, LED is accessible over FEX11

Appx. A: Change History and Legal Notices

Revision Changes

CPLD REV02 to REV03

- FMC JTAG access over CPLD Programmer (not accessible on PCB REV01)
- DIP VADJ (not usable on PCB REV01)
- FMC FAN EN/DIS over FMC_PRSNT (not usable on PCB REV01)

CPLD REV01 to REV02

- BUGFIX: PCIe Reset
- USER LED accessible
- I2C for SI5338, LTM, FMC, SODIMM
- Add FAN Control over I2C

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV03	REV02		• REV03 finished

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24 Oct 2018	v.1	REV02	REV01		• Revision 02 finished • separate page for PCB REV01
2017-08-06	v.1	REV01	REV01	John Hartfiel	• REV01 finished
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