

TEF1001 CPLD

Table of contents

- [1 Table of contents](#)
- [2 Overview](#)
 - [2.1 Feature Summary](#)
 - [2.2 Firmware Revision and supported PCB Revision](#)
- [3 Product Specification](#)
 - [3.1 Port Description](#)
 - [3.2 Functional Description](#)
 - [3.2.1 JTAG](#)
 - [3.2.2 Power](#)
 - [3.2.3 Reset](#)
 - [3.2.4 CLK](#)
 - [3.2.5 I2C](#)
 - [3.2.6 FAN1](#)
 - [3.2.7 FAN FMC](#)
 - [3.2.8 Button](#)
 - [3.2.9 LED](#)
- [4 Appx. A: Change History and Legal Notices](#)
 - [4.1 Revision Changes](#)
 - [4.2 Document Change History](#)
- [5 Appx. A: Legal Notices](#)
 - [5.1 Data Privacy](#)
 - [5.2 Document Warranty](#)
 - [5.3 Limitation of Liability](#)
 - [5.4 Copyright Notice](#)
 - [5.5 Technology Licenses](#)
 - [5.6 Environmental Protection](#)
 - [5.7 REACH, RoHS and WEEE](#)

Overview

Firmware for PCB-Master CPLD with designator U5: LCMX02-1200HC.

Feature Summary

- Power Management
- Reset Management
- FMC JTAG
- LED Control
- FAN Control (FPGA)
- FAN Control (FMC)
- I2C MUX

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Description	Connection changes compared to REV01
200MHZCLK_EN	out	30	Enable 200MHz Osc.	
BUTTON	in	77	Reset Button	
CPLD_JTAG_TCK	in	91	optional FMC JTAG	
CPLD_JTAG_TDI	in	94	optional FMC JTAG	
CPLD_JTAG_TDO	out	95	optional FMC JTAG	
CPLD_JTAG_TMS	in	90	optional FMC JTAG	
DDR3_SCL	inout	43	I2C connected to FPGA	
DDR3_SDA	inout	42	I2C connected to FPGA	
DONE	in	18	FPGA Done	
EN_1V8	out	58	Power Enable	
EN_3V3FMC	out	60	Power Enable	
EN_FMC_VADJ	out	51	Power Enable	
F1PWM	out	98	FAN	
F1SENSE	in	99	FAN / <i>currently_not_used</i>	
FEX_DIR		19	<i>/ currently_not_used</i>	
FEX0	out	12	PERST from PCIe slot	
FEX1		15	<i>/ currently_not_used</i>	
FEX10		4	<i>/ currently_not_used</i>	
FEX11	in	10	User LED	
FEX2		13	<i>/ currently_not_used</i>	
FEX3		9	<i>/ currently_not_used</i>	
FEX4		3	<i>/ currently_not_used</i>	
FEX5		7	<i>/ currently_not_used</i>	
FEX6		24	<i>/ currently_not_used</i>	
FEX7		17	<i>/ currently_not_used</i>	
FEX8		21	<i>/ currently_not_used</i>	
FEX9		25	<i>/ currently_not_used</i>	
FAN_FMC_EN	out	78	FMC FAN Enable	not connected on REV01
FMC_PG_C2M		69	<i>/ currently_not_used</i>	
FMC_PG_M2C		68	<i>/ currently_not_used</i>	
FMC_PRSNT	in	40	FMC Present (inverted FMC_PRSNT_M2C_L)	not connected on REV01
N.C.		70	Not Connected	FMC_PRSNT_M2C_L on REV01
FMC_SCL		49	I2C connected to FPGA	
FMC_SDA		48	I2C connected to FPGA	
FMC_TCK		27	<i>/ currently_not_used</i>	
FMC_TDI		31	<i>/ currently_not_used</i>	
FMC_TDO		32	<i>/ currently_not_used</i>	
FMC_TMS		28	<i>/ currently_not_used</i>	

FMC_TRST		36	/ currently_not_used	
FPGA_IIC_OE		14	I2C FPGA	
FPGA_IIC_SCL		1	I2C FPGA	
FPGA_IIC_SDA		16	I2C FPGA	
JTAG_EN	in	82	JTAG ENABLE over DIP S1-1	constant high on REV01
LED1	out	76	Status LED D1 (green)	
LTM_1V_IO0		86	Power Good	
LTM_1V_IO1		88	Power Good	
LTM_1V5_4V_IO0		85	Power Good	
LTM_1V5_4V_IO1		83	Power Good	
LTM_1V5_RUN		74	/ currently_not_used	
LTM_4V_RUN		75	/ currently_not_used	
LTM_SCL		67	I2C connected to FPGA	
LTM_SDA		66	I2C connected to FPGA	
LTM1_ALERT		65	/ currently_not_used	
LTM2_ALERT		64	/ currently_not_used	
PCIE_RSTB	in	37	PERST from PCIe card edge connector	
PG_1V8	in	59	Power Good	
PG_3V3	in	61	Power Good	
PG_FMC_VADJ	in	52	Power Good	
PLL_SCL	inout	2	I2C SI5338	
PLL_SDA	inout	8	I2C SI5338	
PROGRAM_B	out	20	FPGA PROG_B	
VID0_FMC_VADJ	out	53	FMC EN5365QI power selection pin	
VID0_FMC_VADJ_CTRL	in	71	Power pin pre-selection for FMC VADJ through DIP SW S1-2. CPLD decides.	not connected on REV01
VID1_FMC_VADJ	out	54	FMC EN5365QI power selection pin	
VID1_FMC_VADJ_CTRL	in	63	Power pin pre-selection for FMC VADJ through DIP SW S1-3. CPLD decides.	not connected on REV01
VID2_FMC_VADJ	out	57	FMC EN5365QI power selection pin	
VID2_FMC_VADJ_CTRL	in	62	Power pin pre-selection for FMC VADJ through DIP SW S1-4. CPLD decides.	not connected on REV01

Functional Description

JTAG

CPLD JTAG is selectable with DIP S1-1. (ON FMC, OFF CPLD).

FMC JTAG is accessible with J9 JTAG Pinheader on PCB REV02 and newer only.

Power

Power sequence on will be executed over 4 States:

- State 1 IDLE: Wait until LTM_1V_IO0 (1V), LTM_1V_IO1 (1V) and LTM_1V5_4V_IO1 (4V) is available.
- State 2 PS1: Enables 1V8, 3V3FMC and VADJ. Wait until PG_1V8 (1.8V), PG_3V3 (3.3V) and PG_FMC_VADJ (FMC VADJ) is available.
- State 3 PS2: Wait until LTM_1V5_4V_IO0 (1.5V) is available
- State 4 RDY: All power on

State machine restart power sequencing, if on of the power good signal are lost.

FMC VADJ is selectable via DIP S1-2...4.

S1-4	S1-3	S1-2	Voltage
OFF	OFF	OFF	3.3V
OFF	OFF	ON	2.5V
OFF	ON	OFF	1.9V
OFF	ON	ON	1.5V
ON	OFF	OFF	1.25V
ON	OFF	ON	1.2V

Note on PCB REV01 it's fix 1.8V.

Reset

PROGRAM_B is controlled by push button after power up sequencing is ready.

CLK

200MHz CLK is enabled after power up.

I2C

Connect SI5338, LTM and FMC, SODIMM I2C and internal FAN Control to FPGA I2C Bus.

FAN1

I2C Baseaddress: 0x74 (changeable with Firmware update). I2C with 8Bit Register Address with 8Bit Data. I2C CLK currently 20 MHz supported.

Write Access:

Register Address	Name	Description
0	FAN CTRL	Enable FAN1 (Bit7)
1	FAN1 PWM	FAN1 PWM (0%-100%, Default 80%)

Read Access:

Register Address	Name	Description
0	FAN CTRL	FAN Control register
1	FAN1 RPS	FAN1 Revolutions per second

FAN FMC

Is enabled/disabled with FMC preset signal (PCB REV02 only).

Button

Button is debounced and controls PROG_B signal from FPGA.

LED

LED is used as Status LED for power management and programming. Status depends on blink sequence.

Status	Blink sequence	Comment
Error - Power IDLE state	*****	Reset or Main Power Problem
Error - Power PS1 state	****000	Periphery Power Problem (1.8V, 3.3V, FMC VADJ)
Error - Power PS2 state	***0000	DDR Bank Power Problem (1.5V)
Power Ready, FPGA not programmed	**00000	~0,7 Hz, duty cycle 3/8
--	**000000	~0,7 Hz, duty cycle 2/8, currently not used
--	*0000000	~0,7 Hz, duty cycle 1/8, currently not used
User Mode	user defined	Power Ready, FPGA programmed, LED is accessible over FEX11

Appx. A: Change History and Legal Notices

Revision Changes

CPLD REV02 to REV03

- FMC JTAG access over CPLD Programmer (not accessible on PCB REV01)
- DIP VADJ (not usable on PCB REV01)
- FMC FAN EN/DIS over FMC_PRSNT (not usable on PCB REV01)

CPLD REV01 to REV02

- BUGFIX: PCIe Reset
- USER LED accessible
- I2C for SI5338, LTM, FMC, SODIMM
- Add FAN Control over I2C

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV03	REV02		• REV03 finished

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.
proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.
proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

 **Unknown macro: 'metadata'**

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.
proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

confluence.
pages.
Page]
due to
overlapping
prototypes
between:
[interface
com.
atlassian.
confluence.
user.
ConfluenceUser,
class
java.
lang.
String,
class
com.
atlassian.
confluence.
core.
ContentEntity
Object]
[interface
com.

				atlassi an. user. User, class java. lang. String, class com. atlassi an. conflue nce. core. Conten tEntity Object]	
24 Oct 2018	v.1	REV02	REV01		• Revision 02 finished • separate page for PCB REV01
2017-08-06	v.1	REV01	REV01	John Hartfiel	• REV01 finished
2017-05-29	v.1	---		Error render ing macro 'page- info' Ambig uous metho d	• Initial release

overlo
ading
for
metho
d jdk.
proxy2
79.\$Pr
oxy402
2#has
Conten
tLevel
Permis
sion.
Cannot
resolve
which
metho
d to
invoke
for
[null,
class
java.
lang.
String,
class
com.
atlassi
an.
conflue
nce.
pages.
Page]
due to
overla
pping
prototy
pes
betwee

n:
[interfa
ce
com.
atlassi
an.
conflue
nce.
user.
Conflu
enceU
ser,
class
java.
lang.
String,
class
com.
atlassi
an.
conflue
nce.
core.
Conten
tEntity
Object]
[interfa
ce
com.
atlassi
an.
user.
User,
class
java.
lang.
String,
class
com.

				atlassi an. conflue nce. core. Conten tEntity Object]	
	All			Error render ing macro 'page- info' Ambig uous metho d overlo ading for metho d jdk. proxy2 79.\$Pr oxy402 2#has Conten tLevel Permis sion. Cannot resolve which	

metho
d to
invoke
for
[null,
class
java.
lang.
String,
class
com.
atlassi
an.
conflue
nce.
pages.
Page]
due to
overla
pping
prototy
pes
betwee
n:
[interfa
ce
com.
atlassi
an.
conflue
nce.
user.
Conflu
enceU
ser,
class
java.
lang.
String,

				class com. atlassi an. conflue nce. core. Conten tEntity Object] [interfa ce com. atlassi an. user. User, class java. lang. String, class com. atlassi an. conflue nce. core. Conten tEntity Object]	
--	--	--	--	---	--

Appx. A: Legal Notices

Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

Document Warranty

The material contained in this document is provided "as is" and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method `jdk.proxy279.$Proxy4022#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`