

# TEF1001 Test Board

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## Overview

TEF1001 SI5338 Configuration, DDR Configuration and PCIe Core Example Design.

Refer to <http://trenz.org/tef1001-info> for the current online version of this manual and other available documentation.

## Key Features

- MicroBlaze
- I2C
- Flash
- FMeter
- PCIe
- SI5338
- DDR3 ECC SODIMM (currently ECC disabled)

## Revision History

Date	Vivado	Project Built	Authors	Description
2018-10-25	2018.2	TEF1001-test_board-vivado_2018.2-build_03_20181025165553.zip TEF1001-test_board_noprebuilt-vivado_2018.2-build_03_20181025165625.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• Add -410 assembly variant</li> <li>• Add some notes on Board part Files (summary window description)</li> </ul>
2018-10-25	2018.2	TEF1001-test_board_noprebuilt-vivado_2018.2-build_03_20181024154054.zip TEF1001-test_board-vivado_2018.2-build_03_20181024154034.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• 2018.2</li> <li>• add TEF1001-02</li> <li>• MIG Configuration for AW12P7218BLK0M (4GB for REV01)</li> <li>• MIG Configuration for AW24P7228BLK0M (8GB for REV02)</li> <li>• BUGFIX QSPI IP configuration</li> <li>• add SREC to load application into DDR</li> </ul>
2018-03-07	2017.4	TEF1001-test_board_noprebuilt-vivado_2017.4-build_06_20180307102924.zip TEF1001-test_board-vivado_2017.4-build_06_20180307102845.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• 2017.4 update</li> <li>• new assembly variant</li> </ul>
2017-11-28	2017.2	TEF1001-test_board-vivado_2017.2-build_05_20171128114335.zip TEF1001-test_board_noprebuilt-vivado_2017.2-build_05_20171128114350.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• initial release</li> </ul>

### Design Revision History

## Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
DDR3 ECC SODIMM	DDR3 does not work with ECC enabled	Disable ECC: <ul style="list-style-type: none"> <li>• for Block Design MIG with AXI Interface, create 64Bit MIG</li> <li>• for RTL MIG with Native Interface, disable ECC on MIG configuration and use 72Bit for Data</li> </ul>	---

### Known Issues

## Requirements

### Software

Software	Version	Note
Vivado	2018.2	needed
SDK	2018.2	needed

SI5338 Clock Builder	---	optional
----------------------	-----	----------

#### Software

## Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).

Complete List is available on <design name>/board\_files/\*\_board\_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TEF1001-01-160-2I	1_160_2	REV01	DDR3 ECC SODIMM*	32MB		<ul style="list-style-type: none"> <li>DDR configured for AW12P7218BLK0M (4GB for REV01)</li> </ul>
TEF1001-01-325-2C	1_325_2	REV01	DDR3 ECC SODIMM*	32MB		<ul style="list-style-type: none"> <li>DDR configured for AW12P7218BLK0M (4GB for REV01)</li> </ul>
TEF1001-02-160-2I	2_160_2	REV02	DDR3 ECC SODIMM	32MB		<ul style="list-style-type: none"> <li>DDR configured for AW24P7228BLK0M (8GB for REV02)</li> </ul>
TEF1001-02-325-2C	2_325_2	REV02	DDR3 ECC SODIMM	32MB		<ul style="list-style-type: none"> <li>DDR configured for AW24P7228BLK0M (8GB for REV02)</li> </ul>
TEF1001-02-410-2I	2_410_2	REV02	DDR3 ECC SODIMM	32MB		<ul style="list-style-type: none"> <li>DDR configured for AW24P7228BLK0M (8GB for REV02)</li> </ul>

\* PCB REV01 DDR3 ECC SODIMM is limited to 4GB, for PCB REV02 up to 8GB is possible

#### Hardware Modules

Design supports following carriers:

Carrier Model	Notes
PC with PCIe Card slot	
Stand-alone	

#### Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
JTAG Programmer	<ul style="list-style-type: none"> <li>TE0790 with TE0791 for CPLD or FPGA</li> <li>Xilinx compatible JTAG programmer for FPGA</li> </ul>

DDR3 (204 Pin with ECC)	<ul style="list-style-type: none"> <li>for example: <ul style="list-style-type: none"> <li>AW12P7218BLK0M ( max. 4GB for REV01)</li> <li>AW24P7228BLK0M (max. 8GB for REV02)</li> </ul> </li> </ul>
-------------------------	---

#### Additional Hardware

## Content

For general structure and of the reference design, see [Project Delivery - AMD devices](#)

## Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI

#### Design sources

## Additional Sources

Type	Location	Notes
SI5338	<design name>/misc/SI5338	SI5338 Project with current PLL Configuration

#### Additional design sources

## Prebuilt

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems
SREC-File	*.srec	Converted Software Application for MicroBlaze Processor Systems

#### Prebuilt files (only on ZIP with prebuilt content)

## Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TEF1001 "Test Board" Reference Design](#)

## Design Flow



Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [AMD Development Tools#XilinxSoftware-BasicUserGuides](#)
- [Vivado Projects - TE Reference Design](#)
- [Project Delivery.](#)

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "\_create\_win\_setup.cmd" on Windows OS and "\_create\_linux\_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)

1. \_create\_win\_setup.cmd/\_create\_linux\_setup.sh and follow instructions on shell:

```
C:\WINDOWS\system32\cmd.exe
B:\Design\cores\2017.2\design\TEF1001\test_board>setlocal
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: B:\Design\cores\2017.2\design\TEF1001\test_board\
-----TE Reference Design-----
-- (c) Go to CMD-File Generation (Manual setup)
-- (d) Go to Documentation (Web Documentation)
-- (x) Exit Batch (nothing is done!)
-- (0) Create minimum setup of CMD-Files and exit Batch
-- (1) Create maximum setup of CMD-Files and exit Batch
-----
Select (ex.: '0' for min setup):
```

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
  - a. Select correct device and Xilinx install path on "design\_basic\_settings.cmd" and create Vivado project with "vivado\_create\_project\_gui mode.cmd"  
Note: Select correct one, see [TE Board Part Files](#)
5. Create HDF and export to prebuilt folder
  - a. Run on Vivado TCL: TE::hw\_build\_design -export\_prebuilt  
Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate Programming Files with HSI/SDK

- a. Start with TE Scripts on Vivado TCL: `TE::sw_run_hsi`  
(optional) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: `TE::sw_run_sdk` to generate files manually  
Note: See [SDK Projects](#)
- b. (optional )Copy "prebuilt\software\<short dir>\srec\_spi\_bootloader.elf" into "firmware\microblaze\_0" (replace shipped one) and regenerate design again (HW (Step5)+SW(Step6 only a.))

## Launch

## Programming



Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](#)

## QSPI

1. Connect JTAG and Power ON PC
2. Open Vivado Project with "vivado\_open\_existing\_project\_gui mode.cmd" or if not created, create with "vivado\_create\_project\_gui mode.cmd"
3. Type on Vivado TCL Console: `TE::pr_program_flash_mcsfile -swapp hello_tef1001`
4. Reboot PC

## SD

Not supported.

## JTAG

- Connect Vivado HW Manager and program FPGA  
Note: PCIe enumeration will be not done in this case. SREC Bootloader need Hello TEF1001 application on QSPI Flash for output

## Usage

1. Prepare HW like described on section [Programming](#)
2. Power On PCB  
Note: 1. FPGA Load Bitfile into FPGA, modified SREC Bootloader configure SI5338 and load application from QSPI into DDR (Depends on linker script)

## JTAG/UART Console:

- Launch the XSDB console on SDK (Xilinx XSCT Console):
  - type: connect
  - type: targets -set -filter {name =~ "MicroBlaze Debug\*"} -index 0
  - type: jtagterminal -start

- Separat console starts:

```

C:\Xilinx\SDK\2018.2\bin\unwrapped\win64-o\tclsh85t.exe

Terminal requirements :
(i) Processor's STDOUT is redirected to the ARM DCC/MDM UART
(ii) Processor's STDIN is redirected to the ARM DCC/MDM UART.
Then, text input from this console will be sent to DCC/MDM's UART port.
NOTE: This is a line-buffered console and you have to press "Enter"
to send a string of characters to DCC/MDM.

Hello TEF1001 (Loop: 329)
Hello TEF1001 (Loop: 330)
Hello TEF1001 (Loop: 331)
Hello TEF1001 (Loop: 332)
Hello TEF1001 (Loop: 333)
Hello TEF1001 (Loop: 334)
Hello TEF1001 (Loop: 335)
Hello TEF1001 (Loop: 336)
Hello TEF1001 (Loop: 337)
Hello TEF1001 (Loop: 338)
Hello TEF1001 (Loop: 339)

```

## Vivado HW Manager:

1. Open Vivado HW Manager
2. Add VIO to Dashboard:
3. Set Radix to unsigned integer for FMeterCLKs (labt\_SI\_\*)
4. Control:
  - a. USER LEDs are selectable  
Note USR\_CPLD\_LED on PCB REV1 and REV02, USR\_LED Matrix only on REV02
  - b. Optional PCIe Core Reset (on FPGA only)
  - c. Optional System Reset (on FPGA only)
5. Read: All SI5338 CLKs (Unit Hz), PCIe Cor MMCM Lock signal, MIG MMCM Lock signal, MIG Init Calibration Done

HARDWARE MANAGER - localhost\Xilinx\_tcl\Xilinx\00001176835d01

Name	Status
localhost (1)	Connected
Xilinx_tcl\Xilinx\00001176835d01	Open
xc7k160t_0 (3)	Programmed
XADC (System Monitor)	
hw_vio_1 (msys_l/vio_0)	OK - Outputs F
mt25qu256-spi-x1_x2_x4	

hw\_vio\_1

Name	Value	Activity	Direction	VIO
msys_l/axi_pcie_0_mmcm_lock	[B] 1		Input	hw_vio_1
msys_l/labt_SI_CLK0[31:0]	[U] 62501923		Input	hw_vio_1
msys_l/labt_SI_CLK1[31:0]	[U] 125003845		Input	hw_vio_1
msys_l/labt_SI_CLK2[31:0]	[U] 250007694		Input	hw_vio_1
msys_l/labt_SI_MGT[31:0]	[U] 156254808		Input	hw_vio_1
msys_l/mig_7series_0_init_calib_complete	[B] 1		Input	hw_vio_1
msys_l/mig_7series_0_mmcm_locked	[B] 1		Input	hw_vio_1
msys_l/pcie_rst_n	[B] 1		Output	hw_vio_1
msys_l/sys_rst_n	[B] 1		Input	hw_vio_1
msys_l/sys_rst_n_1	[B] 1		Output	hw_vio_1
msys_l/USR_CPLD_LED[0:0]	[B] 0		Output	hw_vio_1
msys_l/USR_LED[9:0]	[H] 000		Output	hw_vio_1

## PC:

- Use for example PCI-Z (Win) or KInfoCenter (Linux) or lspci command (Linux console) to detect PCIe Card





### i\_bitgen\_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property CONFIG_VOLTAGE 1.8 [current_design]
set_property CFGBVS GND [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

### i\_common.xdc

```
#
#
#
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design]
```

## Design specific constrain

### i\_io.xdc

```
#-----
#USER LED Matrix
#

#USER LEDS CONNECTED TO A FMC_ADJ VCCO BANK (default config 1.8V)
set_property PACKAGE_PIN K25 [get_ports {USR_LED[0]}]
set_property PACKAGE_PIN K26 [get_ports {USR_LED[1]}]
set_property PACKAGE_PIN P26 [get_ports {USR_LED[2]}]
set_property PACKAGE_PIN R26 [get_ports {USR_LED[3]}]
set_property PACKAGE_PIN N16 [get_ports {USR_LED[4]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USR_LED[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USR_LED[1]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USR_LED[2]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USR_LED[3]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USR_LED[4]}]

#USER LEDS CONNECTED TO A 1.8V VCCO BANK
set_property PACKAGE_PIN J26 [get_ports {USR_LED[5]}]
set_property PACKAGE_PIN H26 [get_ports {USR_LED[6]}]
set_property PACKAGE_PIN E26 [get_ports {USR_LED[7]}]
set_property PACKAGE_PIN A24 [get_ports {USR_LED[8]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USR_LED[5]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USR_LED[6]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USR_LED[7]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USR_LED[8]}]

#USER LED CONNECTED TO A FMC_ADJ VCCO BANK (default config 1.8V)
set_property PACKAGE_PIN F19 [get_ports {USR_LED[9]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USR_LED[9]}]
```

```

#-----
#USER LED over CPLD
# FEX11
set_property PACKAGE_PIN B21 [get_ports {USR_CPLD_LED[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USR_CPLD_LED[0]}]
#-----
#CLK DDR3
#AC9 /AD9 for REV01
#AB11 / AC11 for REV02
##set_property PACKAGE_PIN AB11 [get_ports CLK_DDR3_200MHz_clk_p]
##set_property PACKAGE_PIN AC11 [get_ports CLK_DDR3_200MHz_clk_n]
##set_property IOSTANDARD DIFF_SSTL15 [get_ports CLK_DDR3_200MHz_clk_p]
##set_property IOSTANDARD DIFF_SSTL15 [get_ports CLK_DDR3_200MHz_clk_n]
#-----
#QSPI
set_property PACKAGE_PIN C23 [get_ports {spi_rtl_ss_io[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {spi_rtl_ss_io[0]}]
set_property PACKAGE_PIN B24 [get_ports spi_rtl_io0_io]
set_property PACKAGE_PIN A25 [get_ports spi_rtl_io1_io]
set_property PACKAGE_PIN B22 [get_ports spi_rtl_io2_io]
set_property PACKAGE_PIN A22 [get_ports spi_rtl_io3_io]
set_property IOSTANDARD LVCMOS18 [get_ports spi_rtl_io0_io]
set_property IOSTANDARD LVCMOS18 [get_ports spi_rtl_io1_io]
set_property IOSTANDARD LVCMOS18 [get_ports spi_rtl_io2_io]
set_property IOSTANDARD LVCMOS18 [get_ports spi_rtl_io3_io]
#-----
#IIC to CPLD
set_property PACKAGE_PIN G26 [get_ports SCF_cpld_1_scl]
set_property PACKAGE_PIN F25 [get_ports SCF_cpld_14_oe]
set_property PACKAGE_PIN G25 [get_ports SCF_cpld_16_sda]
set_property IOSTANDARD LVCMOS18 [get_ports SCF_cpld_1_scl]
set_property IOSTANDARD LVCMOS18 [get_ports SCF_cpld_14_oe]
set_property IOSTANDARD LVCMOS18 [get_ports SCF_cpld_16_sda]
#-----
#SI5338 CLKs
set_property PACKAGE_PIN H6 [get_ports {SI_MGT115_0_clk_p[0]}]

set_property PACKAGE_PIN G22 [get_ports {SI_FCLK_clk_p[1]}]
set_property PACKAGE_PIN D23 [get_ports {SI_FCLK_clk_p[2]}]
set_property PACKAGE_PIN G24 [get_ports {SI_FCLK_clk_p[0]}]
set_property IOSTANDARD LVDS_25 [get_ports {SI_FCLK_*}]

```

## **\_i\_pcie.xdc**

```

#-----
# FEX0
set_property PACKAGE_PIN B20 [get_ports {PCI_PERSTN}]
set_property IOSTANDARD LVCMOS18 [get_ports {PCI_PERSTN}]
#-----
set_property PACKAGE_PIN K6 [get_ports {CLK_PCIE_100MHz_clk_p[0]}]
set_property PACKAGE_PIN N4 [get_ports {pcie_7x_mgt_rxp[2]}]
set_property PACKAGE_PIN R4 [get_ports {pcie_7x_mgt_rxp[3]}]
set_property PACKAGE_PIN L4 [get_ports {pcie_7x_mgt_rxp[1]}]
set_property PACKAGE_PIN J4 [get_ports {pcie_7x_mgt_rxp[0]}]

```

#### PCB REV01:

##### \_i\_io\_ddr\_clk.xdc

```
#-----  
#CLK DDR3  
#AC9 /AD9 for REV01  
#AB11 / AC11 for REV02  
set_property PACKAGE_PIN AC9 [get_ports CLK_DDR3_200MHz_clk_p]  
set_property PACKAGE_PIN AD9 [get_ports CLK_DDR3_200MHz_clk_n]  
set_property IOSTANDARD DIFF_SSTL15 [get_ports CLK_DDR3_200MHz_clk_p]  
set_property IOSTANDARD DIFF_SSTL15 [get_ports CLK_DDR3_200MHz_clk_n]
```

#### PCB REV02:

##### \_i\_io\_ddr\_clk.xdc

```
#-----  
#CLK DDR3  
#AC9 /AD9 for REV01  
#AB11 / AC11 for REV02  
set_property PACKAGE_PIN AB11 [get_ports CLK_DDR3_200MHz_clk_p]  
set_property PACKAGE_PIN AC11 [get_ports CLK_DDR3_200MHz_clk_n]  
set_property IOSTANDARD DIFF_SSTL15 [get_ports CLK_DDR3_200MHz_clk_p]  
set_property IOSTANDARD DIFF_SSTL15 [get_ports CLK_DDR3_200MHz_clk_n]
```

## Software Design - SDK/HSI

For SDK project creation, follow instructions from:

[SDK Projects](#)

## Application

Template location: ./sw\_lib/sw\_apps/

### hello\_tef1001

- Xiline Hello World as endless loop

### SI5338\_Init

- SI5338 I2C Configuration example only.

srec\_spi\_bootloader

- modified Xilinx SREC Bootloader, including SI5338 configuration
  - modified Files: blconfig.h, bootloader.c
  - add Files: si5338.h, si5338.c, register\_map.h
  - modified xilisf\_v5\_11: xilisf.mld (default Flash Typ:5)

# Additional Software

## SI5338


File location <design name>/misc/SI5338/RegisterMap.txt

General documentation how you work with these project will be available on [SI5338](#)

# Appx. A: Change History and Legal Notices

## Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
<div><div>Error rendering macro 'page-info'</div><div>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.</div></div>	<div><div>Error rendering macro 'page-info'</div><div>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</div><div><div> Unknown macro: 'metadata'</div></div></div>	<div><div>Error rendering macro 'page-info'</div><div>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.</div></div>	<div><ul style="list-style-type: none"><li>• typo correction part name</li><li>• typo correction on programming chapter</li><li>• note pcie</li></ul></div>

confluence.core. ContentEntityObject]		String, class com.atlassian. confluence.core. ContentEntityObject]	
25 Oct 2018	v.9	John Hartfiel	<ul style="list-style-type: none"> <li>• add -410 assembly variant</li> </ul>
25 Oct 2018	v.8	John Hartfiel	<ul style="list-style-type: none"> <li>• 2018.2 release</li> </ul>
07 Mar 2018	v.6	John Hartfiel	<ul style="list-style-type: none"> <li>• 2017.4 release</li> </ul>
2018-02-08	v.5	John Hartfiel	<ul style="list-style-type: none"> <li>• 2017.2 release</li> </ul>
2017-11-28	v.1	John Hartfiel	<ul style="list-style-type: none"> <li>• initial release</li> </ul>
--	all	<div data-bbox="982 1054 1344 1871"> <p><b>Error rendering macro 'page-info'</b></p> <p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> </div>	--

```
[interface com.atlassian.  
user.User, class java.lang.  
String, class com.atlassian.  
confluence.core.  
ContentEntityObject]
```

Document change history.

## Legal Notices

## Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

## REACH, RoHS and WEEE

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

#### Error rendering macro 'page-info'

Ambiguous method overloading for method `jdk.proxy241.$Proxy3496#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`