TE0726 Zynqberry Demo1

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Overview

Zynq PS Design with Linux Example and Camera Demo.

Refer to http://trenz.org/te0726-info for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2022.2
- RPI Camera 1.3 or 2.1
- HDMI
- PetaLinux
- SD
- ETH
- USB
- I2C
- QSPI programming

Revision History

Date	Vivado	Project Built	Authors	Description
2024-01-18	2022.2	TE0726-zynqberrydemo1_noprebuilt-vivado_2022.2-build_9_20240118115537.zip TE0726-zynqberrydemo1-vivado_2022.2-build_9_20240118115537.zip	Mohsen Chamanbaz	• 2022.2 release
2022-02-23	2020.2	TE0726-zynqberrydemo1_noprebuilt-vivado_2020.2-build_9_20220223125457.zip TE0726-zynqberrydemo1-vivado_2020.2-build_9_20220223125446.zip	Mohsen Chamanbaz /John Hartfiel	• add missing QSPI patch

2021-10-06	2020.2	TE0726-zynqberrydemo1-vivado_2020.2-build_8_20211006090231.zip TE0726-zynqberrydemo1_noprebuilt-vivado_2020.2-build_8_20211006090249.zip	Mohsen Chamanbaz	• 2020.2 release • Audio hardware platform is changed. (Audio formatter, I2S transmitter and I2S receiver) • 0001-QSPI-s25fl127_8-2020_2.patch for restart
2020-04-08	2019.2	TE0726-zynqberrydemo1-vivado_2019.2-build_10_20200408190958.zip TE0726-zynqberrydemo1_noprebuilt-vivado_2019.2-build_10_20200408191010.zip	Mohsen Chamanbaz /John Hartfiel	• changes FSBL flash
2020-03-25	2019.2	TE0726-zynqberrydemo1_noprebuilt-vivado_2019.2-build_8_20200325081403.zip TE0726-zynqberrydemo1-vivado_2019.2-build_8_20200325081354.zip	Mohsen Chamanbaz /John Hartfiel	• script update
2020-02-20	2019.2	TE0726-zynqberrydemo1_noprebuilt-vivado_2019.2-build_5_20200214101503.zip TE0726-zynqberrydemo1-vivado_2019.2-build_5_20200214101453.zip	Mohsen Chamanbaz	• update with Vivado 2019.2
2019-12-19	2018.3	te0726-zynqberrydemo1_noprebuilt-vivado_2018.3-build_10_20200113150027.zip te0726-zynqberrydemo1-vivado_2018.3-build_10_20200113150016.zip	Mohsen Chamanbaz	• update with Vivado 2018.3
2018-11-20	2018.2	te0726-zynqberrydemo1_noprebuilt-vivado_2018.2-build_03_20181120163954.zip te0726-zynqberrydemo1-vivado_2018.2-build_03_20181120163939.zip	Oleksandr Kiyenko	• update petalinux with audio config

2018-11-19	2018.2	te0726-zynqberrydemo1_noprebuilt-vivado_2018.2-build_03_20181119110154.zip te0726-zynqberrydemo1-vivado_2018.2-build_03_20181119110059.zip	Oleksandr Kiyenko	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version

Flash Programming failed with 2020.2	Depending on Flash content Flash programming failed with provided fsbl_flash (Xilinx AR# 76051)2020.x version	• Option1:
		  ○ In case Flash is empty, use fsbl_flash on programming GUI
		  ○ In case Flash is programmed use normal fsbl on programming GUI
		• Option2: use in both case fsbl_flash on programming GUI and Vivado LabTools 2018.3
			--- 	

FSBL/ Kernel Vivado 2020.2	Petalinux does not restart after first booting	use 0001-QSPI-s25fl127_8-2020_2.patch from test_board\os\petalinux\project-spec\meta-user\recipes-kernel\linux\linux-xlnx\	---
Error message during boot "memory reservation failed"	During boot message "ERROR: reserving fdt memory region failed (addr=1fc00000 size=400000)" occures.	No workaround Camera is working, picture can be captured with fbgrab function	---

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2022.2	needed,Vivado is included into Vitis installation
PetaLinux	2022.2	needed

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
~~te0726-01~~	01_64MB	REV01	64MB LPDDR2	16MB	NA	NA	not included, user modifications are needed
~~te0726-03R~~	r_128MB	REV03, REV02	128MB DDR3L	16MB	NA	NA	not included, user modifications are needed
te0726-03M	m_512MB	REV03, REV02	512MB DDR3L	16MB	NA	NA	
te0726-03-07S-1C	7s_512MB	REV03, REV02	512MB DDR3L	16MB	NA	NA	
~~TE0726-03RJ~~	r_128MB	REV03, REV02	128MB	16MB	NA	NA	not included, user modifications are needed
~~TE0726-03-41C74-Q~~	r_128MB	REV03, REV02	128MB	16MB	NA	NA	not included, user modifications are needed
~~TE0726-03-41C74-R~~	r_128MB	REV03, REV02	128MB	16MB	NA	NA	not included, user modifications are needed
TE0726-03IM	mi_512MB	REV03, REV02	512MB	16MB	NA	NA	
TE0726-03-11C64-A	7s_512MB	REV03, REV02	512MB	16MB	NA	NA	
TE0726-03-41I64-A	mi_512MB	REV03, REV02	512MB	16MB	NA	NA	
TE0726-03-41C64-A	m_512MB	REV03, REV02	512MB	16MB	NA	NA	
TE0726-03-S001	m_512MB	REV03	512MB	16MB	NA	NA	
TE0726-03-S002	m_512MB	REV03	512MB	16MB	NA	NA	
TE0726-04-41C94-A*	m_512MB	REV04	512MB	16MB	NA	NA	

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Power	Use USB2.0 or higher for power supply via USB
Micro USB Cable	Connect to USB2 or better USB3 Hub for proper power supply over USB
Raspberry Pi Camera Rev 1.3 or Camera Rev 2.1	Beta-implementation of REV2.1(not complette stable)
Monitor	DELL Model Number: U2412Mc
HDMI Cable	--

Additional Hardware

Content

For general structure and of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Design sources

Additional Sources

Type	Location	Notes
init.sh	<design name>/misc/init_script	Additional Initialization Script for Linux

Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File

BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebult content)

Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0726 "Zynqberry Demo1" Reference Design

Design Flow

> Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

> **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
------------------------Set design paths---------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-------------------------------------------------------------------
------------------------TE Reference
Design--------------------------
-------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
    - (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

    > Note: Select correct one, see also Vivado Board Part Flow

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

```
TE::hw_build_design -export_prebuilt
```

> Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see PetaLinux KICKstart
    - use TE Template from "<project folder>\os\petalinux"
    - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>" . **Note:** HW Export from Vivado GUI creates another path as default workspace.
    - The build images are located in the "<plnx-proj-root>/images/linux" directory
    - For 128MB and 64MB only:Netboot Offset must be reduced manually, see Config
6. Configure the **boot.scr** file as needed, see Distro Boot with Boot.scr
7. Copy PetaLinux build image files to prebuilt folder
    a. Copy **u-boot.elf**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

> "<project folder>\prebuilt\os\petalinux\<DDR size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

b. Generate Programming Files with Vitis

run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or
start with TE Scripts on Vivado TCL)
```

> TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

8. Generate Programming Files with Petalinux (alternative), see PetaLinux KICKstart

Launch

Programming

> Check Module and Carrier TRMs for proper HW configuration before you try any design.
>
> Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select Create and open delivery binary folder

> Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash and **image.ub** and **boot.scr** on **SD** or **USB**.

1. Connect **JTAG** and power on the board
2. Set the dip switch S1 to ON state. (JTAG only mode)

> Note: Dip switch S1 exists only for boards with PCB REV04 or later.

3. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

```
TE::pr_program_flash -swapp u-boot
TE::pr_program_flash -swapp hello_te0726 (optional)
```

4. After programming the QSPI set the dip switch S1 to OFF again. (QSPI boot mode)
5. Copy **image.ub** and **boot.scr** on **SD** or **USB**
   - use files from (<project foler>/_binaries_<Articel Name>)/boot_linux from generated binary folder,see: Get prebuilt boot binaries
   - or use prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
   - Important: Do not copy Boot.bin on SD(is not used see SD note), only other files.
6. Copy init.sh on SD-Card
   - location: <design_name>/misc/sd/
7. Insert SD-Card

SD

Xilinx Zynq devices in CLG225 package do not support SD Card boot directly from ROM bootloader. Use QSPI for primary boot and SD for secondary boot (u-boot)

JTAG

Not used on this Example.

Usage

1. Prepare HW like described in section Programming
2. Connect UART USB (most cases same as JTAG)
3. Insert SD Card with image.ub

> Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.
> The boot options described above describe the common boot processes for this hardware; other boot options are possible.
> For more information see Distro Boot with Boot.scr

4. Power On PCB

   1. Zynq Boot ROM loads FSBL from SD/QSPI into OCM,

   2. FSBL init PS, programs PL using the bitstream and loads U-boot from SD into DDR,

   3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

Linux

1. Open Serial Console (e.g. putty)

- Speed: 115200
- Select COM Port

> Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

2. Linux Console:

```
Auto login is activated. Therefore it is not necessary to give
username and password.
```

> Note: Wait until Linux boot finished

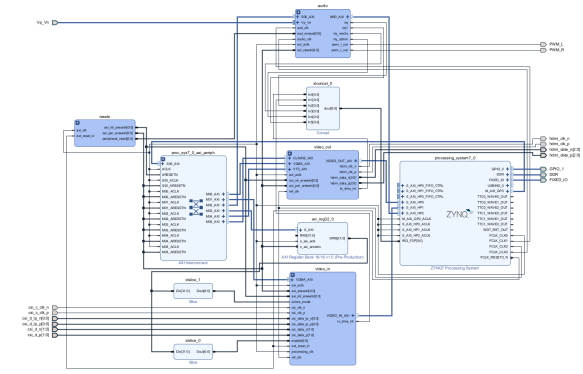
3. You can use a Linux shell now.

```
i2cdetect -y -r 5        (check I2C 1 Bus, Bus 0...5 possible)
udhcpc                                (ETH0 check)
lsusb                                (USB check)
```

4. Camera stream will be enabled via init.sh script on SD
5. Take image from camera (must be enabled with init.sh scripts):
    a. write image to webserver: fbgrab -d /dev/fb0 /srv/www/camera.png
    b. Display image on host PC: http://<ZynqBerry IP>/camera.png

System Design - Vivado

Block Design



Block Design

PS Interfaces

Activated interfaces:

Type	Note
DDR	---
QSPI	MIO
USB0	MIO, ETH over USB
SD1	MIO
UART1	MIO
I2C1	MIO
GPIO	MIO / EMIO
USB RST	MIO
TTC0..1	MIO
WDT	EMIO
AXI HP0..1	

PS Interfaces

Constraints

Basic module constraints

_i_bitgen_common.xdc

```
#
# Common BITGEN related settings for TE0726
#
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
```

Design specific constraint

_i_common.xdc

```
#
#
#
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design
```

_i_te0726.xdc

```
#set_property IOSTANDARD LVCMOS33 [get_ports spdif_tx_o]
#set_property PACKAGE_PIN K15 [get_ports spdif_tx_o]

set_property IOSTANDARD LVCMOS33 [get_ports {GPIO_1_tri_io[*]}]
```

```
# GPIO Pins
# GPIO2
set_property PACKAGE_PIN K15 [get_ports {GPIO_1_tri_io[0]}]
# GPIO3
set_property PACKAGE_PIN J14 [get_ports {GPIO_1_tri_io[1]}]
# GPIO4
set_property PACKAGE_PIN H12 [get_ports {GPIO_1_tri_io[2]}]
# GPIO5
set_property PACKAGE_PIN N14 [get_ports {GPIO_1_tri_io[3]}]
# GPIO6
set_property PACKAGE_PIN R15 [get_ports {GPIO_1_tri_io[4]}]
# GPIO7
set_property PACKAGE_PIN L14 [get_ports {GPIO_1_tri_io[5]}]
# GPIO8
set_property PACKAGE_PIN L15 [get_ports {GPIO_1_tri_io[6]}]
# GPIO9
set_property PACKAGE_PIN J13 [get_ports {GPIO_1_tri_io[7]}]
# GPIO10
set_property PACKAGE_PIN H14 [get_ports {GPIO_1_tri_io[8]}]
# GPIO11
set_property PACKAGE_PIN J15 [get_ports {GPIO_1_tri_io[9]}]
# GPIO12
set_property PACKAGE_PIN M15 [get_ports {GPIO_1_tri_io[10]}]
# GPIO13
set_property PACKAGE_PIN R13 [get_ports {GPIO_1_tri_io[11]}]
# GPIO16
set_property PACKAGE_PIN L13 [get_ports {GPIO_1_tri_io[12]}]
# GPIO17
set_property PACKAGE_PIN G11 [get_ports {GPIO_1_tri_io[13]}]
# GPIO18
set_property PACKAGE_PIN H11 [get_ports {GPIO_1_tri_io[14]}]
# GPIO19
set_property PACKAGE_PIN R12 [get_ports {GPIO_1_tri_io[15]}]
# GPIO20
set_property PACKAGE_PIN M14 [get_ports {GPIO_1_tri_io[16]}]
# GPIO21
set_property PACKAGE_PIN P15 [get_ports {GPIO_1_tri_io[17]}]
# GPIO22
set_property PACKAGE_PIN H13 [get_ports {GPIO_1_tri_io[18]}]
# GPIO23
set_property PACKAGE_PIN J11 [get_ports {GPIO_1_tri_io[19]}]
# GPIO24
set_property PACKAGE_PIN K11 [get_ports {GPIO_1_tri_io[20]}]
# GPIO25
set_property PACKAGE_PIN K13 [get_ports {GPIO_1_tri_io[21]}]
# GPIO26
set_property PACKAGE_PIN L12 [get_ports {GPIO_1_tri_io[22]}]
# GPIO27
set_property PACKAGE_PIN G12 [get_ports {GPIO_1_tri_io[23]}]

## DSI_D0_N
#set_property PACKAGE_PIN F13 [get_ports {GPIO_1_tri_io[24]}]
## DSI_D0_P
#set_property PACKAGE_PIN F14 [get_ports {GPIO_1_tri_io[25]}]
## DSI_D1_N
#set_property PACKAGE_PIN F12 [get_ports {GPIO_1_tri_io[26]}]
## DSI_D1_P
#set_property PACKAGE_PIN E13 [get_ports {GPIO_1_tri_io[27]}]
## DSI_C_N
#set_property PACKAGE_PIN E11 [get_ports {GPIO_1_tri_io[28]}]
## DSI_C_P
```

```
#set_property PACKAGE_PIN E12 [get_ports {GPIO_1_tri_io[29]}]

## CSI_D0_N
#set_property PACKAGE_PIN M11 [get_ports {GPIO_1_tri_io[30]}]
## CSI_D0_P
#set_property PACKAGE_PIN M10 [get_ports {GPIO_1_tri_io[31]}]
## CSI_D1_N
#set_property PACKAGE_PIN P14 [get_ports {GPIO_1_tri_io[32]}]
## CSI_D2_P
#set_property PACKAGE_PIN P13 [get_ports {GPIO_1_tri_io[33]}]
## CSI_C_N
#set_property PACKAGE_PIN N12 [get_ports {GPIO_1_tri_io[34]}]
## CSI_C_P
#set_property PACKAGE_PIN N11 [get_ports {GPIO_1_tri_io[35]}]
## PWM_R
##set_property PACKAGE_PIN N8 [get_ports {GPIO_1_tri_io[36]}]
## PWM_L
##set_property PACKAGE_PIN N7 [get_ports {GPIO_1_tri_io[37]}]

# PWM_R
set_property PACKAGE_PIN N8 [get_ports PWM_R]
# PWM_L
set_property PACKAGE_PIN N7 [get_ports PWM_L]
set_property IOSTANDARD LVCMOS33 [get_ports PWM_*]
```

_i_hdmi.xdc

```
set_property IOSTANDARD TMDS_33 [get_ports hdmi_clk_p]
set_property PACKAGE_PIN R7 [get_ports hdmi_clk_p]

set_property IOSTANDARD TMDS_33 [get_ports {hdmi_data_p[*]}]
set_property PACKAGE_PIN P8 [get_ports {hdmi_data_p[0]}]
set_property PACKAGE_PIN P10 [get_ports {hdmi_data_p[1]}]
set_property PACKAGE_PIN P11 [get_ports {hdmi_data_p[2]}]
```

_i_csi.xdc

```
set_property PACKAGE_PIN N11 [get_ports csi_c_clk_p]
set_property IOSTANDARD LVDS_25 [get_ports csi_c_clk_p]
set_property PACKAGE_PIN M9 [get_ports {csi_d_lp_n[0]}]
set_property IOSTANDARD HSUL_12 [get_ports {csi_d_lp_n[0]}]
set_property PACKAGE_PIN N9 [get_ports {csi_d_lp_p[0]}]
set_property IOSTANDARD HSUL_12 [get_ports {csi_d_lp_p[0]}]
set_property PACKAGE_PIN M10 [get_ports {csi_d_p[0]}]
set_property IOSTANDARD LVDS_25 [get_ports {csi_d_p[0]}]
set_property PACKAGE_PIN P13 [get_ports {csi_d_p[1]}]
set_property IOSTANDARD LVDS_25 [get_ports {csi_d_p[1]}]
set_property INTERNAL_VREF 0.6 [get_iobanks 34]
set_property PULLDOWN true [get_ports {csi_d_lp_p[0]}]
set_property PULLDOWN true [get_ports {csi_d_lp_n[0]}]
# RPI Camera 1
create_clock -period 6.250 -name csi_clk -add [get_ports csi_c_clk_p]
# RPI Camera 2.1
#create_clock -period 1.875 -name csi_clk -add [get_ports csi_c_clk_p]
```

_i_timing.xdc

```
set_property ASYNC_REG true [get_cells {zsys_i/audio/axi_i2s_adi_0/U0/ctrl
/tx_sync/out_data_reg[4]}]
set_property ASYNC_REG true [get_cells {zsys_i/audio/axi_i2s_adi_0/U0/ctrl
/SDATA_O_reg[0]}]
set_false_path -from [get_clocks clk_fpga_0] -to [get_clocks clk_fpga_3]
set_false_path -from [get_clocks clk_fpga_3] -to [get_clocks clk_fpga_0]

set_false_path -from [get_pins {zsys_i/axi_reg32_0/U0
/axi_reg32_v1_0_S_AXI_inst/slv_reg16_reg[1]/C}] -to [get_pins zsys_i
/video_in/axis_raw_demosaic_0/U0/colors_mode_i_reg/D]
set_false_path -from [get_pins zsys_i/video_in/csi_to_axis_0/U0
/lane_align_inst/err_req_reg/C] -to [get_pins zsys_i/video_in
/csi2_d_phy_rx_0/U0/clock_upd_req_reg/D]

set_false_path -from [get_pins {zsys_i/video_in/axi_vdma_0/U0
/I_PRMRY_DATAMOVER/GEN_S2MM_FULL.I_S2MM_FULL_WRAPPER/GEN_INCLUDE_REALIGNER.
I_S2MM_REALIGNER/GEN_INCLUDE_SCATTER.I_S2MM_SCATTER
/sig_max_first_increment_reg[2]/C}] -to [get_pins zsys_i/video_in
/axi_vdma_0/U0/I_PRMRY_DATAMOVER/GEN_S2MM_FULL.I_S2MM_FULL_WRAPPER
/GEN_INCLUDE_REALIGNER.I_S2MM_REALIGNER/GEN_INCLUDE_SCATTER.I_S2MM_SCATTER
/sig_btt_eq_0_reg/D]
set_false_path -from [get_pins {zsys_i/video_in/axi_vdma_0/U0
/I_PRMRY_DATAMOVER/GEN_S2MM_FULL.I_S2MM_FULL_WRAPPER/GEN_INCLUDE_REALIGNER.
I_S2MM_REALIGNER/GEN_INCLUDE_SCATTER.I_S2MM_SCATTER/sig_btt_cntr_dup_reg[1]
/C}] -to [get_pins zsys_i/video_in/axi_vdma_0/U0/I_PRMRY_DATAMOVER
/GEN_S2MM_FULL.I_S2MM_FULL_WRAPPER/GEN_INCLUDE_REALIGNER.I_S2MM_REALIGNER
/GEN_INCLUDE_SCATTER.I_S2MM_SCATTER/sig_btt_eq_0_reg/D]
```

Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis

Application

SDK Template location: ./sw_lib/sw_apps/

zynq_fsbl

TE modified 2022.2 FSBL

General:

- Modified Files:main.c, fsbl_hooks.h/.c (search for 'TE Mod' on source code)
- Add Files: te_fsbl_hooks.h/.c(for hooks and board)\n\
- General Changes:
    - Display FSBL Banner and Device ID

Module Specific:

- Add Files: all TE Files start with te_*
    - enable VTC and VDMA cores for camera access

hello_te0726

Hello TE0726 is a Xilinx Hello World example as endless loop instead of one console output.

u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

For 512MB variant:

- No change

For 64MB variant only:

- CONFIG_SUBSYSTEM_NETBOOT_OFFSET = 0x2000000

For 128MB variant only:

- CONFIG_SUBSYSTEM_NETBOOT_OFFSET = 0x4000000

U-Boot

Start with **petalinux-config -c u-boot**
Changes:

- CONFIG_ENV_IS_NOWHERE=y
- # CONFIG_ENV_IS_IN_SPI_FLASH is not set

Device Tree

```
/include/ "system-conf.dtsi"
/ {
};


/ {

    #address-cells = <1>;
    #size-cells = <1>;

    reserved-memory {
        #address-cells = <1>;
        #size-cells = <1>;
        ranges;
        hdmi_fb_reserved_region@1FC00000 {
            //compatible = "removed-dma-pool";
            compatible = "shared-dma-pool";
            no-map;
            // 512M (M modules)
            reg = <0x1FC00000 0x400000>;
            // 128M (R modules)
            //reg = <0x7C00000 0x400000>;
        };

        // Second framebuffer for direct data streaming from camera to
monitor is not needed.

        //camera_fb_reserved_region@1FC00000 {
        //    //compatible = "removed-dma-pool";
        //    compatible = "shared-dma-pool";
        //    no-map;
        //    // 512M (M modules)
        //    reg = <0x1FC00000 0x400000>;
        //    // 128M (R modules)
        //    //reg = <0x7800000 0x400000>;
        //};

    };

    hdmi_fb: framebuffer@1FC00000 {           // HDMI out
        compatible = "simple-framebuffer";
        // 512M (M modules)
        reg = <0x1FC00000 (1280 * 720 * 4)>;    // 720p
        // 128M (R modules)
        //reg = <0x7C00000 (1280 * 720 * 4)>;   // 720p
        width = <1280>;                         // 720p
        height = <720>;                         // 720p
        stride = <(1280 * 4)>;                  // 720p
        format = "a8b8g8r8";
```

```
        status = "okay";
    };


    //camera_fb: framebuffer@0x1FC00000 {         // CAMERA in
    //    compatible = "simple-framebuffer";
    //    // 512M (M modules)
    //    reg = <0x1FC00000 (1280 * 720 * 4)>;    // 720p
    //    // 128M (R modules)
    //    //reg = <0x7800000 (1280 * 720 * 4)>;   // 720p
    //    width = <1280>;                         // 720p
    //    height = <720>;                         // 720p
    //    stride = <(1280 * 4)>;                  // 720p
    //    format = "a8b8g8r8";
    //};

    vcc_3V3: fixedregulator@0 {
        compatible = "regulator-fixed";
        regulator-name = "vccaux-supply";
        regulator-min-microvolt = <3300000>;
        regulator-max-microvolt = <3300000>;
        regulator-always-on;
    };
};

&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;

        spi-rx-bus-width = <4>;
        spi-tx-bus-width = <4>;

        spi-max-frequency = <50000000>;
        partition@0x00000000 {
            label = "boot";
            reg = <0x00000000 0x00500000>;
        };
        partition@0x00500000 {
            label = "bootenv";
            reg = <0x00500000 0x00020000>;
        };
        partition@0x00520000 {
            label = "kernel";
            reg = <0x00520000 0x00a80000>;
        };
        partition@0x00fa0000 {
            label = "spare";
            reg = <0x00fa0000 0x00000000>;
        };
    };
};

/*
* We need to disable Linux VDMA driver as VDMA
* already configured in FSBL
```

```
*/
&video_in_axi_vdma_0 {
   status = "disabled";
};

&video_out_axi_vdma_0 {
   status = "disabled";
};

&video_out_v_tc_0 {
    //xilinx-vtc: probe of 43c20000.v_tc failed with error -2
    status = "disabled";
};

&gpio0 {
    interrupt-controller;
    #interrupt-cells = <2>;
};

&i2c1 {
    #address-cells = <1>;
    #size-cells = <0>;

    i2cmux0: i2cmux@70  {
        compatible = "nxp,pca9544";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x70>;


        i2c1@0 {
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0>;

            id_eeprom@50 {
                compatible = "atmel,24c32";
                reg = <0x50>;
            };

        };
        i2c1@1 {    // Display Interface Connector
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <1>;
        };
        i2c1@2 {    // HDMI Interface Connector
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <2>;
        };
        i2c1@3 {    // Camera Interface Connector
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <3>;
        };
    };

};

/{
```

```
    usb_phy0: usb_phy@0 {
        compatible = "ulpi-phy";
        #phy-cells = <0>;
        reg = <0xe0002000 0x1000>;
        view-port = <0x0170>;
        drv-vbus;
    };
};

&usb0 {
    usb-phy = <&usb_phy0>;
} ;

/*
* Sound configuration
*/

/{

    /* Use S/PDIF transmitter as codec required by simple-audio-card */
    playback_codec: playback-codec {
        compatible = "linux,spdif-dit";
        #sound-dai-cells = <0>;
    };

    /* Use S/PDIF receiver as codec required by simple-audio-card */
    record_codec: record-codec {
        compatible = "linux,spdif-dir";
        #sound-dai-cells = <0>;
    };
    sound {
        #address-cells = <1>;
        #size-cells = <0>;

        simple-audio-card,widgets =
            "Microphone", "In Jack",
            "Line", "Line In Jack",
            "Line", "Line Out Jack",
            "Headphone", "Out Jack";

        simple-audio-card,routing =
            "Out Jack", "te-out",
            "te-in", "In Jack";

        i2s_receiver_0:i2s_receiver@43C10000 {
           compatible = "xlnx,i2s-receiver-1.0";
           clock-names = "s_axi_ctrl_aclk", "aud_mclk", "m_axis_aud_aclk";
           aud_mclk = <4081632>;
           reg = <0x0 0x43C10000 0x0 0x10000>;
           //xlnx,dwidth = <0x18>;                  //I2S Data Width 24
bit
           xlnx,dwidth = <0x10>;                    //I2S Data Width 16 bit
           xlnx,num-channels = <2>;
           xlnx,snd-pcm = <&audio_formatter_0>;
        };

        i2s_transmitter_0:i2s_transmitter@43C20000 {
             compatible = "xlnx,i2s-transmitter-1.0";
             clock-names = "s_axi_ctrl_aclk", "aud_mclk",
"s_axis_aud_aclk";
             aud_mclk = <4081632>;
```

```
             reg = <0x0 0x43C20000 0x0 0x10000>;
             //xlnx,dwidth = <0x18>;                //I2S Data Width 24 bit
             xlnx,dwidth = <0x10>;                  //I2S Data Width 16 bit
             xlnx,num-channels = <2>;
             xlnx,snd-pcm = <&audio_formatter_0>;
        };

        audio_formatter_0:audio_formatter@43C00000 {
            compatible = "xlnx,audio-formatter-1.0";
            interrupt-names = "irq_mm2s", "irq_s2mm";
            reg = <0x0 0x43C00000 0x0 0x1000>;
            xlnx,tx = <&i2s_transmitter_0>;
            xlnx,rx = <&i2s_receiver_0>;
            clock-names = "s_axi_lite_aclk", "m_axis_mm2s_aclk",
"aud_mclk", "s_axis_s2mm_aclk";
            aud_mclk = <12307691>;
        };
        playback_link: simple-audio-card,dai-link@0 {
            reg = <0>;
            format = "i2s";

            bitclock-master = <&p_codec_dai>;
            frame-master = <&p_codec_dai>;

            p_cpu_dai: cpu {
                sound-dai = <&i2s_transmitter_0>;
            };

            p_platform_dai: plat {
                sound-dai = <&audio_formatter_0>;
            };

            p_codec_dai: codec {
                sound-dai = <&playback_codec>;
            };
        };
        record_link: simple-audio-card,dai-link@1 {
            reg = <1>;
            format = "i2s";

            bitclock-master = <&r_codec_dai>;
            frame-master = <&r_codec_dai>;

            r_cpu_dai: cpu {
                sound-dai = <&i2s_receiver_0>;
            };

            r_platform_dai: plat {
                sound-dai = <&audio_formatter_0>;
            };

            r_codec_dai: codec {
                sound-dai = <&record_codec>;
            };
        };
    };
};



/*
```

```
* We need to disable Linux XADC driver to use XADC for audio recording
*/
&adc {
    status = "disabled";
};
```

Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_MII=y
- CONFIG_XILINX_GMII2RGMII=y
- CONFIG_USB_USBNET=y
- CONFIG_USB_NET_AX8817X=y
- CONFIG_USB_NET_AX88179_178A=y
- CONFIG_USB_NET_CDCETHER=y
- # CONFIG_USB_NET_CDC_EEM is not set
- CONFIG_USB_NET_CDC_NCM=y
- # CONFIG_USB_NET_HUAWEI_CDC_NCM is not set
- # CONFIG_USB_NET_CDC_MBIM is not set
- # CONFIG_USB_NET_DM9601 is not set
- # CONFIG_USB_NET_SR9700 is not set
- # CONFIG_USB_NET_SR9800 is not set
- # CONFIG_USB_NET_SMSC75XX is not set
- CONFIG_USB_NET_SMSC95XX=y
- # CONFIG_USB_NET_GL620A is not set
- CONFIG_USB_NET_NET1080=y
- # CONFIG_USB_NET_PLUSB is not set
- # CONFIG_USB_NET_MCS7830 is not set
- # CONFIG_USB_NET_RNDIS_HOST is not set
- CONFIG_USB_NET_CDC_SUBSET_ENABLE=y
- CONFIG_USB_NET_CDC_SUBSET=y
- # CONFIG_USB_ALI_M5632 is not set
- # CONFIG_USB_AN2720 is not set
- CONFIG_USB_BELKIN=y
- CONFIG_USB_ARMLINUX=y
- # CONFIG_USB_EPSON2888 is not set
- # CONFIG_USB_KC2190 is not set
- CONFIG_USB_NET_ZAURUS=y
- # CONFIG_USB_NET_CX82310_ETH is not set
- # CONFIG_USB_NET_KALMIA is not set
- # CONFIG_USB_NET_QMI_WWAN is not set
- # CONFIG_USB_NET_INT51X1 is not set
- # CONFIG_USB_SIERRA_NET is not set
- # CONFIG_USB_VL600 is not set
- # CONFIG_USB_NET_CH9200 is not set
- # CONFIG_USB_NET_AQC111 is not set
- CONFIG_FB_SIMPLE=y
- # CONFIG_FRAMEBUFFER_CONSOLE is not set
- CONFIG_SND_SIMPLE_CARD_UTILS=y
- CONFIG_SND_SIMPLE_CARD=y
- CONFIG_USBIP_CORE=y
- # CONFIG_USBIP_VHCI_HCD is not set
- # CONFIG_USBIP_HOST is not set
- # CONFIG_USBIP_VUDC is not set
- # CONFIG_USBIP_DEBUG is not set
- CONFIG_SND_SOC_XILINX_I2S=y
- CONFIG_SND_SOC_XILINX_PL_SND_CARD=y
- CONFIG_SND_SOC_HDMI_CODEC=n

- CONFIG_SND_PCM_ELD=y
- CONFIG_SND_PCM_IEC958=n
- CONFIG_SND_SOC_XILINX_AUDIO_FORMATTER=y
- CONFIG_SND_SOC_XILINX_SPDIF=y

Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- CONFIG_i2c-tools=y
- CONFIG_busybox-httpd=y (for web server app)
- CONFIG_packagegroup-petalinux-utils = y (util-linux,cpufrequtils,bridge-utils,mtd-utils,usbutils, pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)
- CONFIG_alsa-plugins = y
- CONFIG_alsa-lib-dev = y
- CONFIG_libasound = y
- CONFIG_alsa-conf-base = y
- CONFIG_alsa-conf = y
- CONFIG_alsa-utils = y
- CONFIG_alsa-utils-aplay = y
- CONFIG_busybox-httpd = y
- CONFIG_util-linux-mount = y
- CONFIG_util-linux-umount = y
- CONFIG_util-linux-mountpoint = y
- CONFIG_linux-blkid = y
- CONFIG_auto-login=y
- CONFIG_ADD_EXTRA_USERS="root:root;petalinux:;"

Applications

startup

Script App to load init.sh from SD Card if available.

See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files

rpicam

Application used to enable and configure Raspbery Pi camera module

See: \os\petalinux\project-spec\meta-user\recipes-apps\rpicam\files

webfwu

Webserver application accemble for Zynq access. Need busybox-httpd

See: \os\petalinux\project-spec\meta-user\recipes-apps\webfwu\files

Additional Software

No additional software is needed.

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null,	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null,	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null,	• 2022.2 release

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2022-02-23	v.27	John Hartfiel	• Add missing design content
2021-10-06	v.26	Mohsen Chamanbaz	• 2020.2 release • Audio hardware platform is changed. • Audio formatter, i2s transmitter and i2s receiver are added. • 0001-QSPI-s25fl127_8-2020_2. patch for restart
2020-06-23	v.20	John Hartfiel	• Typo
2020-04-08	v.18	John Hartfiel	• Design update • Programming issue note
2020-03-25	v.17	John Hartfiel	• Script update
2020-02-20	v.16	Mohsen Chamanbaz	• Vivado 2019.2 release

2020-01-13	v.13	Mohsen Chamanbaz	• Vivado 2018.3 release
2018-11-27	v.12	John Hartfiel	• update documentation
2018-11-20	v.11	John Hartfiel	• update design files
2018-11-19	v.10	John Hartfiel	• 18.2 release
--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null,	--

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Document change history.

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]