TE0726 Zynqberry Demo3

Table of contents

Overview

Zynq PS Design with Linux Example with video and audio configuration.

Refer to http://trenz.org/te0726-info for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2019.2
- RPI Camera 1.3 or 2.1
- VIDEO/AUDIO (plus video/audio player)
- HDMI
- PetaLinux
- SD
- ETH
- USB
- I2C
- Special FSBL for QSPI programming

Revision History

Date	Vivado	Project Built	Authors	Description
2020-03-25	2019.2	TE0726-zynqberrydemo3_noprebuilt-vivado_2019.2-build_8_20200325082001.zip TE0726-zynqberrydemo3-vivado_2019.2-build_8_20200325081946.zip	Mohsen Chamanbaz/John Hartfiel	• script update
2020-02-20	2019.2	TE0726-zynqberrydemo3_noprebuilt-vivado_2019.2-build_5_20200214101637.zip TE0726-zynqberrydemo3-vivado_2019.2-build_5_20200214101624.zip	Mohsen Chamanbaz	• update with Vivado 2019.2
2019-12-19	2018.3	te0726-zynqberrydemo3-vivado_2018.3-build_10_20200114090815.zip te0726-zynqberrydemo3_noprebuilt-vivado_2018.3-build_10_20200114090645.zip	Mohsen Chamanbaz	• update with Vivado 2018.3
2019-02-12	2018.2	te0726-zynqberrydemo3-vivado_2018.2-build_04_20190212141216.zip te0726-zynqberrydemo3_noprebuilt-vivado_2018.2-build_04_20190212141236.zip	Oleksandr Kiyenko	• add missing fgrab in petalinux template
2018-12-05	2018.2	te0726-zynqberrydemo3-vivado_2018.2-build_03_20181128113130.zip te0726-zynqberrydemo3_noprebuilt-vivado_2018.2-build_03_20181128113146.zip	Oleksandr Kiyenko	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version

Flash Programming failed with 19.2	Depending on Flash content Flash programming failed with provided fsbl_flash (Xilinx AR# 70548)2019.2 version	• Option1:
		  ○ In case Flash is empty, use fsbl_flash on programming GUI
		  ○ In case Flash is programmed use normal fsbl on programming GUI
		• Option2: use in both case fsbl_flash on programming GUI and Vivado LabTools 2018.3
			--- 	

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2019.2	needed, Vivado ist included into Vitis installlation
PetaLinux	2019.2	needed

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
~~te0726-01~~	01	REV01	64MB LPDDR2	16MB		not included, user modifications are needed
~~te0726-03r~~	r	REV02, REV03	128MB DDR3L	16MB		not included, user modifications are needed
te0726-03m	m	REV02, REV03	512MB DDR3L	16MB		
te0726-03-07s-1c	7s	REV03	512MB DDR3L	16MB		

Hardware Modules

Design supports following carriers:

Carrier Model	Notes

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Power	Use USB2.0 or higher for power supply via USB
USB Cable	Connect to USB2 or better USB3 Hub for proper power supply over USB
Headphones	--
Raspberry Pi Camera Rev 1.3 or Camera Rev 2.1	Betaimplemenetation of REV2.1(not complette stable)
Monitor	DELL Model Number: U2412Mc

HDMI Cable	--

Additional Hardware

Content

For general structure and of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Design sources

Additional Sources

Type	Location	Notes
init.sh	<design name>/misc/init_script	Additional Initialization Script for Linux

Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebult content)

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0726 "Zynqberry Demo3" Reference Design

Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

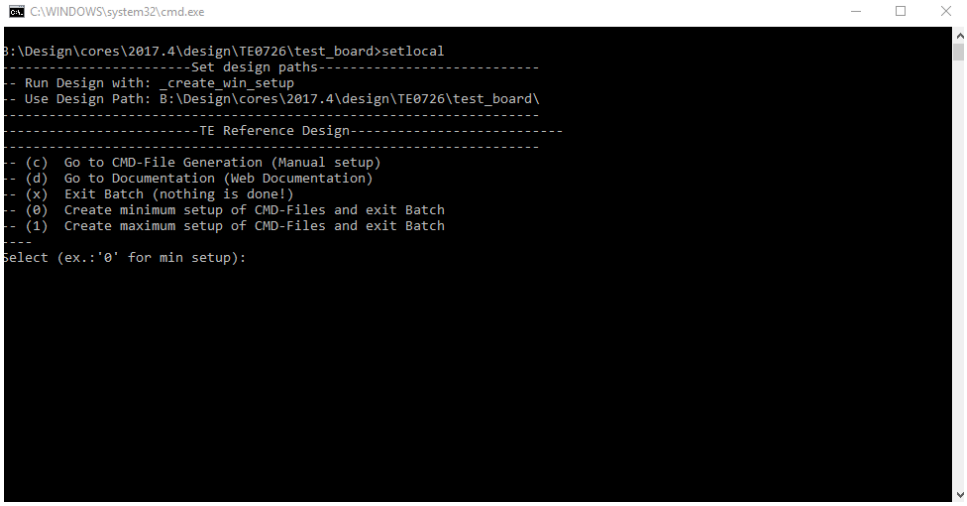
See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
    a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
    Note: Select correct one, see TE Board Part Files
5. Create HDF and export to prebuilt folder
    a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
    Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (uboot.elf and image.ub) with exported XSA
    a. XSA is exported to "prebuilt\hardware\<short name>"
    Note: HW Export from Vivado GUI create another path as default workspace.
    Create Linux images on VM, see PetaLinux KICKstart
        i. Use TE Template from /os/petalinux
        ii. For 128MB and 64MB only:Netboot Offset must be reduced manually, see TE0726 Zynqberry Demo3#Config
7. Add Linux files (uboot.elf and image.ub) to prebuilt folder
    a. "prebuilt\os\petalinux\<DDR size>" or "prebuilt\os\petalinux\<short name>"
    Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise "prebuilt\os\petalinux\\<DDR size>"
8. Generate Programming Files with Vitis

a. Run on Vivado TCL: TE::sw_run_vitis -all
   Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
b. (alternative) Start Vitis with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_vitis
   Note: TCL scripts generate also platform project, this must be done manuelly in case GUI is used. See Vitis

Launch

Programming

> ⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select Create and open delivery binary folder
      Note: Folder (<project foler>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

QSPI

1. Connect JTAG and power module (TE0726 can be powered via JTAG USB or external)
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
   optional "TE::pr_program_flash -swapp hello_te0726" possible
4. Build Image.ub in Petalinux
5. Copy the Petalinux image.ub on SD-Card
   - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
6. Copy init.sh on SD-Card
   - Location : <design-name>/misc/sd/
7. Insert SD-Card

SD

Xilinx Zynq devices in CLG225 package do not support SD Card boot directly from ROM bootloader. Use QSPI for primary boot and SD for secondary boot (u-boot)

JTAG

Not used on this Example.

Usage

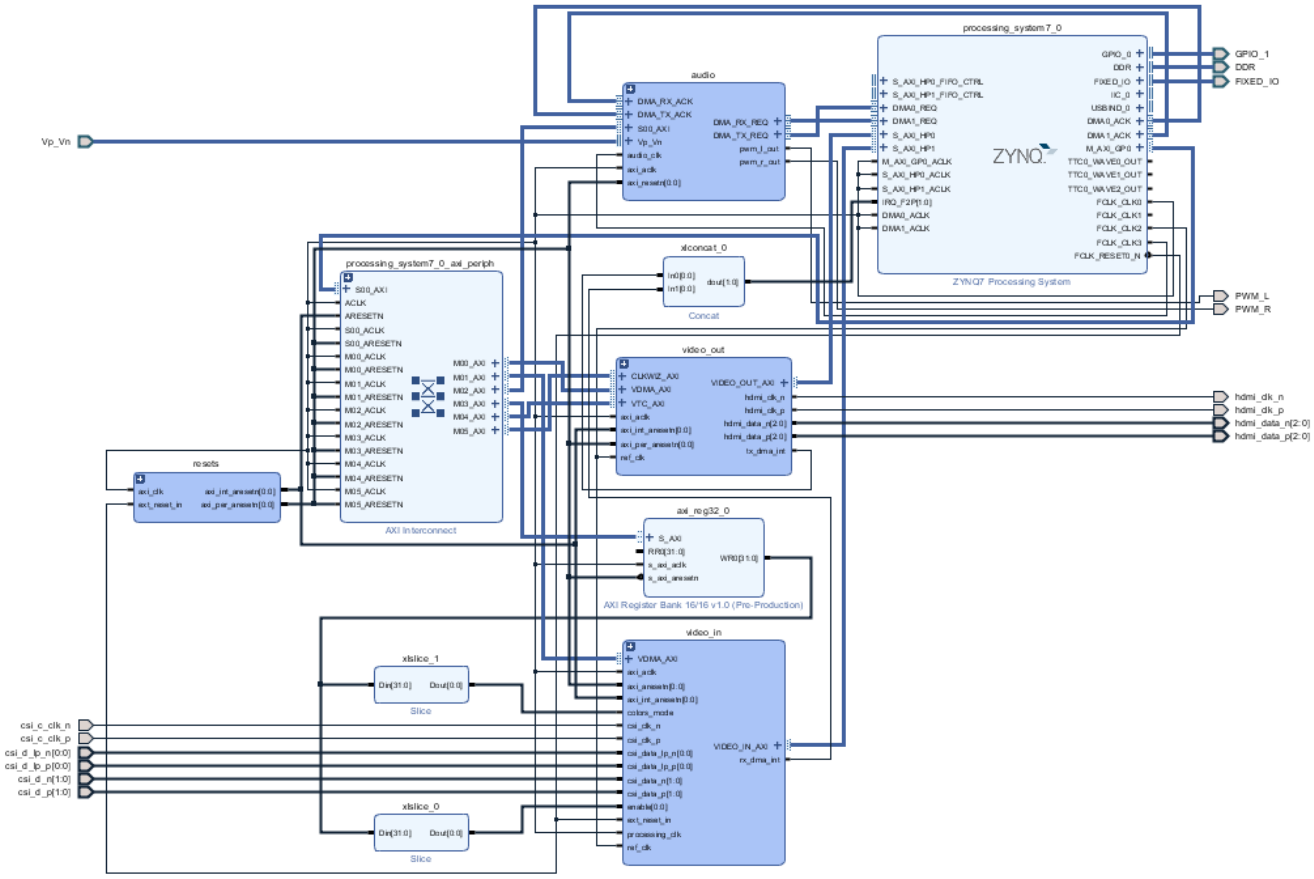
1. Prepare HW like described in section TE0726 Zynqberry Demo3#Programming
2. Connect UART USB (most cases same as JTAG)
3. Insert SD Card with image.ub
4. Power On PCB
   Note: 1. Zynq Boot ROM loads FSBL from QSPI into OCM, 2. FSBL loads U-boot from QSPI into DDR, 3. U-boot load Linux from SD into DDR

Linux

1. Open Serial Console (e.g. putty)
    a. Speed: 115200
    b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
    a. User Name: root
    b. Password: root
       Note: Wait until Linux boot finished For Linux Login use:
        i. User Name: root
        ii. Password: root
3. You can use a Linux shell now.
    a. I2C 1 Bus type: i2cdetect -y -r 5
       Bus 0...5 possible
    b. ETH0 works with udhcpc
    c. USB: insert USB device
4. Start Video with "play <video file>"
    a. "play" is alias to ffmpeg with some parameters for video and audio, type "alias" to see configuration
    b. for videos with higher resolution, disable audio on ffmpeg configuration
5. Start Audio with "aplay <audio files>"
6. Take image from camera (must be enabled with init.sh scripts):
    a. write image to webserver: fbgrab -d /dev/fb1 /srv/www/camera.png
    b. Display image on host PC: http://<ZynqBerry IP>/camera.png

System Design - Vivado

Block Design



Block Design

PS Interfaces

Activated interfaces:

Type	Note
DDR	---
QSPI	MIO
USB0	MIO, ETH over USB
SD1	MIO
UART1	MIO
I2C0	EMIO
I2C1	MIO
GPIO	MIO / EMIO
USB RST	MIO
TTC0..1	MIO
WDT	MIO
AXI HP0..1	
DMA0..1	

PS Interfaces

Constraints

Basic module constraints

_i_bitgen_common.xdc

```
#
# Common BITGEN related settings for TE0726
#
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design]
```

Design specific constraint

_i_common.xdc

```
#
#
#
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design]
```

_i_te0726.xdc

```
#set_property IOSTANDARD LVCMOS33 [get_ports spdif_tx_o]
#set_property PACKAGE_PIN K15 [get_ports spdif_tx_o]

set_property IOSTANDARD LVCMOS33 [get_ports {GPIO_1_tri_io[*]}]
# GPIO Pins
# GPIO2
set_property PACKAGE_PIN K15 [get_ports {GPIO_1_tri_io[0]}]
# GPIO3
set_property PACKAGE_PIN J14 [get_ports {GPIO_1_tri_io[1]}]
# GPIO4
set_property PACKAGE_PIN H12 [get_ports {GPIO_1_tri_io[2]}]
# GPIO5
set_property PACKAGE_PIN N14 [get_ports {GPIO_1_tri_io[3]}]
# GPIO6
set_property PACKAGE_PIN R15 [get_ports {GPIO_1_tri_io[4]}]
# GPIO7
set_property PACKAGE_PIN L14 [get_ports {GPIO_1_tri_io[5]}]
# GPIO8
set_property PACKAGE_PIN L15 [get_ports {GPIO_1_tri_io[6]}]
# GPIO9
set_property PACKAGE_PIN J13 [get_ports {GPIO_1_tri_io[7]}]
# GPIO10
set_property PACKAGE_PIN H14 [get_ports {GPIO_1_tri_io[8]}]
# GPIO11
set_property PACKAGE_PIN J15 [get_ports {GPIO_1_tri_io[9]}]
# GPIO12
set_property PACKAGE_PIN M15 [get_ports {GPIO_1_tri_io[10]}]
# GPIO13
set_property PACKAGE_PIN R13 [get_ports {GPIO_1_tri_io[11]}]
# GPIO16
set_property PACKAGE_PIN L13 [get_ports {GPIO_1_tri_io[12]}]
# GPIO17
set_property PACKAGE_PIN G11 [get_ports {GPIO_1_tri_io[13]}]
# GPIO18
set_property PACKAGE_PIN H11 [get_ports {GPIO_1_tri_io[14]}]
# GPIO19
set_property PACKAGE_PIN R12 [get_ports {GPIO_1_tri_io[15]}]
# GPIO20
set_property PACKAGE_PIN M14 [get_ports {GPIO_1_tri_io[16]}]
# GPIO21
set_property PACKAGE_PIN P15 [get_ports {GPIO_1_tri_io[17]}]
# GPIO22
set_property PACKAGE_PIN H13 [get_ports {GPIO_1_tri_io[18]}]
# GPIO23
set_property PACKAGE_PIN J11 [get_ports {GPIO_1_tri_io[19]}]
# GPIO24
set_property PACKAGE_PIN K11 [get_ports {GPIO_1_tri_io[20]}]
# GPIO25
```

```
set_property PACKAGE_PIN K13 [get_ports {GPIO_1_tri_io[21]}]
# GPIO26
set_property PACKAGE_PIN L12 [get_ports {GPIO_1_tri_io[22]}]
# GPIO27
set_property PACKAGE_PIN G12 [get_ports {GPIO_1_tri_io[23]}]

## DSI_D0_N
#set_property PACKAGE_PIN F13 [get_ports {GPIO_1_tri_io[24]}]
## DSI_D0_P
#set_property PACKAGE_PIN F14 [get_ports {GPIO_1_tri_io[25]}]
## DSI_D1_N
#set_property PACKAGE_PIN F12 [get_ports {GPIO_1_tri_io[26]}]
## DSI_D1_P
#set_property PACKAGE_PIN E13 [get_ports {GPIO_1_tri_io[27]}]
## DSI_C_N
#set_property PACKAGE_PIN E11 [get_ports {GPIO_1_tri_io[28]}]
## DSI_C_P
#set_property PACKAGE_PIN E12 [get_ports {GPIO_1_tri_io[29]}]

## CSI_D0_N
#set_property PACKAGE_PIN M11 [get_ports {GPIO_1_tri_io[30]}]
## CSI_D0_P
#set_property PACKAGE_PIN M10 [get_ports {GPIO_1_tri_io[31]}]
## CSI_D1_N
#set_property PACKAGE_PIN P14 [get_ports {GPIO_1_tri_io[32]}]
## CSI_D2_P
#set_property PACKAGE_PIN P13 [get_ports {GPIO_1_tri_io[33]}]
## CSI_C_N
#set_property PACKAGE_PIN N12 [get_ports {GPIO_1_tri_io[34]}]
## CSI_C_P
#set_property PACKAGE_PIN N11 [get_ports {GPIO_1_tri_io[35]}]
## PWM_R
##set_property PACKAGE_PIN N8 [get_ports {GPIO_1_tri_io[36]}]
## PWM_L
##set_property PACKAGE_PIN N7 [get_ports {GPIO_1_tri_io[37]}]

# PWM_R
set_property PACKAGE_PIN N8 [get_ports PWM_R]
# PWM_L
set_property PACKAGE_PIN N7 [get_ports PWM_L]
set_property IOSTANDARD LVCMOS33 [get_ports PWM_*]
```

_i_hdmi.xdc

```
set_property IOSTANDARD TMDS_33 [get_ports hdmi_clk_p]
set_property PACKAGE_PIN R7 [get_ports hdmi_clk_p]

set_property IOSTANDARD TMDS_33 [get_ports {hdmi_data_p[*]}]
set_property PACKAGE_PIN P8 [get_ports {hdmi_data_p[0]}]
set_property PACKAGE_PIN P10 [get_ports {hdmi_data_p[1]}]
set_property PACKAGE_PIN P11 [get_ports {hdmi_data_p[2]}]
```

_i_csi.xdc

```
set_property PACKAGE_PIN N11 [get_ports csi_c_clk_p]
set_property IOSTANDARD LVDS_25 [get_ports csi_c_clk_p]
set_property PACKAGE_PIN M9 [get_ports {csi_d_lp_n[0]}]
set_property IOSTANDARD HSUL_12 [get_ports {csi_d_lp_n[0]}]
set_property PACKAGE_PIN N9 [get_ports {csi_d_lp_p[0]}]
set_property IOSTANDARD HSUL_12 [get_ports {csi_d_lp_p[0]}]
set_property PACKAGE_PIN M10 [get_ports {csi_d_p[0]}]
set_property IOSTANDARD LVDS_25 [get_ports {csi_d_p[0]}]
set_property PACKAGE_PIN P13 [get_ports {csi_d_p[1]}]
set_property IOSTANDARD LVDS_25 [get_ports {csi_d_p[1]}]
set_property INTERNAL_VREF 0.6 [get_iobanks 34]
set_property PULLDOWN true [get_ports {csi_d_lp_p[0]}]
set_property PULLDOWN true [get_ports {csi_d_lp_n[0]}]
# RPI Camera 1
create_clock -period 6.250 -name csi_clk -add [get_ports csi_c_clk_p]
# RPI Camera 2.1
#create_clock -period 1.875 -name csi_clk -add [get_ports csi_c_clk_p]
```

_i_timing.xdc

```
set_property ASYNC_REG true [get_cells {zsys_i/audio/axi_i2s_adi_0/U0/ctrl/tx_sync/out_data_reg[4]}]
set_property ASYNC_REG true [get_cells {zsys_i/audio/axi_i2s_adi_0/U0/ctrl/SDATA_O_reg[0]}]
set_false_path -from [get_clocks clk_fpga_0] -to [get_clocks clk_fpga_3]
set_false_path -from [get_clocks clk_fpga_3] -to [get_clocks clk_fpga_0]

set_false_path -from [get_pins {zsys_i/axi_reg32_0/U0/axi_reg32_v1_0_S_AXI_inst/slv_reg16_reg[1]/C}] -to
[get_pins zsys_i/video_in/axis_raw_demosaic_0/U0/colors_mode_i_reg/D]
set_false_path -from [get_pins zsys_i/video_in/csi_to_axis_0/U0/lane_align_inst/err_req_reg/C] -to [get_pins
zsys_i/video_in/csi2_d_phy_rx_0/U0/clock_upd_req_reg/D]

set_false_path -from [get_pins {zsys_i/video_in/axi_vdma_0/U0/I_PRMRY_DATAMOVER/GEN_S2MM_FULL.
I_S2MM_FULL_WRAPPER/GEN_INCLUDE_REALIGNER.I_S2MM_REALIGNER/GEN_INCLUDE_SCATTER.I_S2MM_SCATTER
/sig_max_first_increment_reg[2]/C}] -to [get_pins zsys_i/video_in/axi_vdma_0/U0/I_PRMRY_DATAMOVER/GEN_S2MM_FULL.
I_S2MM_FULL_WRAPPER/GEN_INCLUDE_REALIGNER.I_S2MM_REALIGNER/GEN_INCLUDE_SCATTER.I_S2MM_SCATTER/sig_btt_eq_0_reg
/D]
set_false_path -from [get_pins {zsys_i/video_in/axi_vdma_0/U0/I_PRMRY_DATAMOVER/GEN_S2MM_FULL.
I_S2MM_FULL_WRAPPER/GEN_INCLUDE_REALIGNER.I_S2MM_REALIGNER/GEN_INCLUDE_SCATTER.I_S2MM_SCATTER
/sig_btt_cntr_dup_reg[1]/C}] -to [get_pins zsys_i/video_in/axi_vdma_0/U0/I_PRMRY_DATAMOVER/GEN_S2MM_FULL.
I_S2MM_FULL_WRAPPER/GEN_INCLUDE_REALIGNER.I_S2MM_REALIGNER/GEN_INCLUDE_SCATTER.I_S2MM_SCATTER/sig_btt_eq_0_reg
/D]
```

Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis

Application

SDK template in ./sw_lib/sw_apps/ available.

zynq_fsbl

TE modified 2019.2 FSBL

General:

- Modified Files:main.c, fsbl_hooks.h/.c (search for 'TE Mod' on source code)
- Add Files: te_fsbl_hooks.h/.c(for hooks and board)\n\
- General Changes:
    - Display FSBL Banner and Device ID

Module Specific:

- Add Files: all TE Files start with te_*
    - enable VTC and VDMA cores for debian desktop

zynq_fsbl_flash

TE modified 2019.2 FSBL

General:

- Modified Files: main.c
- General Changes:
    - Display FSBL Banner
    - Set FSBL Boot Mode to JTAG
    - Disable Memory initialisation

hello_te0726

Hello TE0726 is a Xilinx Hello World example as an endless loop instead of one console output and TE FSBL screen on HDMI Monitor.

u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

For 64MB variant only:

- CONFIG_SUBSYSTEM_NETBOOT_OFFSET = 0x2000000

For 128MB variant only:

- CONFIG_SUBSYSTEM_NETBOOT_OFFSET = 0x4000000

U-Boot

Start with **petalinux-config -c u-boot**
Changes:

- CONFIG_ENV_IS_NOWHERE=y
- # CONFIG_ENV_IS_IN_SPI_FLASH is not set

Device Tree

```
/include/ "system-conf.dtsi"
/ {
};


/ {
    #address-cells = <1>;
    #size-cells = <1>;

    reserved-memory {
        #address-cells = <1>;
        #size-cells = <1>;
        ranges;
        hdmi_fb_reserved_region@1FC00000 {
            compatible = "removed-dma-pool";
            no-map;
            // 512M (M modules)
            reg = <0x1FC00000 0x400000>;
            // 128M (R modules)
            //reg = <0x7C00000 0x400000>;
        };
        camera_fb_reserved_region@1F800000 {
            compatible = "removed-dma-pool";
            no-map;
            // 512M (M modules)
            reg = <0x1F800000 0x400000>;
            // 128M (R modules)
            //reg = <0x7800000 0x400000>;
        };

    };

    hdmi_fb: framebuffer@0x1FC00000 {           // HDMI out
        compatible = "simple-framebuffer";
        // 512M (M modules)
        reg = <0x1FC00000 (1280 * 720 * 4)>;    // 720p
        // 128M (R modules)
        //reg = <0x7C00000 (1280 * 720 * 4)>;   // 720p
        width = <1280>;                         // 720p
        height = <720>;                         // 720p
        stride = <(1280 * 4)>;                  // 720p
        format = "a8b8g8r8";
        status = "okay";
    };

    camera_fb: framebuffer@0x1F800000 {         // CAMERA in
```

```
        compatible = "simple-framebuffer";
        // 512M (M modules)
        reg = <0x1F800000 (1280 * 720 * 4)>;    // 720p
        // 128M (R modules)
        //reg = <0x7800000 (1280 * 720 * 4)>;   // 720p
        width = <1280>;                         // 720p
        height = <720>;                         // 720p
        stride = <(1280 * 4)>;                  // 720p
        format = "a8b8g8r8";
    };

    vcc_3V3: fixedregulator@0 {
        compatible = "regulator-fixed";
        regulator-name = "vccaux-supply";
        regulator-min-microvolt = <3300000>;
        regulator-max-microvolt = <3300000>;
        regulator-always-on;
    };
};

&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
        spi-max-frequency = <50000000>;
        partition@0x00000000 {
            label = "boot";
            reg = <0x00000000 0x00500000>;
        };
        partition@0x00500000 {
            label = "bootenv";
            reg = <0x00500000 0x00020000>;
        };
        partition@0x00520000 {
            label = "kernel";
            reg = <0x00520000 0x00a80000>;
        };
        partition@0x00fa0000 {
            label = "spare";
            reg = <0x00fa0000 0x00000000>;
        };
    };
};

/*
* We need to disable Linux VDMA driver as VDMA
* already configured in FSBL
*/
&video_in_axi_vdma_0 {
   status = "disabled";
};

&video_out_axi_vdma_0 {
   status = "disabled";
};
```

```
&video_out_v_tc_0 {
    //xilinx-vtc: probe of 43c20000.v_tc failed with error -2
    status = "disabled";
};

&gpio0 {
    interrupt-controller;
    #interrupt-cells = <2>;
};

&i2c1 {
    #address-cells = <1>;
    #size-cells = <0>;

    i2cmux0: i2cmux@70  {
        compatible = "nxp,pca9544";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x70>;


        i2c1@0 {
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0>;

            id_eeprom@50 {
                compatible = "atmel,24c32";
                reg = <0x50>;
            };

        };
        i2c1@1 {    // Display Interface Connector
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <1>;
        };
        i2c1@2 {    // HDMI Interface Connector
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <2>;
        };
        i2c1@3 {    // Camera Interface Connector
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <3>;
        };
    };

};

/{
    usb_phy0: usb_phy@0 {
        compatible = "ulpi-phy";
        #phy-cells = <0>;
        reg = <0xe0002000 0x1000>;
        view-port = <0x0170>;
        drv-vbus;
    };
};
```

```
&usb0 {
    usb-phy = <&usb_phy0>;
} ;

/*
* Sound configuration
*/

/{
    // Custom driver based on spdif-transmitter
    te_audio: dummy_codec_te {
        compatible = "te,te-audio";
        #sound-dai-cells = <0>;
    };

    // Simple Audio Card from AXI_I2S and custom XADC audio input and
    // PWM audio output cores
    sound {
        compatible = "simple-audio-card";
        simple-audio-card,name = "TE0726-PWM-Audio";
        simple-audio-card,format = "i2s";
        simple-audio-card,widgets =
            "Microphone", "In Jack",
            "Line", "Line In Jack",
            "Line", "Line Out Jack",
            "Headphone", "Out Jack";

        simple-audio-card,routing =
            "Out Jack", "te-out",
            "te-in", "In Jack";

        simple-audio-card,cpu {
            sound-dai = <&audio_axi_i2s_adi_0>;
        };
        simple-audio-card,codec {
            sound-dai = <&te_audio>;
        };
    };
};

&audio_axi_i2s_adi_0 {
    compatible = "adi,axi-i2s-1.00.a";
    reg = <0x43c00000 0x1000>;
    clocks = <&clkc 15>, <&clkc 18>; // FCLK_CLK0, FCLK_CLK3
    clock-names = "axi", "ref";
    dmas = <&dmac_s 0 &dmac_s 1>;
    dma-names = "tx", "rx";
    #sound-dai-cells = <0>;
};

/*
* We need to disable Linux XADC driver to use XADC for audio recording
*/
&adc {
    status = "disabled";
};
```

Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_XILINX_GMII2RGMII=y
- CONFIG_USB_USBNET=y
- CONFIG_USB_NET_AX8817X=y
- CONFIG_USB_NET_AX88179_178A=y
- CONFIG_USB_NET_CDCETHER=y
- # CONFIG_USB_NET_CDC_EEM is not set
- CONFIG_USB_NET_CDC_NCM=y
- # CONFIG_USB_NET_HUAWEI_CDC_NCM is not set
- # CONFIG_USB_NET_CDC_MBIM is not set
- # CONFIG_USB_NET_DM9601 is not set
- # CONFIG_USB_NET_SR9700 is not set
- # CONFIG_USB_NET_SR9800 is not set
- # CONFIG_USB_NET_SMSC75XX is not set
- CONFIG_USB_NET_SMSC95XX=y
- # CONFIG_USB_NET_GL620A is not set
- CONFIG_USB_NET_NET1080=y
- # CONFIG_USB_NET_PLUSB is not set
- # CONFIG_USB_NET_MCS7830 is not set
- # CONFIG_USB_NET_RNDIS_HOST is not set
- CONFIG_USB_NET_CDC_SUBSET_ENABLE=y
- CONFIG_USB_NET_CDC_SUBSET=y
- # CONFIG_USB_ALI_M5632 is not set
- # CONFIG_USB_AN2720 is not set
- CONFIG_USB_BELKIN=y
- CONFIG_USB_ARMLINUX=y
- # CONFIG_USB_EPSON2888 is not set
- # CONFIG_USB_KC2190 is not set
- CONFIG_USB_NET_ZAURUS=y
- # CONFIG_USB_NET_CX82310_ETH is not set
- # CONFIG_USB_NET_KALMIA is not set
- # CONFIG_USB_NET_QMI_WWAN is not set
- # CONFIG_USB_NET_INT51X1 is not set
- # CONFIG_USB_SIERRA_NET is not set
- # CONFIG_USB_VL600 is not set
- # CONFIG_USB_NET_CH9200 is not set
- CONFIG_USBIP_CORE=y
- # CONFIG_USBIP_VHCI_HCD is not set
- # CONFIG_USBIP_HOST is not set
- # CONFIG_USBIP_VUDC is not set
- # CONFIG_USBIP_DEBUG is not set
- CONFIG_FB_SIMPLE=y
- CONFIG_SND_SIMPLE_CARD_UTILS=y
- CONFIG_SND_SIMPLE_CARD=y
- # CONFIG_FRAMEBUFFER_CONSOLE is not set

Rootfs

Start with **petalinux-config -c rootfs**

Avtivate:

- i2c-tools
- alsa-plugins
- alsa-lib-dev
- libasound
- alsa-conf-base
- alsa-conf
- alsa-utils
- alsa-utils-aplay
- busybox-httpd

Applications

startup

Script App to load init.sh from SD Card if available.

See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files

rpicam

Application used to enable and configure Raspbery Pi camera module

See: \os\petalinux\project-spec\meta-user\recipes-apps\rpicam\files

fbgrab

Application used to take screenshot from camera

See: \os\petalinux\project-spec\meta-user\recipes-apps\fgrab

webfwu

Webserver application accemble for Zynq access. Need busybox-httpd

See: \os\petalinux\project-spec\meta-user\recipes-apps\webfwu\files

Kernel Modules

te-audio-codec

Simple module stab to use audio interface.

See: \os\petalinux\project-spec\meta-user\recipes-modules\te-audio-codec\files

Additional Software

No additional software is needed.

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• typo • Programming issue note
2020-03-25	v.14	John Hartfiel	• script update
2020-02-20	v.13	Mohsen Chamanbaz	• Vivado 2019.2 release
2020-01-14	v.11	Mohsen Chamanbaz	• Vivado 2018.3 release
2019-02-12	v.10	John Hartfiel	• design linux source update

2018-12-05	v.7	John Hartfiel	• Vivado 2018.2 release
--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	--

Document change history.

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]