

TE0841 IBERT

Table of contents

Error rendering macro 'toc'

java.lang.RuntimeException: com.ctc.wstx.exc.WstxParsingException: String '--' not allowed in comment (missing '>?') at [row,col {unknown-source}]: [39,-1115]

Overview

Example show, how to reconfigure SI5338 with MCS and monitor CLK. Additional MicroBlaze is add for Hello TE0741 example.

Key Features

- MGT
- SI5338 initialisation with MCS

Revision History

Date	Vivado	Project Built	Authors	Description
2018-06-22	2017.4	TE0841-IBERT_noprebuilt-vivado_2017.4-build_11_20180622140813.zip TE0841-IBERT-vivado_2017.4-build_11_20180622140615.zip	John Hartfiel	<ul style="list-style-type: none">• REV02 Board parts• new SI5338 configuration (default REV02)• change xilisf_v5_9 for N25Q512A11G1240E support• Some changes on block design
2018-06-05	2017.4	TE0841-IBERT_noprebuilt-vivado_2017.4-build_10_20180605143852.zip TE0841-IBERT-vivado_2017.4-build_10_20180605143837.zip	John Hartfiel	<ul style="list-style-type: none">• initial release

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
PCB REV01 only: IBERT no CLK	PCB REV01 SI5338 is not preprogrammed and SI programming over MCS is disabled by default design and I2C is not connected	Load test_board bitfile for REV01 and load IBERT design again without power off HW	---

Requirements

Software

Software	Version	Note
Vivado	2017.4	needed
SDK	2017.4	needed

Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0841-01-035-1C	01_35_1c	REV01	2x 512MB DDR4	32MB	---	
TE0841-01-035-1I	01_35_1i	REV01	2x 512MB DDR4	32MB	---	
TE0841-01-035-2I	01_35_2i	REV01	2x 512MB DDR4	32MB	---	
TE0841-01-040-1C	01_40_1c	REV01	2x 512MB DDR4	32MB	---	Serial number 512479 up tp 512474 has same 64MB Flash like REV02
TE0841-01-040-1I	01_40_1i	REV01	2x 512MB DDR4	32MB	---	
TE0841-01-040-2I	01_40_2i	REV01	2x 512MB DDR4	32MB	---	
TE0841-02-035-1C	02_35_1c	REV02	2x 1GB DDR4	64MB	---	
TE0841-02-035-1I	02_35_1i	REV02	2x 1GB DDR4	64MB	---	
TE0841-02-035-2I	02_35_2i	REV02	2x 1GB DDR4	64MB	---	
TE0841-02-040-1C	02_40_1c	REV02	2x 1GB DDR4	64MB	---	
TE0841-02-040-1I	02_40_1i	REV02	2x 1GB DDR4	64MB	---	
TE0841-02-040-1IL	02_40_1i	REV02	2x 1GB DDR4	64MB	low profile B2B connector	

Design supports following carriers:

Carrier Model	Notes
TEBA0841	used as reference carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI
Heat sink	It's recommended to use heat sink for this design

Content

For general structure and of the reference design, see [Project Delivery - AMD devices](#)

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib <design name>/firmware	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI

Additional Sources

Type	Location	Notes
SI5338 Project	\misc\SI5338	

Prebuilt

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0841 "IBERT" Reference Design](#)

Design Flow



Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

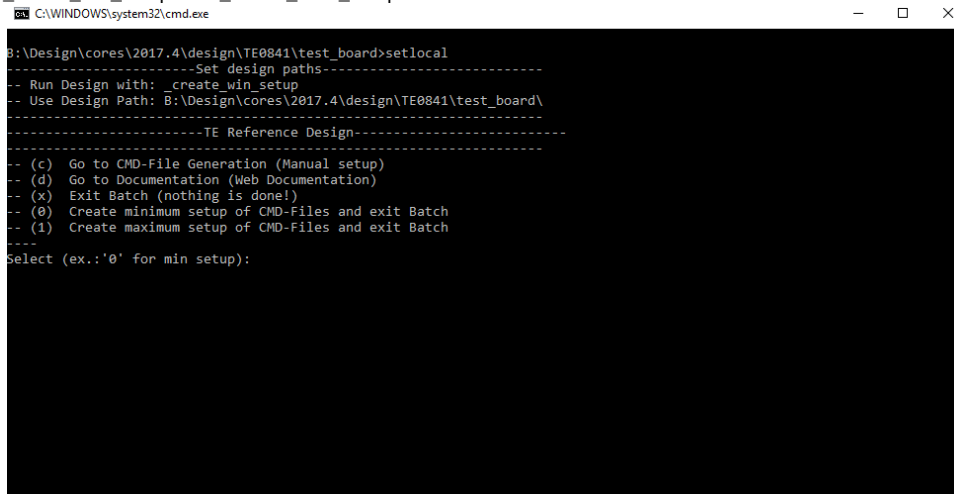
See also: [AMD Development Tools#XilinxSoftware-BasicUserGuides](#)

- [AMD Development Tools#XilinxSoftware-BasicUserGuides](#)
- [Vivado Projects - TE Reference Design](#)
- [Project Delivery](#).

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



```
C:\WINDOWS\system32\cmd.exe
B:\Design\cores\2017.4\design\TE0841\test_board>setlocal
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: B:\Design\cores\2017.4\design\TE0841\test_board\
-----TE Reference Design-----
-- (c) Go to CMD-File Generation (Manual setup)
-- (d) Go to Documentation (Web Documentation)
-- (x) Exit Batch (nothing is done!)
-- (0) Create minimum setup of CMD-Files and exit Batch
-- (1) Create maximum setup of CMD-Files and exit Batch
-----
Select (ex.: '0' for min setup):
```

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
 - a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_gui mode.cmd"Note: Select correct one, see [TE Board Part Files](#)
5. Create HDF and export to prebuilt folder
 - a. Run on Vivado TCL: TE::hw_build_design -export_prebuiltNote: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate MCS Firmware (optional):
 - a. Create SDK Project with TE Scripts on Vivado TCL: TE::sw_run_sdk
 - b. Create "SCU" applicationNote: Select MCS Microblaze and SCU Application
- c. Select Release Built
- d. Regenerate App
7. (optional) Copy "\\workspace\sdk\scu\Release\scu.elf" into "firmware\microblaze_mcs_0"
8. Regenerate Vivado Project or Update Bitfile only and "scu.elf"
9. Copy MCS file with Bitfile into prebuilt folder
 - a. Create SDK Project with TE Scripts on Vivado TCL: TE::sw_run_hsi

Launch

Programming



Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](#)

QSPI

1. Connect JTAG and power on PCB
2. (if not done) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_gui mode.cmd" or open with "vivado_open_project_gui mode.cmd", if generated.
3. Type on Vivado Console: TE::pr_program_flash_mcsfile -swapp
Note: Alternative use SDK or setup Flash on Vivado manually
4. Reboot (if not done automatically)

SD

Not used on this Example.

JTAG

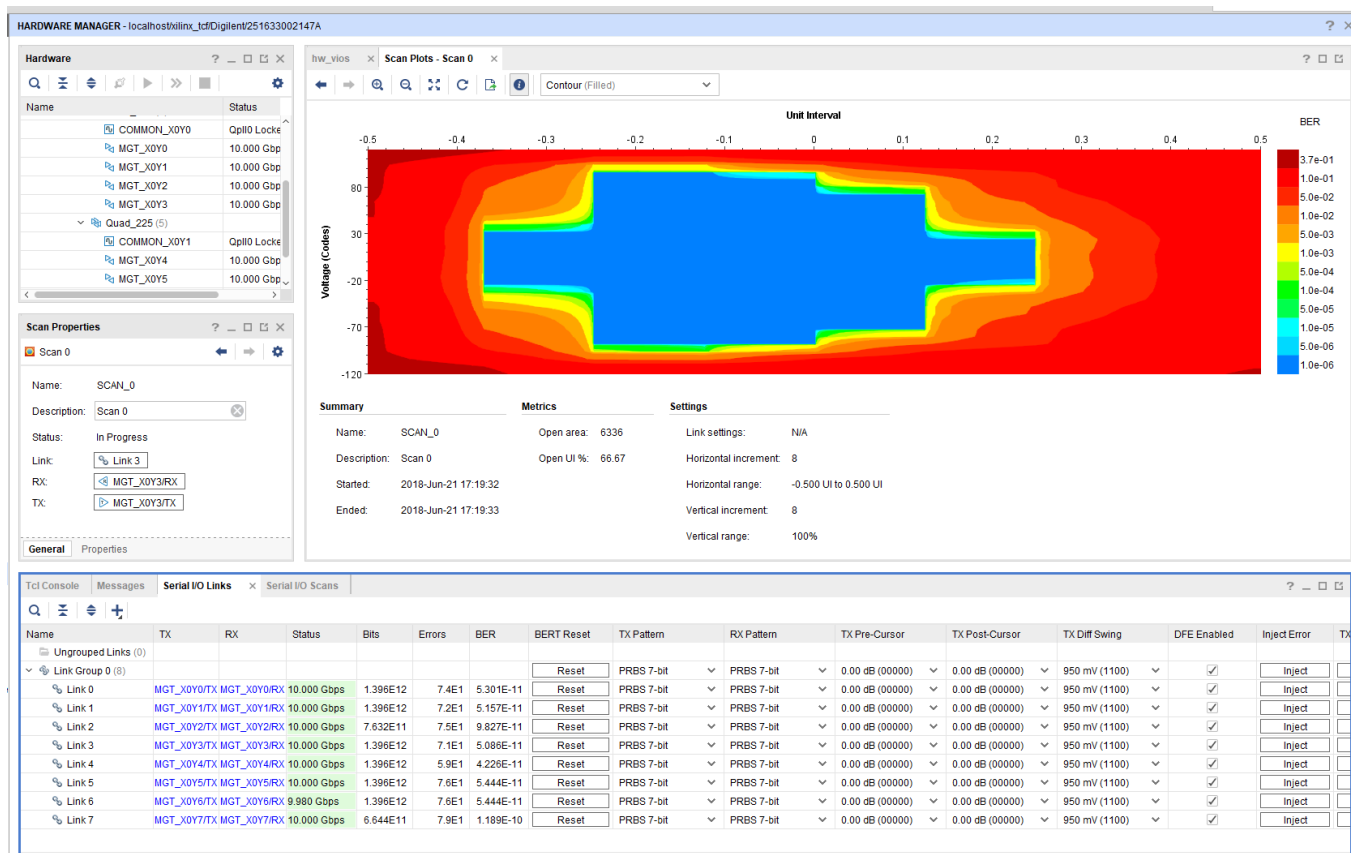
1. Connect JTAG and power on PCB
2. Open Vivado HW Manager
3. Program FPGA with Bitfile from "prebuilt\hardware\<short dir>"

Usage

1. Prepare HW like described on section [TE0841 IBERT#Programming](#)
2. Connect UART USB (most cases same as JTAG)
3. Power on PCB
Note: FPGA Loads Bitfile from Flash, MCS Firmware configure SI5338 and starts IBERT.
Do not reboot, if Bitfile programming over JTAG is used as programming method.
 - a. On TE0841 SI5338 has default configuration and reprogramming of SI5338 is optional
4. LED:
 - a. D1 (green) OFF MCS SI configuration finished (System Reset is off)

Vivado HW Manager:

1. Open Vivado HW-Manager
2. "Refresh device" is needed after Bitfile programming, because MCS reconfigure SI5338 and enables IBERT a little bit later.
 - a. loopback depends on TEB0841 Revision an connection



IBERT	Component Name	Net Name	TEB0841
X0Y0	224-0	MGT4	loop back RX/TX
X0Y1	224-1	MGT5	loop back RX/TX
X0Y2	224-2	MGT6	loopback over SD Pin header possible with lower Linerate otherwise use internal loopback
X0Y3	224-3	MGT7	loop back RX/TX. Note: N.C. on TEB0841-01, use internal loopback
X0Y4	225-0	MGT0	loop back RX/TX
X0Y5	225-1	MGT1	loop back RX/TX
X0Y6	225-2	MGT2	loop back RX/TX
X0Y7	225-3	MGT3	loopback over sfp possible

System Design - Vivado

Block Design

Design specific constrain

ibert_ultrascale_gth_0.xdc

```
# file: ibert_ultrascale_gth_0.xdc
#####
##
##  /___/ \___/
## /___/ \___/   Vendor: Xilinx
## \___/ \___/   Version : 2012.3
## \___/ \___/   Application : IBERT Ultrascale
## /___/ \___/   Filename : example_ibert_ultrascale_gth_0.xdc
## /___/ \___/
## \___/ \___/
## \___/ \___/
##
##
##
## Generated by Xilinx IBERT 7Series
#####
##
## Icon Constraints
##
create_clock -name D_CLK -period 10.0 [get_ports gth_sysclkp_i]
set_clock_groups -group [get_clocks D_CLK -include_generated_clocks] -asynchronous
set_property C_CLK_INPUT_FREQ_HZ 100000000 [get_debug_cores dbg_hub]
set_property C_ENABLE_CLK_DIVIDER true [get_debug_cores dbg_hub]

##gth_refclk lock constraints
##
set_property PACKAGE_PIN AD6 [get_ports gth_refclk0p_i[0]]
set_property PACKAGE_PIN AD5 [get_ports gth_refclk0n_i[0]]
set_property PACKAGE_PIN AB6 [get_ports gth_refclk1p_i[0]]
set_property PACKAGE_PIN AB5 [get_ports gth_refclk1n_i[0]]
##
## Refclk constraints
##
create_clock -name gth_refclk0_0 -period 8.0 [get_ports gth_refclk0p_i[0]]
create_clock -name gth_refclk1_0 -period 8.0 [get_ports gth_refclk1p_i[0]]
set_clock_groups -group [get_clocks gth_refclk0_0 -include_generated_clocks] -asynchronous
set_clock_groups -group [get_clocks gth_refclk1_0 -include_generated_clocks] -asynchronous
##
## System clock pin locs and timing constraints
##
#set_property PACKAGE_PIN R25 [get_ports gth_sysclkp_i]
#set_property IOSTANDARD LVDS [get_ports gth_sysclkp_i]
```

Software Design - SDK/HSI

For SDK project creation, follow instructions from:

[SDK Projects](#)

Application

SCU

MCS Firmware to configure SI5338 and Reset System.

Template location: \sw_lib\sw_apps\scu

Additional Software

SI5338

Download [ClockBuilder Desktop for SI5338](#)

- 1. Install and start ClockBuilder
- 2. Select SI5338
- 3. Options Open register map file
Note: File location <design name>/misc/SI5338/RegisterMap.txt
- 4. Modify settings
- 5. Options save C code header files
- 6. Replace Header files from SCU template with generated file

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
------	-------------------	---------	-------------

<p>Error rendering macro 'page-info'</p> <p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p>	<p>Error rendering macro 'page-info'</p> <p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> <div>  Unknown macro: 'metadata' </div>	<p>Error rendering macro 'page-info'</p> <p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p>	<ul style="list-style-type: none"> • some notes • Issue for PCB REV01 only: MCS is disabled on the prebuilt design files
22 Jun 2018	v.5	John Hartfiel	<ul style="list-style-type: none"> • Design update • new assembly variants (PCB REV02)
05 Jun 2018	v.4	John Hartfiel	<ul style="list-style-type: none"> • Release 2017.4

2018-04-16	v.1	<div><p>Error rendering macro 'page-info'</p><p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p></div>	<ul style="list-style-type: none">Initial release
------------	-----	--	---

	All	<div> <p>Error rendering macro 'page-info'</p> <p>Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> </div>	
--	-----	---	--

Legal Notices

Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

Document Warranty

The material contained in this document is provided "as is" and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.



Error rendering macro 'page-info'

Ambiguous method overloading for method `jdk.proxy241.$Proxy3496#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`