TE0745 IBERT

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Overview

Xilinx IBERT configured with 3.125GBits.

> Important optical transceiver will be not enable with this example design, so only copper connections works out of the box with this example design.
>
> Enable transceiver is shown in the linux example of the test_board design. Bare metal example will be follow in one of the next design updates.

Refer to http://trenz.org/te0745-info for the current online version of this manual and other available documentation.

Key Features

- Xilinx IBERT
- Modified FSBL for SI5338 programming
- Special FSBL for QSPI programming

Revision History

Date	Vivado	Project Built	Authors	Description
2019-09-18	2018.2	TE0745-IBERT_noprebuilt-vivado_2018.2-build_04_20190918103506.zip TE0745-IBERT-vivado_2018.2-build_04_20190918103450.zip	John Hartfiel	• bugfix for TE0745-02-45-3EA board parts
2018-12-19	2018.2	TE0745-IBERT_noprebuilt-vivado_2018.2-build_04_20181219143313.zip TE0745-IBERT-vivado_2018.2-build_04_20181219143258.zip	John Hartfiel	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Known Issues

Requirements

Software

Software	Version	Note
Vivado	2018.2	needed
SDK	2018.2	needed
SI5338 Clock Builder	---	optional

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0745-02-30-1I	30_1i	01,02	1GB	32MB		*xc7z030 has lower MGT count
TE0745-02-30-2IA	30_2i	01,02	1GB	64MB		*xc7z030 has lower MGT count

TE0745-02-35-1C	35_1c	01,02	1GB	32MB		
TE0745-02-45-2I	45_2i	01,02	1GB	32MB		
TE0745-02-45-2IA	45_2i	01,02	1GB	64MB		
TE0745-02-45-1C	45_1c	01,02	1GB	32MB		
TE0745-02-45-1CA	45_1c	01,02	1GB	64MB		
TE0745-02-45-3EA	45_3e	01,02	1GB	64MB		

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TEB0745	

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
SFP Loopback Adapter Module	for external loopback
Heat sink	is recommended to use with IBERT Example

Additional Hardware

Content

For general structure and of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib <design name>/hdl	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI

Design sources

Additional Sources

Type	Location	Notes
SI5338	<design name>/misc/Si5338	SI5338 Project with current PLL Configuration

Additional design sources

Prebuilt

File	File-Extension	Description

BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebult content)

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0745 "IBERT" Reference Design

Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

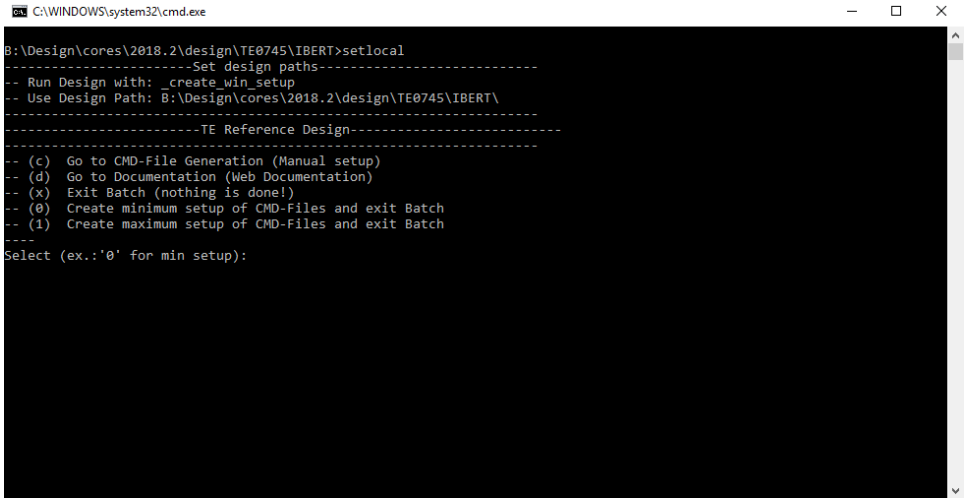
See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
   a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
      Note: Select correct one, see TE Board Part Files
5. Create HDF and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate Programming Files with HSI/SDK
   a. Run on Vivado TCL: TE::sw_run_hsi
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
      Note: See SDK Projects

Launch

Programming

> ⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp te0745_ibert
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup

SD

1. Copy Boot.bin on SD-Card.
   - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.

    - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

JTAG

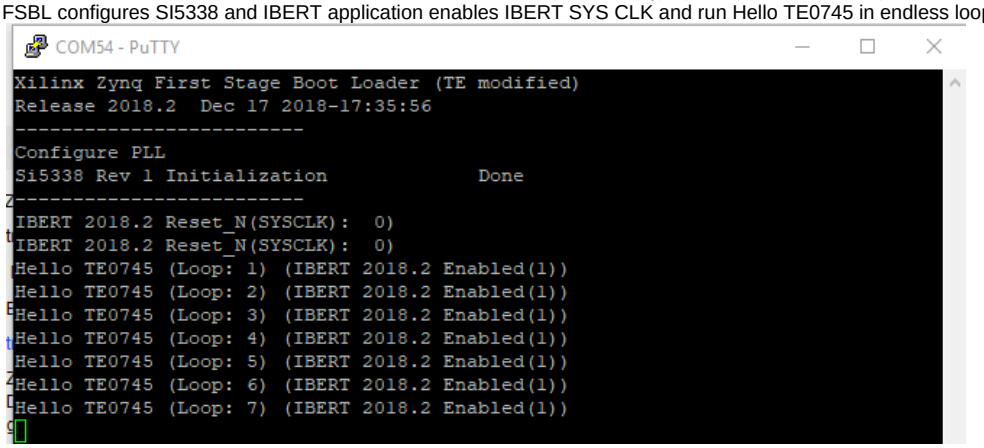
Not used on this Example.

Usage

1. Prepare HW like described on section #Programming
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode
   Note: See TRM of the Carrier, which is used.
4. Power On PCB
   Note: 1. Zynq Boot ROM loads FSBL from SD into OCM, 2. FSBL loads "IBERT Enable" App into DDR

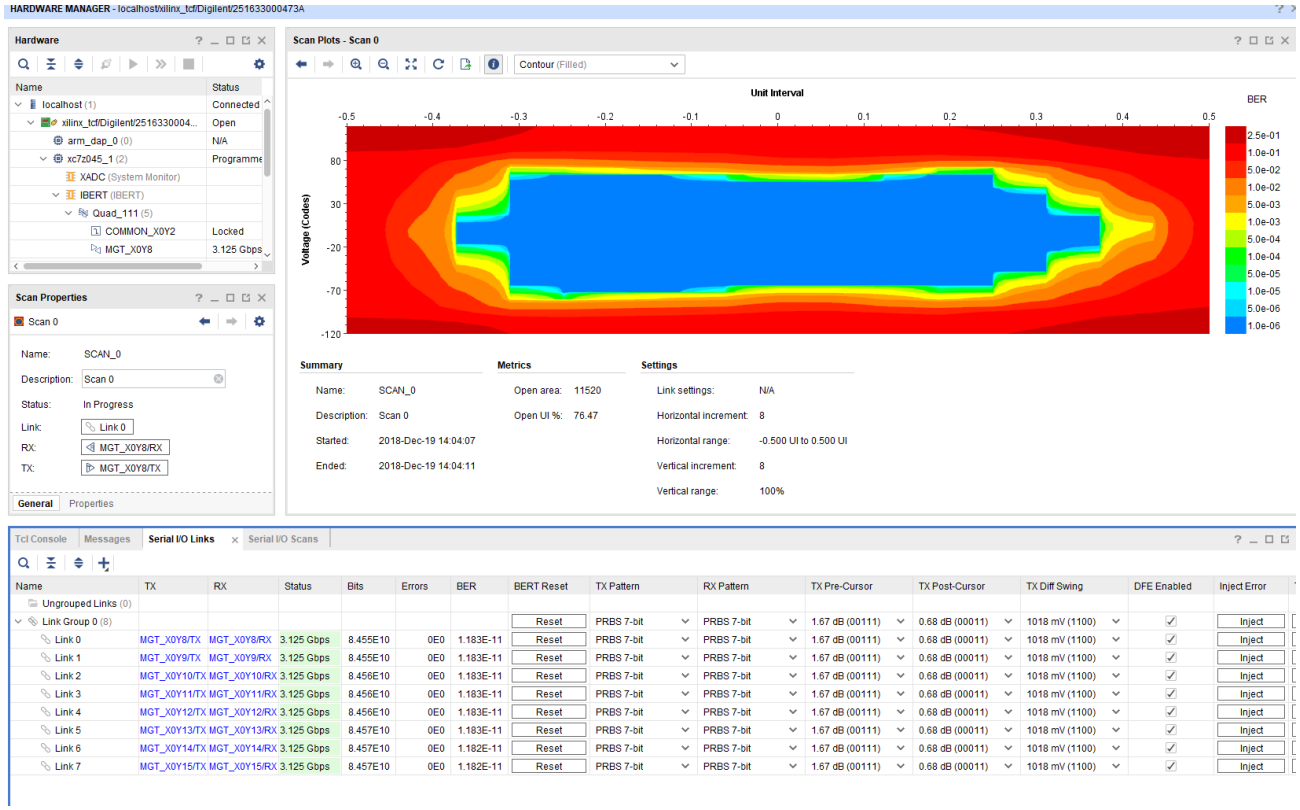
UART Console

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. FSBL configures SI5338 and IBERT application enables IBERT SYS CLK and run Hello TE0745 in endless loop



Vivado HW Manager

- Xilinx default IBERT, Link connection depends on SFP feedback connection.



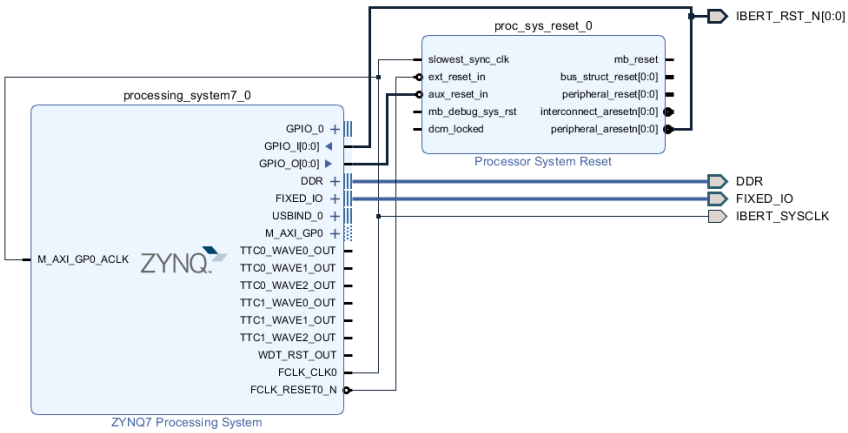
Vivado Hardware Manager

IBERT MGT (on Z045 / on Z030)	TE0745 Xil Symb	TE0745 Schem Name	TEB0745 SFP Designator
X0Y8	MGT0_111	MGT_RX/TX4	J20/21
X0Y9	MGT1_111	MGT_RX/TX5	J18/19
X0Y10	MGT2_111	MGT_RX/TX6	J15/17
X0Y11	MGT3_111	MGT_RX/TX7	J13/14
X0Y12 / X0Y0	MGT0_112	MGT_RX/TX0	J10/11
X0Y13 / X0Y1	MGT1_112	MGT_RX/TX1	J8/9
X0Y14 / X0Y2	MGT2_112	MGT_RX/TX2	J6/7
X0Y15 / X0Y3	MGT3_112	MGT_RX/TX3	J4/J5

System Design - Vivado

Block Design

BD is included into modified Xilinx IBERT export to start IBERT after SI5338 initialisation.



Block Design

PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
ETH0	MIO
USB0	MIO
SD0	MIO
UART0	MIO
I2C0	MIO
GPIO	MIO
ETH0 Reset	MIO
USB0 Reset	MIO
I2C0 Reset	MIO
GPIO	MIO
ETH0 Reset	MIO
USB0 Reset	MIO
I2C0 Reset	MIO
TTC0..1	EMIO
SWDT0	EMIO

PS Interfaces

Constrains

Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 1.8 [current_design]
set_property CFGBVS GND [current_design
```

Design specific constrain

- Note different constrain files for variants with xc7z030 assembled.

_i_example_ibert_7series_gtx_0.xdc

```
# file: ibert_7series_gtx_0.xdc
##############################################################################
##   ____  ____
##  /   /\/   /
## /___/  \  /    Vendor: Xilinx
## \   \   \/     Version : 2012.3
##  \   \         Application : IBERT 7Series
##  /   /         Filename : example_ibert_7series_gtx_0.xdc
## /___/   /\
## \   \  /  \
##  \___\/\___\
##
##
##
## Generated by Xilinx IBERT 7Series
##*************************************************************************

##
## System clock Divider paramter values
##
set_property CLKFBOUT_MULT_F 10.000 [get_cells u_ibert_core/inst/SYSCLK_DIVIDER.U_GT_MMCM]
set_property DIVCLK_DIVIDE 1 [get_cells u_ibert_core/inst/SYSCLK_DIVIDER.U_GT_MMCM]
set_property CLKIN1_PERIOD 10.0 [get_cells u_ibert_core/inst/SYSCLK_DIVIDER.U_GT_MMCM]
set_property CLKOUT0_DIVIDE_F 10.000 [get_cells u_ibert_core/inst/SYSCLK_DIVIDER.U_GT_MMCM]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_pins u_ibert_core/inst/SYSCLK_DIVIDER.U_GT_MMCM/CLKIN1]

##
## Icon Constraints
##
create_clock -name J_CLK -period 30 [get_pins -of_objects [get_cells u_ibert_core/inst/bscan_inst/SERIES7_BSCAN.
bscan_inst] -filter {name =~ *DRCK}]
#create_clock -name D_CLK -period 10.0 [get_ports SYSCLKP_I]
#set_clock_groups -group [get_clocks D_CLK] -asynchronous
set_clock_groups -group [get_clocks J_CLK] -asynchronous

##
## Clock Constraints for MGT refclk
##
create_clock -name REFCLK0_1 -period 8.0 [get_ports GTREFCLK1P_I[0]]
```

```
set_clock_groups -group [get_clocks -include_generated_clocks REFCLK0_1] -asynchronous
create_clock -name REFCLK0_0 -period 8.0 [get_ports GTREFCLK0P_I[0]]
set_clock_groups -group [get_clocks -include_generated_clocks REFCLK0_0] -asynchronous
create_clock -name REFCLK1_1 -period 8.0 [get_ports GTREFCLK1P_I[1]]
set_clock_groups -group [get_clocks -include_generated_clocks REFCLK1_1] -asynchronous
create_clock -name REFCLK1_0 -period 8.0 [get_ports GTREFCLK0P_I[1]]
set_clock_groups -group [get_clocks -include_generated_clocks REFCLK1_0] -asynchronous

##
## TX/RX out clock constraints
##
# GT X0Y8
create_clock -name Q2_RXCLK0 -period 10.24 [get_pins {u_ibert_core/inst/QUAD[0].u_q/CH[0].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q2_RXCLK0] -asynchronous
create_clock -name  Q2_TX0 -period 10.24 [get_pins {u_ibert_core/inst/QUAD[0].u_q/CH[0].u_ch/u_gtxe2_channel
/TXOUTCLK}]
set_clock_groups -group [get_clocks Q2_TX0] -asynchronous
# GT X0Y9
create_clock -name Q2_RXCLK1 -period 10.24 [get_pins {u_ibert_core/inst/QUAD[0].u_q/CH[1].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q2_RXCLK1] -asynchronous
# GT X0Y10
create_clock -name Q2_RXCLK2 -period 10.24 [get_pins {u_ibert_core/inst/QUAD[0].u_q/CH[2].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q2_RXCLK2] -asynchronous
# GT X0Y11
create_clock -name Q2_RXCLK3 -period 10.24 [get_pins {u_ibert_core/inst/QUAD[0].u_q/CH[3].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q2_RXCLK3] -asynchronous
# GT X0Y12
create_clock -name Q3_RXCLK0 -period 10.24 [get_pins {u_ibert_core/inst/QUAD[1].u_q/CH[0].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q3_RXCLK0] -asynchronous
create_clock -name  Q3_TX0 -period 10.24 [get_pins {u_ibert_core/inst/QUAD[1].u_q/CH[0].u_ch/u_gtxe2_channel
/TXOUTCLK}]
set_clock_groups -group [get_clocks Q3_TX0] -asynchronous
# GT X0Y13
create_clock -name Q3_RXCLK1 -period 10.24 [get_pins {u_ibert_core/inst/QUAD[1].u_q/CH[1].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q3_RXCLK1] -asynchronous
# GT X0Y14
create_clock -name Q3_RXCLK2 -period 10.24 [get_pins {u_ibert_core/inst/QUAD[1].u_q/CH[2].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q3_RXCLK2] -asynchronous
# GT X0Y15
create_clock -name Q3_RXCLK3 -period 10.24 [get_pins {u_ibert_core/inst/QUAD[1].u_q/CH[3].u_ch/u_gtxe2_channel
/RXOUTCLK}]
set_clock_groups -group [get_clocks Q3_RXCLK3] -asynchronous

##
## System clock pin locs and timing constraints
##
#set_property PACKAGE_PIN G7 [get_ports SYSCLKP_I]
#set_property IOSTANDARD DIFF_SSTL15 [get_ports SYSCLKP_I]
#set_property PACKAGE_PIN F7 [get_ports SYSCLKN_I]
#set_property IOSTANDARD DIFF_SSTL15 [get_ports SYSCLKN_I]

##
## GTXE2 Channel and Common Loc constraints
##
```

```
set_property LOC GTXE2_CHANNEL_X0Y8 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[0].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_CHANNEL_X0Y9 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[1].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_CHANNEL_X0Y10 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[2].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_CHANNEL_X0Y11 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[3].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_COMMON_X0Y2 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property LOC GTXE2_CHANNEL_X0Y12 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[0].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_CHANNEL_X0Y13 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[1].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_CHANNEL_X0Y14 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[2].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_CHANNEL_X0Y15 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[3].u_ch/u_gtxe2_channel]
set_property LOC GTXE2_COMMON_X0Y3 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]

##
## BUFH Loc constraints for TX/RX userclks
##
set_property LOC BUFHCE_X1Y24 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_clocking/local_txusr.NON_K7.
u_txusr]
set_property LOC BUFHCE_X1Y25 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr0]
set_property LOC BUFHCE_X1Y26 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr1]
set_property LOC BUFHCE_X1Y27 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr2]
set_property LOC BUFHCE_X1Y28 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr3]
set_property LOC BUFHCE_X1Y36 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_clocking/local_txusr.NON_K7.
u_txusr]
set_property LOC BUFHCE_X1Y37 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr0]
set_property LOC BUFHCE_X1Y38 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr1]
set_property LOC BUFHCE_X1Y39 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr2]
set_property LOC BUFHCE_X1Y40 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_clocking/rx_ind.NON_K7.
u_rxusr3]


##
## MGT reference clock BUFFERS location constraints
##
set_property LOC IBUFDS_GTE2_X0Y4 [get_cells u_buf_q2_clk0]
set_property LOC IBUFDS_GTE2_X0Y5 [get_cells u_buf_q2_clk1]
set_property LOC IBUFDS_GTE2_X0Y6 [get_cells u_buf_q3_clk0]
set_property LOC IBUFDS_GTE2_X0Y7 [get_cells u_buf_q3_clk1]

##
## Asynchronous constraints for Userclks and systemclock clock groups
##
#set_clock_groups -group [get_clocks Q*_RXCLK*] -group [get_clocks Q*_TX*] -asynchronous
#set_clock_groups -group [get_clocks D_CLK*] -group [get_clocks Q*_TX*] -asynchronous
#set_clock_groups -group [get_clocks Q*_RXCLK*] -group [get_clocks D_CLK*] -asynchronous
#set_clock_groups -group [get_generated_clocks -of_objects [get_pins u_ibert_core/inst/SYSCLK_DIVIDER.U_GT_MMCM
/CLKOUT0]] -group [get_clocks Q*_TX*] -asynchronous
#set_clock_groups -group [get_clocks Q*_RXCLK*] -group [get_generated_clocks -of_objects [get_pins u_ibert_core
/inst/SYSCLK_DIVIDER.U_GT_MMCM/CLKOUT0]] -asynchronous

##
## Set Case Analysis constraints for fabric clock calculation
##
#MUX select QPLLREFCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/u_common/U_COMPLEX_REGS/reg_202/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[2]/Q ]
```

```
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[0].u_q/u_common/U_COMPLEX_REGS/reg_202/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[1]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/u_common/U_COMPLEX_REGS/reg_202/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[0]/Q ]
#MUX select CPLLREFCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[6]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[5]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[4]/Q ]
#MUX select RXRATE:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_216/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[5]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_216/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[4]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_216/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[3]/Q ]
#MUX select TXRATE:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[8]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[7]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[6]/Q ]
#MUX select RXOUTCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[15]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[14]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[13]/Q ]
#MUX select TXOUTCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[2]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[1]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[0]/Q ]
#MUX select QPLLREFCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/u_common/U_COMPLEX_REGS/reg_202/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[2]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[1].u_q/u_common/U_COMPLEX_REGS/reg_202/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[1]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/u_common/U_COMPLEX_REGS/reg_202/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[0]/Q ]
#MUX select CPLLREFCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[6]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[5]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[4]/Q ]
#MUX select RXRATE:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_216/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[5]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_216/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[4]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_216/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[3]/Q ]
#MUX select TXRATE:
```

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set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[8]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[7]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[6]/Q ]
#MUX select RXOUTCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[15]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[14]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_215/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[13]/Q ]
#MUX select TXOUTCLKSEL:
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[2]/Q ]
set_case_analysis 1 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[1]/Q ]
set_case_analysis 0 [get_pins u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/U_CHANNEL_REGS/reg_217/I_EN_CTL_EQ1.U_CTL
/xsdb_reg_reg[0]/Q ]

##
## Attribute values for GTXE2 Channel and Common instances
##
##
## Attribute Values for QUAD[2] - Channel
##

 ##------Comma Detection and Alignment---------
set_property ALIGN_COMMA_DOUBLE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_COMMA_ENABLE 10'b0001111111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ALIGN_COMMA_WORD 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_MCOMMA_DET "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_MCOMMA_VALUE 10'b1010000011 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ALIGN_PCOMMA_DET "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_PCOMMA_VALUE 10'b0101111100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property DEC_MCOMMA_DETECT "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property DEC_PCOMMA_DETECT "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property DEC_VALID_COMMA_ONLY "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property DMONITOR_CFG 24'h000A01 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##--------------Channel Bonding--------------
set_property CBCC_DATA_SOURCE_SEL "DECODED" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_KEEP_ALIGN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_MAX_SKEW 7 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_LEN 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_1 10'b0101111100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_1 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
```

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/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_USE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------Clock Correction------------
set_property CLK_COR_KEEP_IDLE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_MAX_LAT 19.0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_MIN_LAT 15.0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_PRECEDENCE "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_CORRECT_USE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_REPEAT_WAIT 0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_LEN 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_1 10'b0100011100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_1 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_USE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------Channel PLL----------------------
set_property CPLL_CFG 24'hBC07DC [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_FBDIV 5 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_FBDIV_45 5 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_INIT_CFG 24'h00001E [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_LOCK_CFG 16'h01C0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_REFCLK_DIV 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXOUT_DIV 2 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXOUT_DIV 2 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------------Eyescan--------------
set_property ES_CONTROL 6'b000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_ERRDET_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_EYE_SCAN_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_HORZ_OFFSET 12'h000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_PMA_CFG 10'b0000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_PRESCALE 5'b00000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_QUALIFIER 80'h00000000000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ES_QUAL_MASK 80'h00000000000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ES_SDATA_MASK 80'h00000000000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ES_VERT_OFFSET 9'b000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property FTS_DESKEW_SEQ_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property FTS_LANE_DESKEW_CFG 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property FTS_LANE_DESKEW_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property GEARBOX_MODE 3'b000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property OUTREFCLK_SEL_INV 2'b11 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PCS_PCIE_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PCS_RSVD_ATTR 48'h000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PMA_RSV 32'h00018480 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PMA_RSV2 16'h2070 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
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set_property PMA_RSV3 2'b00 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_BIAS_CFG 12'b000000000100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------Rx Elastic Buffer and Phase alignment-------------
set_property RXBUF_ADDR_MODE "FAST" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_EIDLE_HI_CNT 4'b1000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_EIDLE_LO_CNT 4'b0000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_BUFFER_CFG 6'b000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_RESET_ON_CB_CHANGE "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXBUF_RESET_ON_COMMAALIGN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXBUF_RESET_ON_EIDLE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_RESET_ON_RATE_CHANGE "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXBUFRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_THRESH_OVFLW 61 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_THRESH_OVRD "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_THRESH_UNDFLW 4 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDLY_CFG 16'h001F [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDLY_LCFG 9'h030 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDLY_TAP_CFG 16'h0000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------RX driver, OOB signalling, Coupling and Eq., CDR------------
set_property RXCDR_CFG 72'h03800023FF40200020 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXCDRFREQRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_FR_RESET_ON_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_HOLD_DURING_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_LOCK_CFG 6'b010101 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_PH_RESET_ON_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDRPHRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDFELPMRESET_TIME 7'b0001111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXOOB_CFG 7'b0000110 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------------------RX Interface-------------------------
set_property RX_INT_DATAWIDTH 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DATA_WIDTH 32 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CLKMUX_PD 1'b1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CLK25_DIV 5 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CM_SEL 2'b11 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CM_TRIM 3'b100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DDI_SEL 6'b000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DEBUG_CFG 12'b000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------RX Decision Feedback Equalizer(DFE)-------------
set_property RX_DEFER_RESET_BUF_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_GAIN_CFG 23'h020FEA [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H2_CFG 12'b000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H3_CFG 12'b000001000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H4_CFG 11'b00011110000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H5_CFG 11'b00011100000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_LPM_HOLD_DURING_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_KL_CFG 13'b0000011111110 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_KL_CFG2 32'h3010D90C [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_LPM_CFG 16'h0954 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_OS_CFG 13'b0000010000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_UT_CFG 17'b10001111000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
```

```
/u_gtxe2_channel]
set_property RX_DFE_VP_CFG 17'b00011111100000011 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_XYD_CFG 13'b0000000000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DISPERR_SEQ_MATCH "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------------------RX Gearbox---------------------------
set_property RXGEARBOX_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXISCANRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXLPM_HF_CFG 14'b00000011110000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXLPM_LF_CFG 14'b00000011110000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXPCSRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPH_CFG 24'h000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPHDLY_CFG 24'h084020 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPH_MONITOR_SEL 5'b00000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPMARESET_TIME 5'b00011 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------------------PRBS Detection-----------------------
set_property RXPRBS_ERR_LOOPBACK 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_SIG_VALID_DLY 10 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXSLIDE_AUTO_WAIT 7 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXSLIDE_MODE "off" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_XCLK_SEL "RXREC" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------RX Attributes for PCI Express/SATA/SAS----------
set_property PD_TRANS_TIME_FROM_P2 12'h03c [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PD_TRANS_TIME_NONE_P2 8'h3c [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PD_TRANS_TIME_TO_P2 8'h64 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SAS_MAX_COM 64 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SAS_MIN_COM 36 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_BURST_SEQ_LEN 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_BURST_VAL 3'b100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_CPLL_CFG "VCO_3000MHZ" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_EIDLE_VAL 3'b100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MAX_BURST 8 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MAX_INIT 21 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MAX_WAKE 7 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MIN_BURST 4 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MIN_INIT 12 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MIN_WAKE 4 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SHOW_REALIGN_COMMA "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TERM_RCAL_CFG 5'b10000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TERM_RCAL_OVRD 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TRANS_TIME_RATE 8'h0E [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TST_RSV 32'h00000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------TX Buffering and Phase Alignment----------------
set_property TXBUF_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXBUF_RESET_ON_RATE_CHANGE "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch
/u_gtxe2_channel]

 ##-----------------------TX Interface-------------------------
set_property TX_DATA_WIDTH 32 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_DEEMPH0 5'b00000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_DEEMPH1 5'b00000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXDLY_CFG 16'h001F [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXDLY_LCFG 9'h030 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXDLY_TAP_CFG 16'h0000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
```

```
set_property TX_INT_DATAWIDTH 1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_CLKMUX_PD 1'b1 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_CLK25_DIV 5 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##--------------TX Driver and OOB Signalling------------------
set_property TX_EIDLE_ASSERT_DELAY 3'b110 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_EIDLE_DEASSERT_DELAY 3'b100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_LOOPBACK_DRIVE_HIZ "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MAINCURSOR_SEL 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_DRIVE_MODE "DIRECT" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------------------TX Gearbox---------------------------
set_property TXGEARBOX_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##----------------TX Attributes for PCI Express---------------
set_property TX_MARGIN_FULL_0 7'b1001110 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_1 7'b1001001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_2 7'b1000101 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_3 7'b1000010 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_4 7'b1000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_0 7'b1000110 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_1 7'b1000100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_2 7'b1000010 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_3 7'b1000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_4 7'b1000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPCSRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPH_CFG 16'h0780 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPHDLY_CFG 24'h084020 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPH_MONITOR_SEL 5'b00000 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPMARESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_PREDRIVER_MODE 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_QPI_STATUS_EN 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_RXDETECT_CFG 14'h1832 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_RXDETECT_REF 3'b100 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_XCLK_SEL "TXOUT" [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property UCODEER_CLR 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/CH[*].u_ch/u_gtxe2_channel]
##
## Attribute Values for QUAD[2] - Common
##
set_property BIAS_CFG 64'h0000040000001000 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property COMMON_CFG 32'h00000000 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_CFG 27'h06801C1 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_CLKOUT_CFG 4'b0000 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_COARSE_FREQ_OVRD 6'b010000 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_COARSE_FREQ_OVRD_EN 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_CP 10'b0000011111 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_CP_MONITOR_EN 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_DMONITOR_SEL 1'b0 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_FBDIV_MONITOR_EN 1'b1 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_INIT_CFG 24'h000028 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_LOCK_CFG 16'h21E8 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_LPF 4'b1111 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
set_property QPLL_REFCLK_DIV 2 [get_cells u_ibert_core/inst/QUAD[0].u_q/u_common/u_gtxe2_common]
##
## Attribute Values for QUAD[3] - Channel
##

 ##------Comma Detection and Alignment---------
set_property ALIGN_COMMA_DOUBLE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_COMMA_ENABLE 10'b0001111111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
```

```
set_property ALIGN_COMMA_WORD 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_MCOMMA_DET "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_MCOMMA_VALUE 10'b1010000011 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ALIGN_PCOMMA_DET "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ALIGN_PCOMMA_VALUE 10'b0101111100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property DEC_MCOMMA_DETECT "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property DEC_PCOMMA_DETECT "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property DEC_VALID_COMMA_ONLY "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property DMONITOR_CFG 24'h000A01 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##--------------Channel Bonding--------------
set_property CBCC_DATA_SOURCE_SEL "DECODED" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_KEEP_ALIGN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_MAX_SKEW 7 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_LEN 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_1 10'b0101111100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_1_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_1 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CHAN_BOND_SEQ_2_USE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------Clock Correction------------
set_property CLK_COR_KEEP_IDLE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_MAX_LAT 19.0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_MIN_LAT 15.0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_PRECEDENCE "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_CORRECT_USE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_REPEAT_WAIT 0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_LEN 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_1 10'b0100011100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_1_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_1 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_2 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_3 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_4 10'b0100000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CLK_COR_SEQ_2_USE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------Channel PLL----------------------
set_property CPLL_CFG 24'hBC07DC [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_FBDIV 5 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_FBDIV_45 5 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
```

```
set_property CPLL_INIT_CFG 24'h00001E [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_LOCK_CFG 16'h01C0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property CPLL_REFCLK_DIV 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXOUT_DIV 2 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXOUT_DIV 2 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------------Eyescan--------------
set_property ES_CONTROL 6'b000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_ERRDET_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_EYE_SCAN_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_HORZ_OFFSET 12'h000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_PMA_CFG 10'b0000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_PRESCALE 5'b00000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property ES_QUALIFIER 80'h00000000000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ES_QUAL_MASK 80'h00000000000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ES_SDATA_MASK 80'h00000000000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property ES_VERT_OFFSET 9'b000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property FTS_DESKEW_SEQ_ENABLE 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property FTS_LANE_DESKEW_CFG 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property FTS_LANE_DESKEW_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property GEARBOX_MODE 3'b000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property OUTREFCLK_SEL_INV 2'b11 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PCS_PCIE_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PCS_RSVD_ATTR 48'h000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PMA_RSV 32'h00018480 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PMA_RSV2 16'h2070 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PMA_RSV3 2'b00 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_BIAS_CFG 12'b000000000100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------Rx Elastic Buffer and Phase alignment-------------
set_property RXBUF_ADDR_MODE "FAST" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_EIDLE_HI_CNT 4'b1000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_EIDLE_LO_CNT 4'b0000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_BUFFER_CFG 6'b000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_RESET_ON_CB_CHANGE "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXBUF_RESET_ON_COMMAALIGN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXBUF_RESET_ON_EIDLE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_RESET_ON_RATE_CHANGE "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXBUFRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_THRESH_OVFLW 61 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_THRESH_OVRD "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXBUF_THRESH_UNDFLW 4 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDLY_CFG 16'h001F [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDLY_LCFG 9'h030 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDLY_TAP_CFG 16'h0000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------RX driver, OOB signalling, Coupling and Eq., CDR------------
set_property RXCDR_CFG 72'h03800023FF40200020 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXCDRFREQRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_FR_RESET_ON_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_HOLD_DURING_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_LOCK_CFG 6'b010101 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXCDR_PH_RESET_ON_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
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set_property RXCDRPHRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXDFELPMRESET_TIME 7'b0001111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXOOB_CFG 7'b0000110 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------------------RX Interface-------------------------
set_property RX_INT_DATAWIDTH 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DATA_WIDTH 32 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CLKMUX_PD 1'b1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CLK25_DIV 5 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CM_SEL 2'b11 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_CM_TRIM 3'b100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DDI_SEL 6'b000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DEBUG_CFG 12'b000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------RX Decision Feedback Equalizer(DFE)-------------
set_property RX_DEFER_RESET_BUF_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_GAIN_CFG 23'h020FEA [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H2_CFG 12'b000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H3_CFG 12'b000001000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H4_CFG 11'b00011110000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_H5_CFG 11'b00011100000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_LPM_HOLD_DURING_EIDLE 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_KL_CFG 13'b0000011111110 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_KL_CFG2 32'h3010D90C [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_LPM_CFG 16'h0954 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_OS_CFG 13'b0000010000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_DFE_UT_CFG 17'b10001111000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_VP_CFG 17'b00011111100000011 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DFE_XYD_CFG 13'b0000000000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RX_DISPERR_SEQ_MATCH "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------------------RX Gearbox---------------------------
set_property RXGEARBOX_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXISCANRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXLPM_HF_CFG 14'b00000011110000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXLPM_LF_CFG 14'b00000011110000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]
set_property RXPCSRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPH_CFG 24'h000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPHDLY_CFG 24'h084020 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPH_MONITOR_SEL 5'b00000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXPMARESET_TIME 5'b00011 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------------------PRBS Detection------------------------
set_property RXPRBS_ERR_LOOPBACK 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_SIG_VALID_DLY 10 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXSLIDE_AUTO_WAIT 7 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RXSLIDE_MODE "off" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property RX_XCLK_SEL "RXREC" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------RX Attributes for PCI Express/SATA/SAS----------
set_property PD_TRANS_TIME_FROM_P2 12'h03c [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PD_TRANS_TIME_NONE_P2 8'h3c [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property PD_TRANS_TIME_TO_P2 8'h64 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SAS_MAX_COM 64 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
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set_property SAS_MIN_COM 36 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_BURST_SEQ_LEN 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_BURST_VAL 3'b100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_CPLL_CFG "VCO_3000MHZ" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_EIDLE_VAL 3'b100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MAX_BURST 8 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MAX_INIT 21 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MAX_WAKE 7 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MIN_BURST 4 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MIN_INIT 12 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SATA_MIN_WAKE 4 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property SHOW_REALIGN_COMMA "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TERM_RCAL_CFG 5'b10000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TERM_RCAL_OVRD 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TRANS_TIME_RATE 8'h0E [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TST_RSV 32'h00000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##------------TX Buffering and Phase Alignment----------------
set_property TXBUF_EN "TRUE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXBUF_RESET_ON_RATE_CHANGE "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch
/u_gtxe2_channel]

 ##-----------------------TX Interface------------------------
set_property TX_DATA_WIDTH 32 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_DEEMPH0 5'b00000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_DEEMPH1 5'b00000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXDLY_CFG 16'h001F [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXDLY_LCFG 9'h030 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXDLY_TAP_CFG 16'h0000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_INT_DATAWIDTH 1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_CLKMUX_PD 1'b1 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_CLK25_DIV 5 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##--------------TX Driver and OOB Signalling------------------
set_property TX_EIDLE_ASSERT_DELAY 3'b110 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_EIDLE_DEASSERT_DELAY 3'b100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_LOOPBACK_DRIVE_HIZ "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MAINCURSOR_SEL 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_DRIVE_MODE "DIRECT" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##-----------------------TX Gearbox---------------------------
set_property TXGEARBOX_EN "FALSE" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]

 ##----------------TX Attributes for PCI Express---------------
set_property TX_MARGIN_FULL_0 7'b1001110 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_1 7'b1001001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_2 7'b1000101 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_3 7'b1000010 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_FULL_4 7'b1000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_0 7'b1000110 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_1 7'b1000100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_2 7'b1000010 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_3 7'b1000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_MARGIN_LOW_4 7'b1000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPCSRESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPH_CFG 16'h0780 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPHDLY_CFG 24'h084020 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPH_MONITOR_SEL 5'b00000 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TXPMARESET_TIME 5'b00001 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_PREDRIVER_MODE 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_QPI_STATUS_EN 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
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set_property TX_RXDETECT_CFG 14'h1832 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_RXDETECT_REF 3'b100 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property TX_XCLK_SEL "TXOUT" [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
set_property UCODEER_CLR 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/CH[*].u_ch/u_gtxe2_channel]
##
## Attribute Values for QUAD[3] - Common
##
set_property BIAS_CFG 64'h0000040000001000 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property COMMON_CFG 32'h00000000 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_CFG 27'h06801C1 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_CLKOUT_CFG 4'b0000 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_COARSE_FREQ_OVRD 6'b010000 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_COARSE_FREQ_OVRD_EN 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_CP 10'b0000011111 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_CP_MONITOR_EN 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_DMONITOR_SEL 1'b0 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_FBDIV_MONITOR_EN 1'b1 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_INIT_CFG 24'h000028 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_LOCK_CFG 16'h21E8 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_LPF 4'b1111 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
set_property QPLL_REFCLK_DIV 2 [get_cells u_ibert_core/inst/QUAD[1].u_q/u_common/u_gtxe2_common]
```

Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

Application

Template location: ./sw_lib/sw_apps/

zynq_fsbl

TE modified 2018.2 FSBL

Changes:

- Si5338 Configuration see fsbl_hooks.c
- Add register_map.h, si5338.c, si5338.h

zynq_fsbl_flash

TE modified 2018.2 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

te0745_ibert

Enable IBERT SysCLK and print Hello TE0745 a Xilinx Hello World example as endless loop instead of one console output.

Additional Software

SI5338

File location <design name>/misc/Si5338/RegisterMap.txt

General documentation how you work with these project will be available on Si5338

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• IBERT Mapping Table add Z030 Names

2019-09-18	v.4	John Hartfiel	• bugfix for TE0745-02-45-3EA
2018-12-19	v.2	John Hartfiel	• 2018.2 initial release
--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	--

Document change history.

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Error rendering macro 'page-info'

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